A Low-Voltage, High Efficiency Power Generation Structure for UHF RFID

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Abstract: This paper presents a new power generation structure that can provide DC energy for passive UHF RFID with high sensitivity and high efficiency. The structure is designed with 0.18μm standard CMOS technology, including two charge pumps, a current reference, and a group of bias circuits. Low-voltage performance is improved thanks to the bias structure, which eliminates the threshold voltage drop and body-effect of conventional circuits. A 350mV minimum input level is required to generate a 1.5V power supply for a 100kΩ load with power conversion efficiency (PCE) of 22%. PCE up to 29.8% is achieved with a 60kΩ load. Simulation results show that the new circuit is superior to conventional charge pumps.

Key words: UHF RFID; power generation; charge pump; low voltage; CMOS
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1 Introduction

Radio frequency identification (RFID) technology is gradually replacing optical bar reading architectures in many areas such as retail industry, goods storage, and management. Industries looking for reliable, tiny, and inexpensive ways to control products are focusing on passive UHF RFID tags, which allow a long read and write operation from up to a few meters without any external battery or power generator, only obtaining a power supply from electromagnetic fields, therefore, providing a great advantage both in terms of size and cost[1]. As a passive device, the on-chip power generation circuit that converts RF signal into DC energy is an essential element that greatly affects the performance of passive UHF RFID. Since it is difficult for circuits to work with input levels beneath the threshold, which always occurs when tags are meters away from the readers, many solutions have been reported to eliminate threshold voltage and improve PCE, such as designing rectifiers[2,3] based on Schottky diodes, SOI,[4] or FeRAM[5] technologies. However, methods based on circuit improvement, such as rectifiers with bias circuits,[5,6] are preferable. Without precise bias control and power limitation, conventional biased rectifiers[5,6] are enduring dramatical power and PCE loss from small signal input. To resolve these drawbacks and improve low voltage performance, a novel circuit structure with a start up circuit and a precise bias circuit based on current mirror technology is proposed in this paper.

2 Analysis of conventional circuit

To understand the proposed structure, a traditional Dickson charge pump[7] is analyzed. As illustrated in Fig. 1, the input signal RF_INPUT acts as a clock to charge pump while the MOS transistors with gate and drain connected act as diodes.

For a simple analysis, the input signal is considered as a square wave and the body-effect is neglected, hence the output voltage is estimated as follows.

$$V_{\mathrm{DD\_output}} = NG_{\mathrm{V}} - \frac{NI_{\mathrm{out}}}{(C + C_{\mathrm{s}})f} \tag{1}$$

where G_{V} is the voltage gain for each stage.

$$G_{\mathrm{V}} = V_{\mathrm{RF}}\left(\frac{C}{C + C_{\mathrm{s}}}\right) - V_{\mathrm{th}} \tag{2}$$

N, C, C_{s}, V_{RF}, V_{th}, I_{out} and f are the number of stages, couple capacitance, parasitic capacitance, input signal amplitude, threshold voltage, output current, and frequency, respectively. V_{th} is significant because it reduces G_{V} and the output voltage. When V_{RF} equals or is less than V_{th}, output voltage is close to zero because transistors of the charge pump cannot turn on.

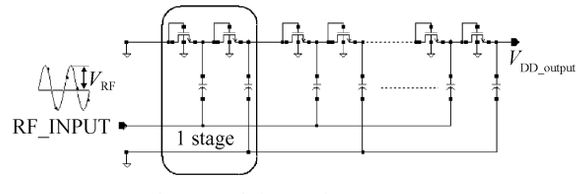

Fig. 1 Dickson charge pump

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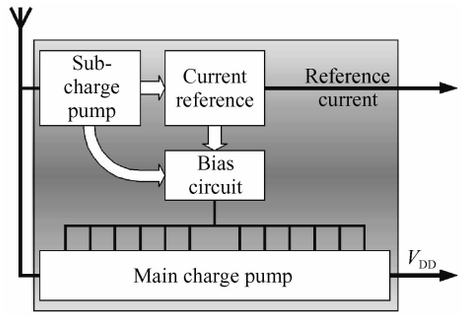

Fig. 2 Proposed power generation structure

If the body-effect is taken into account, V_{th} in Eqs. (1) and (2) is replaced by

$$V_{thb} = V_{th0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \quad (3)$$

where V_{th0} is the intrinsic threshold voltage, V_{SB} is the voltage between source and bulk, ϕ_F is the Fermi potential, and γ is the body-effect coefficient which is defined as:

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \quad (4)$$

Since MOS transistors in latter stages have higher V_{SB}, hence higher V_{thb}, according to Eqs. (1) and (2), more voltage and energy are wasted in the charge pump itself. Therefore, the input level must be 300 or 400mV higher than the threshold voltage in order to sufficiently turn on transistors and compensate the body-effect.

3 Circuit implementation

The proposed circuit structure is shown in Fig. 2. The main charge pump supplies power to internal circuits of UHF RFID, while the bias circuit, the sub-charge pump, and the current reference gives stable and precise bias voltage to eliminate the body-effect and the threshold voltage of the main charge pump. Thus, the main charge pump has a threshold voltage close to zero.

3.1 Main charge pump and bias circuit

As illustrated in Fig. 3 (a), the main charge pump and relative bias circuit act as a group of current mirrors. When there is a constant current flow through the transistor in the bias circuit, a voltage equal to the threshold is established. This voltage acts on the drain and gate of transistors in the charge pump and eliminates threshold loss. The body-effect is eliminated by connecting the bias circuit to the transistors in the charge pump respectively. Therefore, the bias voltage varies with the threshold voltage change due to the body-effect. The equivalent circuit of the first stage is shown in Fig. 3 (b).

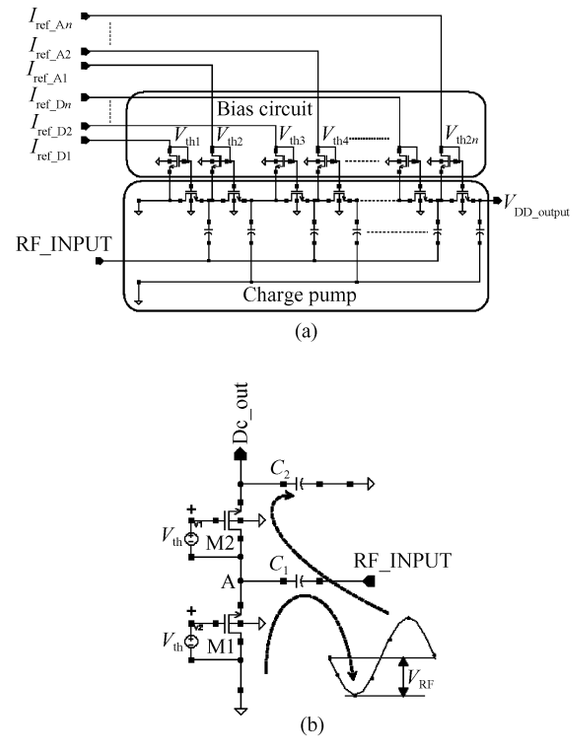

Fig. 3 Proposed main charge pump (a) and bias circuit (b)

When RF_INPUT swings to negative phase, as illustrated in Fig. 3(b), for M1

$$V_{gs} = V_{ds} + V_{thb} \quad (5)$$

Thus, M1 is constantly biased at the triode region. With RF_INPUT acting on V_{ds}, V_{gs} is high enough to drive M1 into the strong inversion region, which enables a large current to charge C_1. In the positive phase, the definition of source and gate is switched. V_{gs} is clamped to V_{thb} and only a small sub-threshold leakage current flows from C_1 to GND, while a large part of the current flows through M2 charging C_2. Therefore, transistors in the main charge pump act as diodes with threshold voltage close to zero. The number of stages is limited to 6 for optimized performance.

3.2 Current reference and bias distributor

To provide proper current source, a low power, low voltage constant current reference and its distributor circuit was designed. Figure 4 illustrates the schematic.

The current reference, the startup circuit, and the operational amplifier generate a stable reference current. The bias distributor duplicates this current and directs it to each bias circuit. The current $I_{ref\_D1} \sim I_{ref\_Dn}$ provide constant current for bias circuits connected to the DC signal input, while $I_{ref\_A1} \sim I_{ref\_An}$ for those connected to the AC signal, as illustrated in Fig. 3.

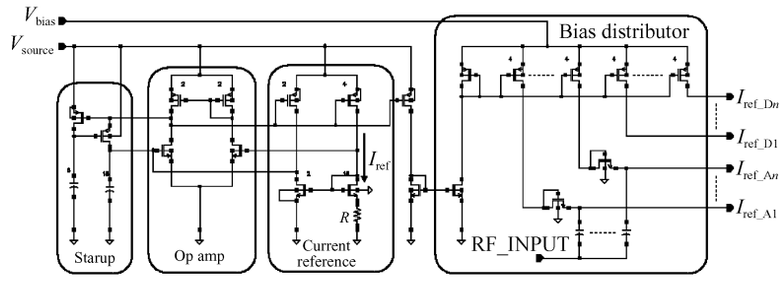

Fig. 4　Current reference

3.3　Sub-charge pump

The sub-charge pump works before any other circuits，providing voltage higher than the main charge pump，but the current has to be small enough to minimize power consumption. Therefore，a 10-stage NCP-2 Dickson charge pump with self-biasing ability is designed，as shown in Fig. 5. Native nMOS transistor is used for the sub-charge pump because its threshold voltage is nearly zero and it is fully process-compatible with the standard CMOS process without adding an extra mask. Due to the high leakage，the native nMOS transistor is not suitable for driving a heavy load，so the size is minimized.

The output of the sub-charge pump is separated into V_{source} and V_{bias} in order to keep a clean power supply for the current reference circuit.

4　Results

The proposed structure was built and simulated with TSMC 0.18μm technology in which the normal threshold voltage is 400mV. The simulation frequency is 900MHz. Figure 6 (a) shows the PCE varies with different input powers and output loads. For every load condition，PCE first increases with input power before decreasing after the peak level. At the beginning，the increasing input power enlarges the overdrive voltage of transistors，hence improving PCE. Later，the increasing output current gradually becomes a domain factor，which reduces overall PCE because it causes more power loss on the transistors. Figure 6 (b) shows the relationship between input and output voltage. For 1.5V output at 100kΩ load，the minimum input voltage is 350mV，while the traditional design has no voltage output because transistors are unable to turn on when the input voltage is beneath the threshold. Figure 6 (c) gives the relationship between input power and output voltage. The curve shows the minimum input power for 1.4V output at 200kΩ load is -14dBm.

Figure 6 (d) shows the power consumption ratio of each part. A large part of the energy is lost in the main charge pump due to its large size and the large parasitic capacitance of the transistors，while the add-on circuits consume a small portion of energy but make a great contribution to the improvement of PCE and low voltage performance.

Figure 7 gives a comparison of voltage gain in each stage of the proposed structure and a Dickson charge pump. For the same voltage output，900mV input is required for a Dickson charge pump，while the proposed structure requires only 370mV. Because threshold loss and body-effect is eliminated，the proposed structure has the same voltage gain in each stage，while the old structure suffers a smaller gain in latter stages. Longer setup time is required for the proposed structure，since the current reference needs time to stabilize before the main charge pump is biased. According to the ISO/IEC 18000-6C standard，this delay is acceptable.

Table 1 gives a comparison between the conventional power generation structures[6,7] and the proposed structure.

With 200kΩ load and -14dBm input power，the proposed structure can supply 1.4V output with PCE of 18.5%，which is much higher than conventional structures. When the input level increases，output voltage and PCE of the proposed structure increase as well，and it still shows higher driving ability than conventional structures. This comparison indicates a great enhancement in low power input conditions，which gives the passive UHF RFID a longer read/write range.

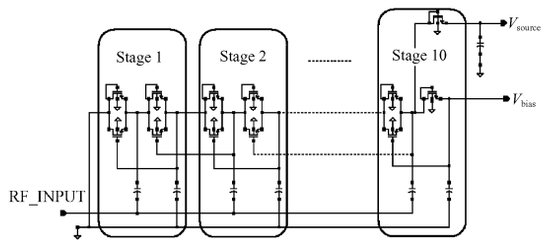

Fig. 5　Sub-charge pump

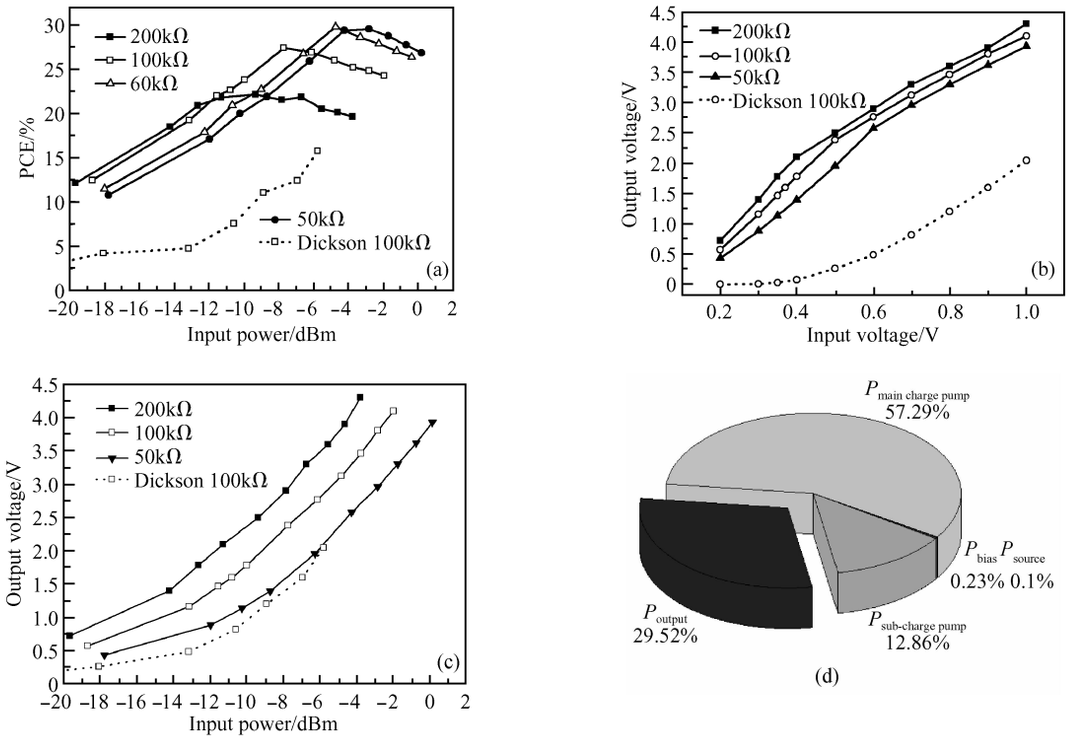

Fig. 6 (a) PCE versus input power; (b) Output voltage versus input voltage; (c) Output voltage versus input power; (d) Power consumption of each part

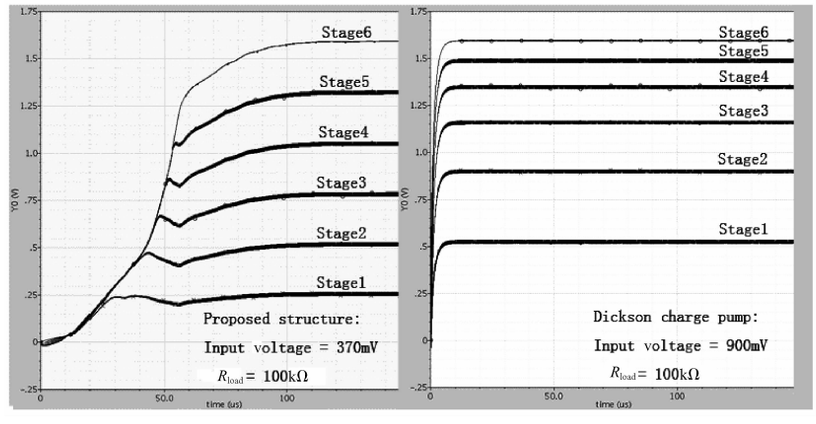

Fig. 7 Comparison of voltage gain between the traditional and proposed structures

Table 1 Comparison of different CMOS power generation structures

Input power/dBm		−14	−12	−10
Proposed structure	Output voltage/V	1.4	1.78	2.5
	PCE/%	18.5	20.9	22
Conventional structure[6]	Output voltage/V	1.5	1.6	1.7
	PCE/%	1.2	4	7
Conventional structure[8]	Output voltage/V	1.25	1.6	2.75
	PCE/%	3	12	20

5 Conclusion

A new power generation structure for passive UHF RFID has been presented. The structure is designed with 0.18μm standard CMOS technology and includes two charge pumps, a current reference, and a group of bias circuits. On account of this new circuit design, performance in low voltage input is dramatically improved thanks to the carefully designed bias structure, which eliminates the threshold voltage drop and body-effect of conventional circuits. As shown in the simulation results, the new structure yields much higher sensitivity and efficiency than traditional Dickson charge pumps. Therefore, the proposed structure is suitable for low cost, high performance passive UHF RFID applications.

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一种用于 UHF RFID 的低压高效电源产生电路

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摘要：介绍了一种为无源 UHF RFID 设计的高效高灵敏度电源产生电路.该电路基于 0.18μm 工艺，其中包含了两个电荷泵，一个参考电流源和一组偏置电路.由于其偏置电路消除了传统电路中的阈值损失和体效应，使该电路在低压下的电源转换性能得到很大的提高.要为 100kΩ 负载提供 1.5V 电源电压，所需最小输入电压为 350mV，转换效率为 22%.在负载为 60kΩ 时，最高可以获得 29.8% 的转换效率.仿真结果表明，新的电路结构比传统的电荷泵具有更优越的性能.

关键词：UHF RFID；电源产生；电荷泵；低压；CMOS

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