A Piecewise Linear Slope Compensation Circuit for DC-DC Converters*

Ye Qiang†, Lai Xinquan, Li Yanming, Yuan Bing, and Chen Fuji

(*Institute of Electronic CAD, Xidian University, Xi'an 710071, China*)

Abstract: To prevent sub-harmonic oscillation and improve the stability and load capacity of the system, a piecewise linear slope compensation circuit is designed. Compared with the traditional design, this circuit provides a compensation signal whose slope varies from different duty cycles at $-40\sim85$℃, and reduces the negative effect of slope compensation on the system's load capacity and transient response. A current mode PWM Boost DC-DC converter employing this slope compensation circuit is implemented in a UMC 0.6μm-BCD process. The results indicate that the circuit works well and effectively, and the load capacity is increased by 20%. The chip area of the piecewise linear slope compensation circuit is 0.01mm^2, which consumes only 8μA quiescent current, and the efficiency ranges up to 93%.

Key words: DC-DC converter; slope compensation; piecewise linear; duty cycle
EEACC: 2570P; 2570A; 2560P
CLC number: TN433 **Document code**: A **Article ID**: 0253-4177(2008)02-0281-07

1 Introduction

In medium and small power DC/DC switched power supplies[1], the peak current-mode controlling technique in constant frequency PWM closed loop feedback controlling system is widely used to achieve better dynamic performance, higher precision, larger gain bandwidth, and protection from transient large current.

For the duty cycle $D>50\%$, there is an inherent open-loop instability and sub-harmonic oscillation in the constant frequency peak current-mode[2] controlling system. If the conventional compensation that is stable under all duty cycles including the maximum di/dt (the worst condition) promised with the constant compensation rate is used, then it will lead to a large slope compensation and damage the transient response characteristic and peak inductor current of the switched power supply. Especially in the unload conditions, the excessive compensation may make the peak current-mode control change into the voltage-mode control, which is unexpected. Therefore, new circuits are required that can produce a compensation rate that varies in different duty cycles to solve these issues. In this paper, a piecewise linear slope compensation is introduced to prevent sub-harmonic oscillation and stabilize the constant frequency configuration[2,3].

The design we propose can decrease the negative effects of the slope compensation to system's load capacity. The duty cycle is divided into three parts, and, in each part, there is a linear compensation signal, which achieves a large peak current and the system's load capacity, and is stable under high duty cycle. The design is suitable to boost DC/DC converters as well as buck DC/DC converters by adjusting the feedback voltage.

2 Principle of slope compensation

Figure 1 shows the principle of slope compensation[4], where m, m_1, and $m_2>0$, and ΔI_0 is a little distortion.

From Fig.1, we have:

$$\Delta I_1 = -\Delta I_0 \times \frac{m_2 - m}{m_1 + m} \tag{1}$$

It is evident that the condition of the system is stable, which satisfies:

$$\frac{m_2 - m}{m_1 + m} < 1 \tag{2}$$

Moreover,

$$Dm_1 = (1 - D)m_2 \tag{3}$$

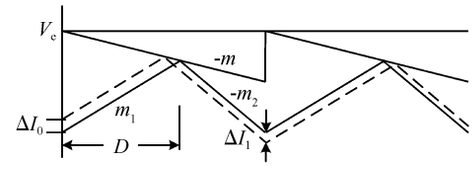

Fig.1 Slope compensation

* Project supported by the Innovation Foundation for Applied Materials of Xi'an (No. XA-AM-200504)
† Corresponding author. Email: yeqiang4213@126.com
Received 6 August 2007, revised manuscript received 25 September 2007

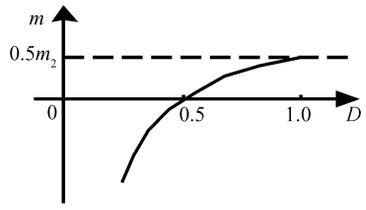

Fig. 2 Slope of compensation versus duty cycle

Thus, from Eqs. (2) and (3), we have

$$m > \frac{2D-1}{2D}m_2 = \left(1-\frac{1}{2D}\right)m_2 \tag{4}$$

Figure 2 shows the function of compensation rate of the duty cycle according to Eq. (4), where m_2 satisfies:

$$m_2 = \left(\frac{\mathrm{d}i}{\mathrm{d}t}\right)_{\max} = \left(\frac{V_{\mathrm{OUT}} - V_{\mathrm{DD}}}{L}\right)_{\max} \tag{5}$$

m_2 is the maximum falling slope of the inductor current, which is determined by the maximum output voltage and minimum inductance. The compensation rate m is proportional to every increase of duty cycle D. For $D = 100\%$, i.e., $m > 0.5m_2$, the system is stable under all conditions[5,6].

3 Circuit design

3.1 Piecewise linear slope compensation design

Figure 3 presents the boost DC/DC block diagram, which consists of such blocks as reference, oscillator, start up and fault control (including soft-start, under-voltage lock, over-current protection, over-temperature protection and over-voltage protection), error amplifier, PWM comparator, and driving circuit[9]. The reference block can provide five kinds of voltages, which are 1.2, 0.8, 0.35, 0.3, and 0.15V. The chip has a peak current threshold of 3A and an oscillation frequency of 1MHz. The under voltage lock block acts when the power supply is lower than 2.0V and makes the chip cut down to prevent unstable operation. The slope compensation block can produce a slope compensation signal. This signal will be added to the inductor current sampling signal, which will be further compared with the signal produced by the error amplifier to secure the inductor current peak testing signal.

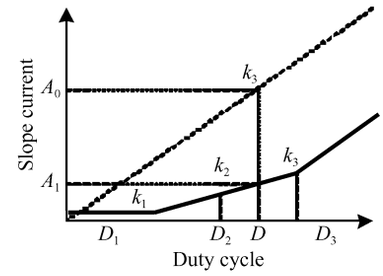

Fig. 4 Current of slope compensation

For the whole chip, the duty cycle can be divided into three parts to make piecewise linear compensation. By Eq. (4), for $D < 50\%$, the system is stable without slope compensation (i.e., $m = 0$). In addition, considering a certain margin, a slope compensation signal is added to the inductor current sampling signal when the duty cycle is larger than 30%. Since the slope m is proportional to the increase of the duty cycle, the compensating slope is determined by the maximum duty cycle in its own part. Hence, the compensation slope can be inferred from Eq. (4) at the maximum duty cycle. Therefore, we can obtain the current of the piecewise linear compensation denoted by the solid line shown in Fig. 4.

If the constant slope compensation is used, the compensation slope m must make the system stable under the worst conditions. Provided the maximum compensation slope is k_3, the current of slope compensation is the dotted line shown in Fig. 4.

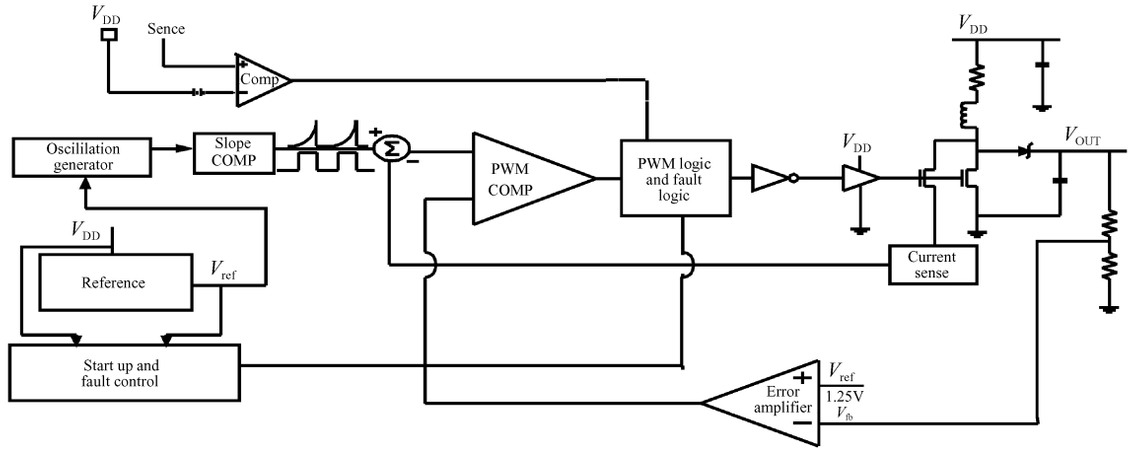

Fig. 3 Function block diagram of boost DC-DC converter

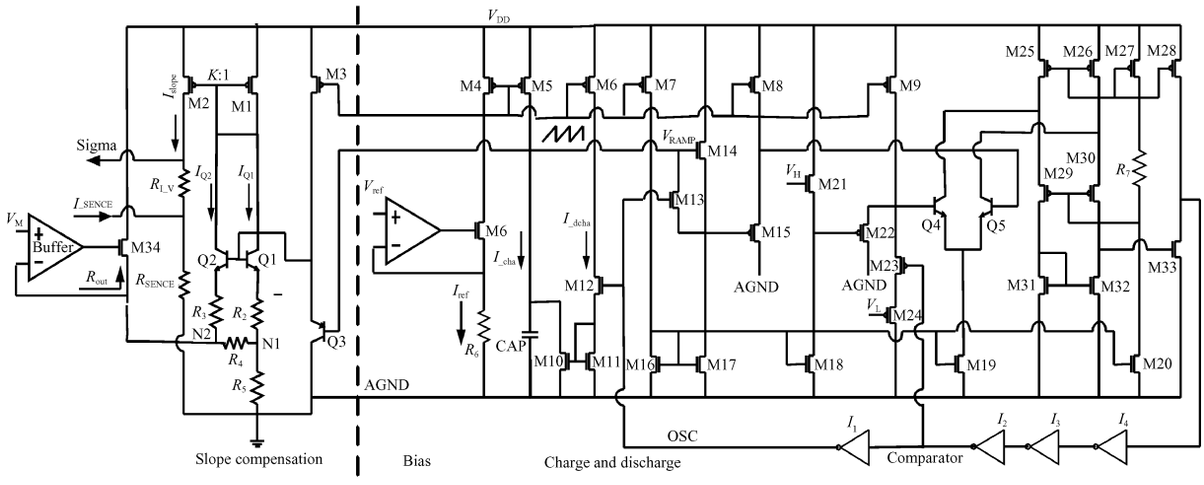

Fig. 5　Circuit of slope compensation

When the duty cycle equals D, the system is stable under both the conditions (see Fig. 4). Comparing the two lines, we find that the slope current amplitude is A_0 with constant slope compensation and A_1 with piecewise linear compensation. The difference $\Delta A = A_0 - A_1$ is the excessive current range, which makes the transient response of the system worse, degrades the inductor peak current, and reduces the load capacity. Thus, piecewise linear compensation can determine the current amplitude in terms of the duty cycle and improve the system performance.

3.2　Realization of piecewise linear slope compensation circuit

The piecewise linear slope compensation signal is produced by the oscillator[7,8] and the piecewise linear function circuit in the slope compensation block, as shown in Fig. 5. The left side of the dotted line is the slope current generation circuit and the right oscillator, which can produce a chip clock signal of 1MHz.

We make a slope transformation and an I-V transformation to the sawtooth wave signal V_{RAMP} from the oscillator to obtain the slope compensation current. The slope compensation of the circuit can be captured by the piecewise linear current. The improved slope compensation technique can complete the current loop compensation much better and degrade the effect of the compensation current on the system peak current targets. The oscillator in Fig. 5 is composed of four parts: the bias current generation circuit, the folded cascade comparator, the charging and discharging circuit, and the control logic. V_{ref} is the reference produced by the reference block, and V_H and V_L are parts of V_{ref}. When the capacitor CAP begins charging, the control logic turns M22 off. When the capacitor voltage V_{CAP} is charged to V_H, the output OSC of the comparator is high "1", which turns M12 on. When the capacitor CAP discharges to V_L, and the output of the comparator is low "0", then M12 is off and the capacitor is charged again. So, this circulation provides a sawtooth signal V_{RAMP}. The frequency of the clock signal produced by OSC is 1MHz. The current flowing through Q1 and Q2 is I_{Q1} and I_{Q2}, respectively. $(W/L)_{M1} : (W/L)_{M2} = 1 : K$.

By charging and discharging to the capacitor, the V_{RAMP} varies from V_L to V_H. $F(Q1)$ and $F(Q2)$ are functions of Q1 and Q2 when they turn on individually.

$$F(Q1) = V_{RAMP} + V_{BEQ3} - V_{BEQ1} - I_{Q1}R_2 - V_{N1} \tag{6}$$

$$F(Q2) = V_{RAMP} + V_{BEQ3} - V_{BEQ2} - I_{Q2}R_3 - V_{N2} \tag{7}$$

According to the iterative theorem, the voltages of N1 and N2 are expressed as:

$$V_{N1} = V_M \frac{R_4}{R_4 + R_5} \tag{8}$$

$$V_{N2} = V_M \tag{9}$$

For $F(Q1) < 0$ and $F(Q2) < 0$, both Q1 and Q2 are off. Here, the voltage of N1 is V_{N1} and N2 is V_{N2} and $V_L \leqslant V_{RAMP} < V_H$. The duty cycle of the OSC signal is D_{OSC}. We divided the V_{RAMP} signal into three parts, which are $[V_L, V_L + \Delta V_1]$, $[V_L + \Delta V_1, V_L + \Delta V_2]$ and $[V_L + \Delta V_2, V_H]$. When $V_{RAMP} = V_L + \Delta V_1$, the duty cycle of corresponding system is as follows:

$$\begin{aligned} D_1 &\approx D_{OSC} + \frac{\Delta V_1}{V_H - V_L}(1 - D_{OSC}) \\ &= D_{OSC} + \frac{V_M R_4 (1 - D_{OSC})}{(R_4 + R_5)(V_H - V_L)} \end{aligned} \tag{10}$$

During the first part of the duty cycle, there is no slope compensation and the slope current is zero. In the clock cycle n:

$$I_{slope1}[nT, nT + D_1 T] = 0, \quad m_{slope1} = 0 \tag{11}$$

By the current loop stability principle, it will be unstable when the duty cycle is larger than 50%. But, in order to have a certain margin, the slope compensation is added when $D_1 > 30\%$ in the design.

For $F(Q1) > 0$ and $F(Q2) < 0$, Q1 is on while Q2 is off. It enters the second part $D_1 \sim D_2$, that is, $V_L + \Delta V_1 \leqslant V_{RAMP} < V_L + \Delta V_2$. Under this condition, the slope current I_{slope} is provided by Q1 and equals KI_{Q1}. By the iterative theorem, the voltage of N1 and N2 are expressed as follows:

$$V_{N1} = V_M \frac{R_4}{R_4 + R_5} + (V_{RAMP} + V_{BEQ3} - V_{BEQ1}) \frac{R_5 /\!/ (R_4 + R_{OUT})}{R_5 /\!/ (R_4 + R_{OUT}) + R_2} \approx V_M \frac{R_4}{R_4 + R_5} + V_{RAMP} \frac{R_5 /\!/ (R_4 + R_{OUT})}{R_5 /\!/ (R_4 + R_{OUT}) + R_2} \quad (12)$$

$$V_{N2} = V_M \quad (13)$$

Thus, for $V_{RAMP} = V_L + \Delta V_2$, the duty cycle D_2 of corresponding system is:

$$D_2 \approx D_{OSC} + \frac{\Delta V_2}{V_H - V_L}(1 - D_{OSC}) = D_{OSC} + \frac{V_M(1 - D_{OSC})}{V_H - V_L} \quad (14)$$

$$I_{slope2}[nT, nT + D_2 T]_{Q_1} = K \frac{V_{RAMP}(nT + D_2 T)}{R_2 + R_5 /\!/ (R_4 + R_{OUT})} \approx K \frac{V_L(R_4 + R_5) + V_M R_4}{R_2(R_4 + R_5)} \quad (15)$$

$$m_{slope2} = \frac{m_{VRAMP}}{R_2 + R_5 /\!/ (R_4 + R_{OUT})} \approx K \frac{V_L(R_4 + R_5) + V_M R_4}{R_2(R_4 + R_5)(D_2 - D_1)T} \quad (16)$$

For $F(Q1) > 0$ and $F(Q2) > 0$, both Q1 and Q2 are on. It enters the third part $D_2 \sim 100\%$, that is, $V_L + \Delta V_2 \leqslant V_{RAMP} < V_L + \Delta V_H$. Under this condition, the slope current I_{slope} is provided by both Q1 and Q2.

$$I_{slope3}[nT, nT + (1 - D_{OSC})T]_{Q1,Q2} = K\{I_{slope3}[nT, nT + (1 - D_{OSC})T]_{Q1} + I_{slope3}[nT, nT + (1 - D_{OSC1})T]_{Q2}\} = K\left\{\frac{V_{RAMP}[(1 - D_{OSC})] - V_{TH}}{R_3} + \frac{V_{RAMP}[(1 - D_{OSC})]}{R_2 + R_5 /\!/ R_4 + R_{OUT}}\right\} \approx K\left[\frac{V_H - V_M}{R3} + \frac{2V_H - V_M}{2R_2}\right] \quad (17)$$

$$m_{slope3} = \frac{m_{VRAMP}}{R_2 + R_5 /\!/ (R_4 + R_{OUT} /\!/ R_3)} + \frac{m_{VRAMP}}{R_3 + R_{OUT} /\!/ (R_4 + R_2 /\!/ R_5)} \approx \frac{K}{(1 - D_2)T}\left[\frac{V_H - V_M}{R_3} + \frac{2V_H - V_M}{2R_2}\right] \quad (18)$$

The slope compensation voltage signal is produced by making the slope current in the terminal SLOPE flow through the resistance R_{LV} and R_{SENCE}, which is the inductor current sampling resistance. Then, the compensation slope and current in the arbitrary period of the ultimate system are as follows:

$$m_n = \begin{cases} m_{slope1} = 0, & 0 < D < D_1 \\ m_{slope2} = K \dfrac{V_L(R_4 + R_5) + V_M R_4}{R_2(R_4 + R_5)(D_2 - D_1)}, & D_1 \leqslant D < D_2 \\ m_{slope3} = \dfrac{K}{1 - D_{OSC} - D_2}\left[\dfrac{V_H - V_M}{R_3} - \dfrac{2V_H - V_M}{2R_2}\right], & D_2 \leqslant D < 100\% \end{cases} \quad (19)$$

$$I_{slope}[nT, nT + t] = \begin{cases} 0, & nT < t < nT + D_1 T \\ m_{slope2}[t - (n + D_1)T], & nT + D_1 T \leqslant t < nT + D_2 T \\ m_{slope3}[t - (n + D_2)T], & nT + D_2 T \leqslant t < 100\% \end{cases} \quad (20)$$

$$D_1 = D_{OSC} + \frac{V_M R_4(1 - D_{OSC})}{(R_4 + R_5)(V_H - V_L)}$$

$$D_2 = D_{OSC} + \frac{V_M(1 - D_{OSC})}{(V_H - V_L)}$$

Figure 6 is the equivalent configuration of the slope compensation circuit, where the feedback voltage V_{fb} is compared to the reference voltage V_{ref} to obtain the differential amplified signal $V_{\_EA}$. The inductor current peak sampling signal is added to the slope signal to get the signal V_{sigma}. Then, the peak current monitoring signal is found by comparing $V_{\_EA}$ and V_{sigma} in order to monitor each periodic signal. Given the peak value of the inductor current I_{SW}, the on resistance of the main switch transistor R_{DSON}, and the limitation of the inductor current I_{LIM} when the inductor current reaches the peak value, we have:

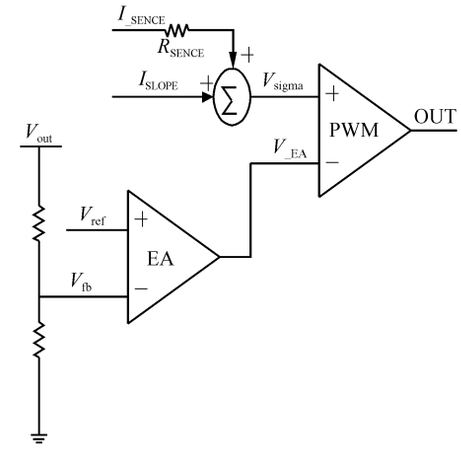

Fig. 6 Function block diagram of slope compensation

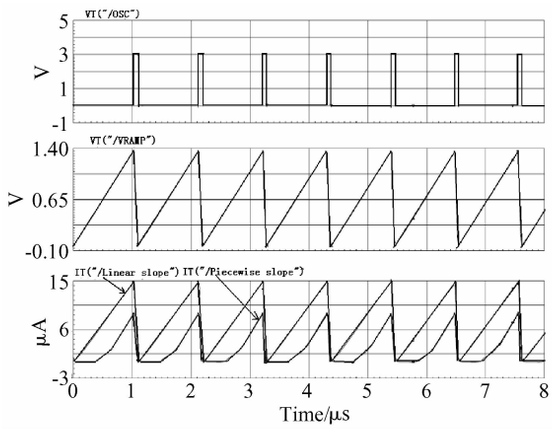

Fig. 7　Linear versus piecewise linear slope current

$$V_{\_EA} = V_{\text{sigma}} = I_{\text{SW}} R_{\text{DSON}} + m_{\text{slope}} DT(R_{I\_V} + R_{\text{SENSE}}),$$
$$0 \leqslant I_{\text{SW}} \leqslant I_{\text{LIM}} \tag{21}$$

The maximum load current of the Boost DC-DC is:

$$I_{\text{OMAX}} = \left(I_{\text{LIM}} - \frac{\Delta I_{\text{L}}}{2}\right)\frac{V_{\text{DD}}}{V_{\text{OUT}}},$$
$$\Delta I_{\text{L}} = \frac{V_{\text{DD}}}{L} \times \frac{D}{f_{\text{s}}}, D = \frac{V_{\text{OUT}} - V_{\text{DD}}}{V_{\text{OUT}}} \tag{22}$$

From Eq. (21), we can see that when $V_{\_EA}$ remains constant, the greater $m_{\text{slope}}(I_{\text{slope}})$ is, the less I_{SW} (the maximum I_{SW} equals I_{LIM}) is. In order to guarantee current loop stability, the piecewise linear slope compensation greatly reduced the negative effects on the system's load capacity from Eqs. (21) and (22). The simulation results are shown in Fig. 7.

4　Experimental results

4.1　Entire circuit simulation results

Based on the UMC 0.6μm-BCD process, the circuit is simulated using H-spice. Figure 7 shows the simulation results, which indicate better transient characteristics of the piecewise linear slope compensation current. When the duty cycle is D and the system is stable, the current of piecewise linear slope compensation is less than that of linear slope compensation. We can derive that the adoption of piecewise linear slope compensation degrades the effect of the peak value of the inductor current greatly and raises the load capacity by 20% from Eqs. (21) and (22) (see Table 1).

The value of the slope current is calculated at different duty cycles according to Eqs. (15) and (16). Table 1 shows the electrical characteristics of the chip with the proposed piecewise slope compensation circuit, which gives the slope current value in the three duty cycle parts at −40, 25, and 85℃ respectively. Figure 8 is the current slope of compensation under the duty cycle between 0 and $D_{\text{MAX}} < 100\%$ and at temperature between −40 and 85℃.

Table 1　Electrical characteristics of the chip with the proposed piecewise slope compensation circuit

Power supply/V	2.5	3.6	5.5
Frequency/MHz	1	1	1
Peak current/A	1.5	2.1	3
Efficiency/%	90	92	93
R_{DSON}/Ω	0.18	0.16	0.14
D	Slope (A/S)		
Temp	<30%	30%～60%	>60%
−40℃	0	4.29	9.63
25℃	0	5.32	11.2
85℃	0	6.08	11.9
$V_{\text{DD}} = 5\text{V}$, $V_{\text{OUT}} = 9\text{V}$	Linear slope		Piecewise linear slope
I_{OMAX}	860mA		1036mA

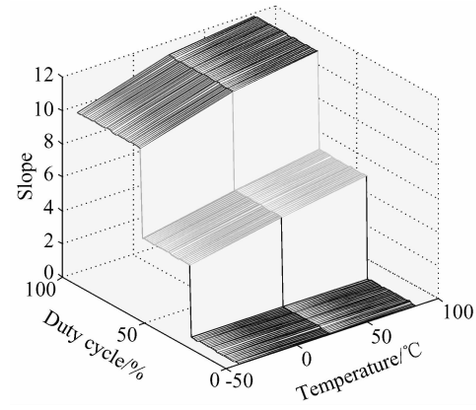

Fig. 8　Current slope of compensation versus duty cycle at different temperatures

4.2　Testing results and layout

To test and verify the chip, the transient response is tested taking the output wave filtering capacitor of 47μF and the 300mA square load current, whose rising and falling time are 1μs. We find that the output voltage pulse is in the range of 100mV at the terminal V_{OUT} and there is no ringing. Figures 9 and 10 show the testing results. The testing conditions in Fig. 9 are

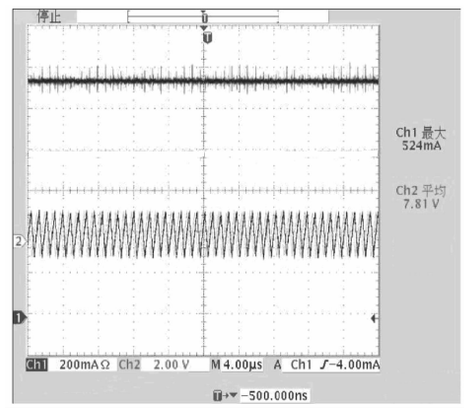

Fig. 9　Output and inductor current of DC-DC converter

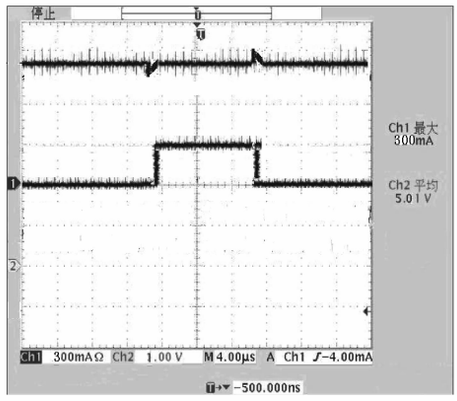

Fig. 10 Experimental results-output of load response

$V_{DD}=3V$ and $V_{OUT}=7.81V$ (V_{OUT} can reach the design value of 8V by trimming) and in Fig. 10 are $V_{DD}=2.5V$, $V_{OUT}=5V$ with load current skipping from 0 to 300mA. The results show that the piecewise linear slope compensation diminishes the negative effects of slope compensation on load capacity and the transient response of the system. Therefore, while satisfying system stability, the piecewise linear slope compensation improved the load transient response characteristics and load capacity.

Figure 11 is the boost DC-DC layout of the chip with the proposed piecewise linear slope compensation circuit. It is the piecewise linear slope compensation circuit within the block, whose area is $0.01mm^2$ and the quiescent current is only $8\mu A$.

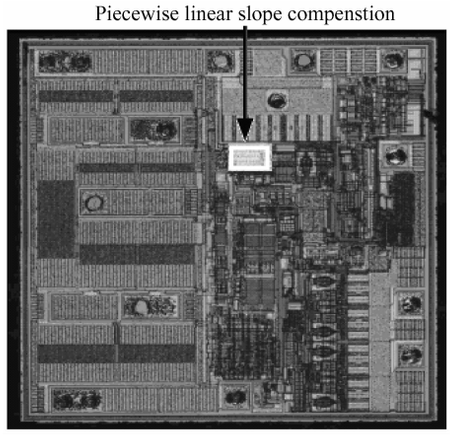

Fig. 11 Layout of the chip with the proposed piecewise slope compensation circuit

5 Conclusion

Based on the analyses of the slope compensation principle, a piecewise linear slope compensation circuit is designed. It can produce a piecewise linear slope compensation signal by employing the oscillator and piecewise linear function circuit in the design and layout. The test results show that, while system stability is satisfied, the circuit has a better transient response characteristic and load capacity, and realizes the piecewise linear slope compensation according to different duty cycles accurately. The proposed design is suitable for the current-mode boost DC/DC converters of constant frequency as well as buck DC/DC converters by adjusting the feedback voltage.

References

[1] Hua Wei. Study on five PWM feedback control modes of SMPS for telecommunication. Telecom Power Technologies, 2001, 18(2):8 (in Chinese) [华伟. 通信开关电源的五种 PWM 反馈控制模式研究. 通信电源技术, 2001, 18(2):8]

[2] Wang Hongyi, Lai Xinquan, Li Yushan, et al. Reducing the slope compensation effect on the load capacity of DC-DC converters. Chinese Journal of Semiconductors, 2006, 27(8): 1484 (in Chinese) [王红义, 来新泉, 李玉山, 等. 减小 DC-DC 中斜波补偿对带载能力的影响. 半导体学报, 2006, 27(8): 1484]

[3] Ridley R. A more accurate current mode control model. http://focus.ti.com/lit/ml/slup122/slup122.pdf

[4] Tse C K, Lai Y M, Chow M H L, et al. Control of bifurcation in current-programmed DC/DC converters: an alternative viewpoint of ramp compensation. International Conference on Industrial Electronics, Control and Instrumentation, Nagoya, Japan, 2000: 2413

[5] Redl R, Novak I. Instabilities in current-mode controlled switching voltage regulators. Power Electronics Specialists Conference, Boulder, CO, 1981: 178

[6] http://focus.ti.com/lit/an/slualol/slualol.pdf

[7] Razavi B. Design of analog CMOS integrated circuits. Translated by Chen Guican, Cheng Jun, Zhang Ruizhi, et al. Xi'an: Xi'an Jiaotong University Press, 2003: 391 (in Chinese) [毕查德·拉扎维. 模拟 CMOS 集成电路设计. 陈贵灿, 程军, 张瑞智, 等译. 西安: 西安交通大学出版社, 2003: 391]

[8] Gregorian R. Introduction to CMOS op-amp and comparators. New York: John Wiley & Sons Inc, 1999

[9] Ye Qiang, Lai Xinquan, Dai Guoding, et al. Novel driver for class-D audio power amplifier. Chinese Journal of Semiconductors, 2007, 28(9): 1477 (in Chinese) [叶强, 来新泉, 代国定, 等. 一种新颖的 D 类音频功率放大器电路. 半导体学报, 2007, 28(9): 1477]

一种 DC-DC 全区间分段线性斜坡补偿电路设计*

叶　强†　来新泉　李演明　袁　冰　陈富吉

（西安电子科技大学电路 CAD 所，西安　710071）

摘要：为了防止亚谐波振荡以及提高系统的稳定性和带载能力，设计了一种全区间分段线性斜坡补偿电路.与传统的设计方法相比，该电路在－40～85℃下提供的补偿信号在不同的占空比区间内具有不同的斜率，对三个占空比区间进行分段线性斜坡补偿，有效减小了斜坡补偿对系统带载能力、瞬态响应的负面影响，极大地改善了系统的稳定性和带载能力.采用此电路的一款电流模 PWM 升压型 DC-DC 已在 UMC 0.6μm-BCD 工艺线投片，测试结果证明分段线性斜坡补偿电路性能良好，带载能力提高了 20%.分段线性斜坡补偿电路芯片面积为 0.01mm^2，静态电流消耗仅为 8μA，芯片效率高达 93%.

关键词：DC-DC 转换器；斜坡补偿；分段线性；占空比

EEACC：2570P；2570A；2560P

中图分类号：TN433　　**文献标识码**：A　　**文章编号**：0253-4177(2008)02-0281-07

* 西安应用材料创新基金资助项目（批准号：XA-AM-200504）

† 通信作者.Email：yeqiang4213@126.com

2007-08-06 收到，2007-09-25 定稿