第 29 卷 第 3 期
2008 年 3 月

半 导 体 学 报
JOURNAL OF SEMICONDUCTORS

Vol. 29 No. 3
Mar., 2008

A 10GHz LC Voltage-Controlled Oscillator in 0.25μm CMOS

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Abstract: A monolithic 10GHz LC voltage-controlled oscillator (VCO) is implemented in standard 0.25μm CMOS technology. The VCO adopts an optimized symmetric circular inductor with center-tap, an accumulation-mode MOS (A-MOS) varactor in series with a passive metal-isolator-metal capacitor (MIM-CAP) and a tail current source with an LC filter to operate with high-frequency and low-noise resulting in − 103.2dBc/Hz at 1MHz offset from carrier frequency of 10.2GHz and approximately 11.5% tuning range. With a 3.3V supply voltage, the core circuit consumes 9.9mW. The chip area is 0.67mm×0.58mm.

Key words: VCO; LC oscillator; CMOS technology
EEACC: 2560
CLC number: TN772 **Document code**: A **Article ID**: 0253-4177(2008)03-0484-06

1 Introduction

With the rapid development of CMOS technology, it is possible to realize transceivers with low-cost CMOS technology for high bit rate transmission systems. A high performance VCO is the critical component of these transceivers, usually used in clock and data recovery circuits. Compared with relaxation oscillators and ring oscillators, LC-tuned oscillators can offer lower phase noise and improved frequency stability, which are important for communication systems. Such VCOs have been implemented in 0.25μm CMOS with modified substrate[1], 0.18μm CMOS[2], 0.13μm CMOS,[3] and 0.13μm CMOS with only simulation results[4]. The VCO proposed in this paper has been implemented in standard 5-metal 0.25μm CMOS technology, focusing on the optimization of the high-Q inductor, the high-Q varactor, and the low noise tail current source to achieve low phase noise performance.

2 Circuit design

2.1 Topology

The presented VCO has a topology of an nMOS cross-coupling differential pair, an nMOS tail current source, and an LC-tank together with an nMOS differential output buffer for measurement. The detailed circuit configuration is shown in Fig. 1. All-nMOS structures, including two cross-coupled transistors, were chosen instead of the complementary structures with four transistors presented in Refs. [2,5], which yields a larger parasitic capacitor and decreases the tuning range and operating frequency. The structure shown in Fig. 1 is suitable for low voltage operation.

Compared with traditional nMOS cross-coupled LC-VCO, R_1 is introduced in Fig. 1 to reduce the DC voltage drop across the channels of M1 and M2 with the consequence of weaker velocity saturation and a smaller γ[5]. Moreover, this configuration can weaken the cross-coupled transistors' body effect and improve the waveform symmetry slightly. To reduce phase noise around carrier, the Q-enhanced varactor is presented as well as an optimized tail current source with an LC filter. The details will be described in the following sections.

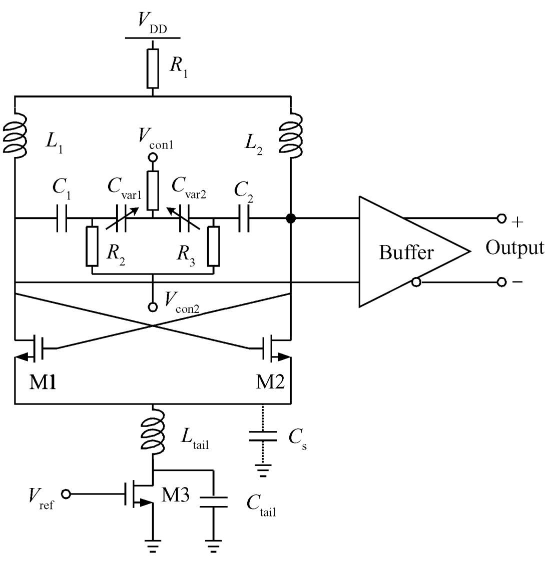

Fig. 1 Schematic of the VCO

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Received 11 August 2007, revised manuscript received 19 October 2007

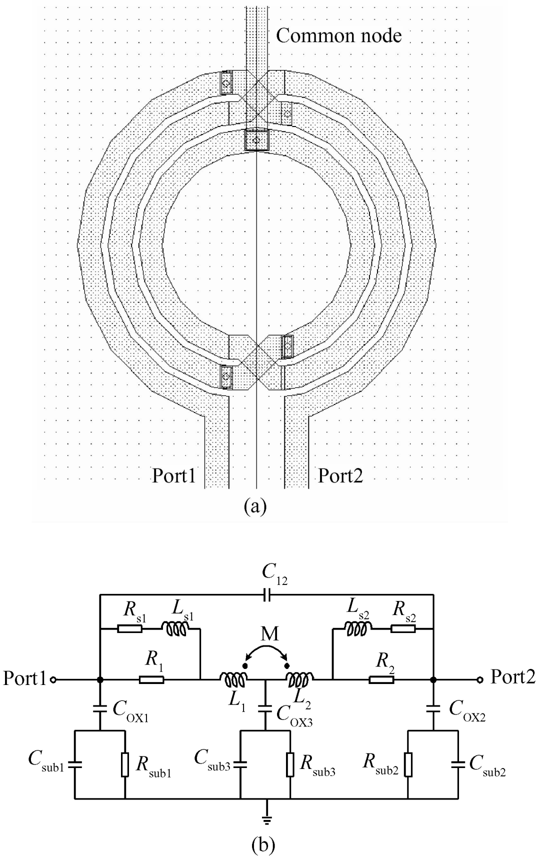

Fig.2 (a) Layout of the symmetric inductor with center tap; (b) Lumped RLC equivalent circuit

2.2 Inductor

Due to a lack of an inductor operating up to 10GHz in the process design kits, a symmetric inductor with center-tap, whose self-resonant frequency is $>$10GHz, has been optimized to meet this requirement. Since polygon spirals with more than four sides have an improvement in Q-factor up to approximately 10% over square ones[6], especially at high frequency, it is an advantage to draw the inductor to be circular, as shown in Fig. 2 (a). The symmetric circular inductor has an optimum geometry of 10μm metal width, 3μm spacing, an 80μm hollow diameter, and 1.5μm metal thickness.

The fully symmetric spiral inductor is designed for the VCO of Fig. 1 with a differential structure. Unlike the traditional differential VCO using a pair of asymmetric inductors spaced far enough to limit unwanted coupling, the presented VCO takes a single coil to realize two symmetric inductors, which occupies smaller die area. When driven differentially, the current flows in the same direction along each adjacent conducting strip. Consequently, the whole magnetic field is reinforced and the overall inductance is increased with the same die area consumption. This is called mutual inductance. In addition, differentially excited inductors are less affected by substrate parasitics, resulting in higher Q-factors and higher self-resonant frequencies than their single-ended equivalents[7].

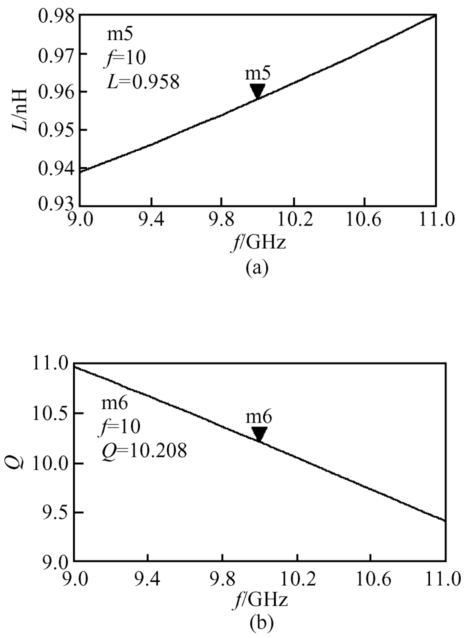

Fig.3 Simulated equivalent inductance (a) and Q-factor half of the symmetric inductor (b)

In order to work with other devices, a compact and accurate Spice model should be extracted from the inductor's layout. First, two-port S-parameters are extracted from the layout with the aid of a 2.5-dimensional electromagnetic simulator of Agilent's ADS-momentum. Then, a proper lumped RLC equivalent circuit, shown in Fig. 2 (b), is selected to fit the S-parameters. Finally, optimum parameters of the equivalent circuit are achieved to fit the two-port S-parameters.

As shown in Figs. 3 (a) and 3 (b), the simulated equivalent inductance and Q-factor of the half of the symmetric inductor excited differentially are 0.96nH and 10.2, respectively.

2.3 Varactor

A MOS varactor working in accumulation mode, called an A-MOS varactor, has a larger tuning range, more compact geometry, and a somewhat higher Q-factor than other types of MOS varactors[8,9], such as B≡D≡S MOS varactors and inversion-MOS (I-MOS) varactors.

Benefiting from the rapid progress of the MOS technology, the model of such a varactor is available in a standard 0.25μm CMOS technology provided by TSMC. Unfortunately, its Q-factor drops quickly when operating at high frequency. At 10GHz, the simulated capacitor value and Q-factor curve versus tuning voltage of this A-MOS varactor are plotted in

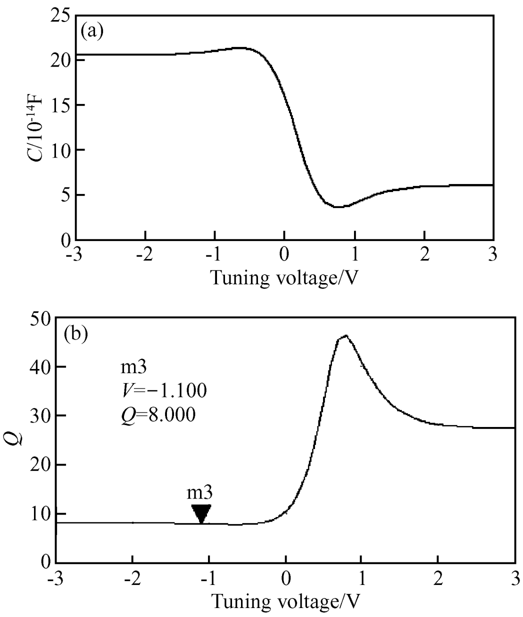

Fig. 4 Simulated A-MOS varactor's capacitor value (a) and Q-factor curve versus tuning voltage (b)

Figs. 4 (a) and 4 (b). It shows a poor Q value, below 10 in some cases. To overcome the Q-factor drop at high frequency, the varactor in the LC-tank is connected in series with MIM-CAP possessing high self-resonant frequency and a large Q-factor, as shown in Fig. 1. Such a configuration can impair the Q-factor dropping trend effectively. The cost is the simultaneous attenuation of the voltage-dependent capacitor, or the tuning range in other words. The improved structure's tuning characteristics presented in Figs. 5 (a) and 5 (b) proves this prediction.

The voltage-dependent capacitor of LC-tank in VCO can convert the low frequency amplitude noise

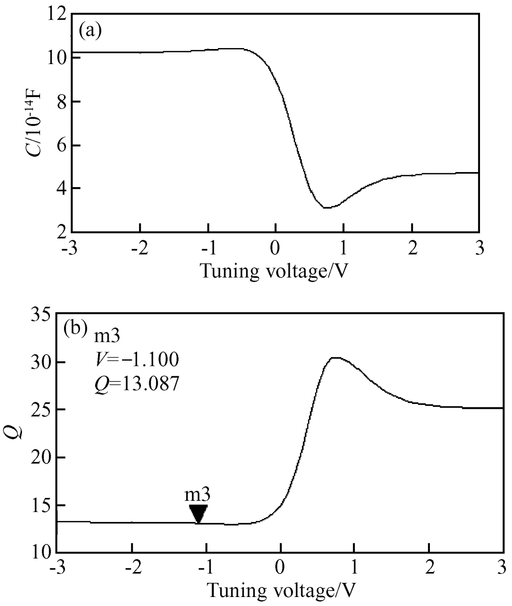

Fig. 5 Improved A-MOS varactor's capacitor value (a) and Q-factor curve versus tuning voltage (b)

around oscillation frequency into phase noise. Such low-frequency amplitude noise comes primarily from the tail current source, $1/f$ noise for example. The most attractive aspect is that the proposed varactor configuration above can prevent the low frequency noise from passing across the A-MOS varactor, benefiting from a fixed small MIM-CAP in series with the varactor. An array of switchable fixed binary-weighted capacitors is also reported elsewhere to suppress the same effect[10].

Another advantage of the varactor's configuration shown in Fig. 1 is the capability to eliminate the parasitic n-well to p-sub capacitor as long as the n-well is treated as a common node. Also, it is convenient to tune the varactor differentially through V_{con1} and V_{con2} presented in Fig. 1.

2.4 Tail current source

The noise from the tail current source can affect the VCO's phase noise significantly through up-conversion. The noise in the vicinity of f_0 and its odd-order does not influence the phase noise. Otherwise, the noise around $2Nf_0$ has an obvious effect on the phase noise and the low-frequency noise of the tail current source. According to the principle above, a bypass capacitor C_{tail}, shown in Fig. 1, is introduced to shunt M3's high frequency noise around $2Nf_0$ ($N \geqslant 1$) to ground. On the other hand, the C_{tail} degrades the AC impedance of the tail current source, which leads to Q-factor degradation if either M1 or M2 is driven into the triode range[10]. To avoid this degradation, a parasitic inductor L_{tail}, in series with M3, is chosen to resonant at $2f_0$ in parallel with the parasitic capacitor C_s, illustrated in Fig. 1. As a result, the high frequency noise from the tail current, particularly around $2Nf_0$ ($N \geqslant 1$), can be reduced effectively, but not low frequency noise such as $1/f$ noise. However, the performance is satisfactory if the tail current source is with the proper size and the symmetry of the wave is perfect.

2.5 Phase noise prediction

Treated as linear time variant (LTV) system, an oscillator's phase noise can be predicted with transient simulation[11]. With an injected charge 18fC, the simulated impulse sensitivity functions (ISFs) of M1 and M3 are shown in Figs. 6 and 9, respectively. Figures 7 and 8 are the normalized noise modulation function (NMF) and the effective ISF of M1. The simulation is implemented in SmartSpice.

The parameters calculated from the device characteristics and extracted from the simulation results above are listed in Table 1. Based on these parameters,

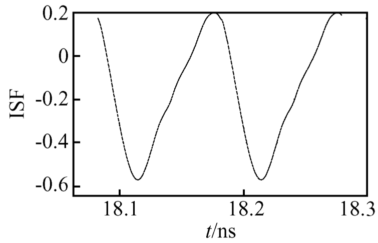

Fig.6 ISF of M1

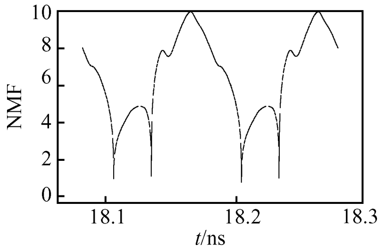

Fig.7 NMF of M1

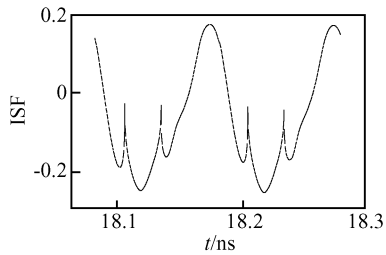

Fig.8 Effective ISF of M1

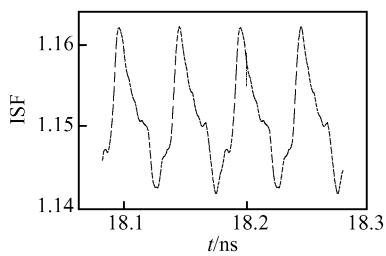

Fig.9 ISF of M3

the VCO's phase noise is predicted in Fig. 10, in which the phase noise values at different frequency offsets are illustrated. In particular, the predicted phase noise $1/f^3$ corner frequency is about 1.2MHz.

3 Measured results

The monolithic LC VCO is fabricated in a TSMC 0.25μm CMOS mixed signal process. Figure 11 shows the photograph of the chip, which occupies an area of

Table 1 Parameters for phase noise prediction

Noise source	$\overline{I_n^2}/\Delta f$ /(A^2/Hz)	γ	ΣC_n^2	C_0^2	$f_{1/f}$/Hz
M1	7.47×10^{-23}	2.5	0.0402	0.0042	1.14×10^{7}
M3	8.68×10^{-23}	2.5	1.32×10^{-6}	1.32×10^{-6}	148.5×10^{3}

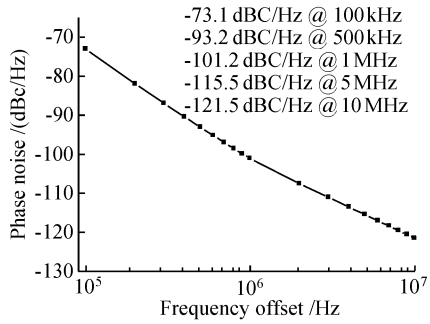

Fig.10 Predicted phase noise

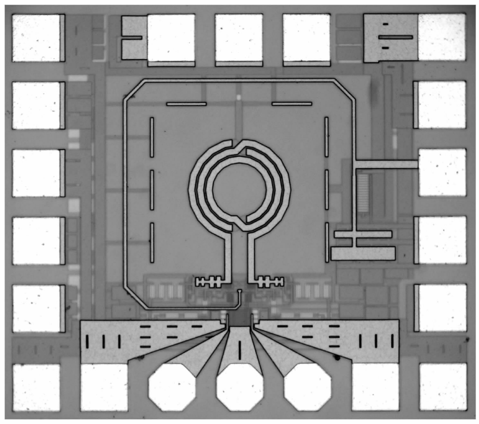

Fig.11 VCO photograph

0.67mm × 0.58mm including output buffer and all test pads. The measured results on the probe station indicate that the circuit consumes 3mA of current with a 3.3V supply, excluding the output buffer.

Figure 12 shows the oscillation frequency of the VCO as the control voltage ($V_{con1} - V_{con2}$) is varied. According to the measured results, a tuning range of approximately 11.5%, from 9.97 to 11.12GHz, is achieved. Figure 13 is the transient waveform of the VCO, whose peak-peak amplitude is 220mV on 50Ω load.

The frequency spectrum, power and phase noise of the VCO's single-end output, measured by an Agilent E4440A spectrum analyzer, are shown in Figs. 14 and 15.

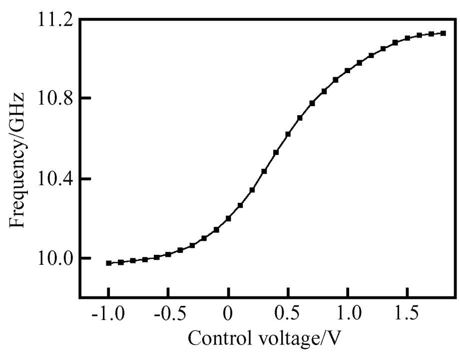

Fig.12 Tuning characteristics

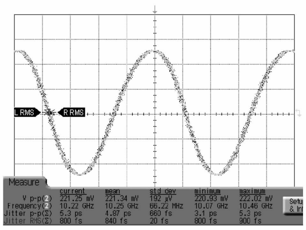

Fig. 13 Transient waveform

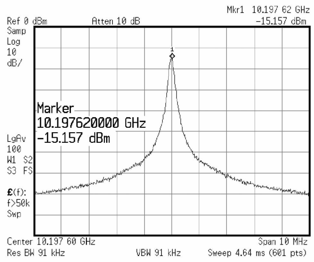

Fig. 14 Frequency spectrum

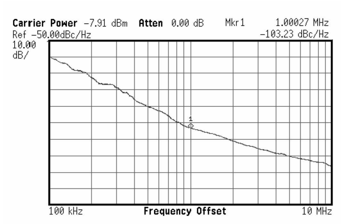

Fig. 15 Phase noise

The phase noise at 1MHz offset from a carrier of 10.2GHz is -103.2dBc/Hz and the figure of merit (FOM) is -173.4dBc/Hz, calculated from the following definition[12]:

$$\mathrm{FOM} = L(f_{\mathrm{offset}}) - 20\lg\left(\frac{f_0}{f_{\mathrm{offset}}}\right) + 10\lg\left(\frac{P}{1\mathrm{mW}}\right)$$

where f_{offset} is the frequency offset, f_0 is the oscillation frequency, $L(f_{\mathrm{offset}})$ is the phase noise at f_{offset}, and P is the power consumption. The VCO presented in this paper is comparable to other 10GHz LC-VCOs published elsewhere and summarized in Table 2.

Table 2 Comparison with published LC-VCOs

Reference	CMOS process	Phase noise /(dBc/Hz)	Tuning range /%	Power consumption /mW	FOM /(dBc/Hz)
[2]	0.18μm	−89@100kHz	11	5.8	−181.4
[3]	0.13μm	−95@1MHz	15	14.4	−163.4
[4]	0.13μm	−99@1MHz	37	3.6	−173.4
[13]	0.18μm	−101@1MHz	4.5	9	−171.5
[14]	0.18μm	−105@1MHz	12	7.2	−176.4
This work	0.25μm	−103.2@1MHz	11.5	9.9	−173.4

4 Conclusion

A monolithic 10GHz LC VCO has been implemented in TSMC 0.25μm CMOS technology. An optimized symmetric inductor, a *Q*-enhanced varactor, and a low noise tail current source are helpful to improve the VCO's performance. The measured results show a tuning range from 9.97 to 11.12GHz and a phase noise of -103.2dBc/Hz at 1MHz offset from 10.2GHz carrier. With a 3.3V supply, the core circuit consumes 3mA of current. Experimental results indicate the possibility of integrating a 10Gb/s clock and data recovery circuit for SONET communication in low-cost 0.25μm CMOS technology.

References

[1] Wang H. A 50GHz VCO in 0.25μm CMOS. IEEE Int Solid-State Circuits Conf, 2001: 372
[2] Jia L, Ma J G, Yeo K S, et al. 9.3～10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance. IEEE Trans Microw Theory Tech, 2004, 52(4): 1273
[3] Li S, Kipnis I, Ismail M. A 10-GHz CMOS quadrature LC-VCO for multirate optical applications. IEEE J Solid-State Circuits, 2003, 38(10): 1626
[4] Mukherjee D, Bhattacharjee J, Laskar J. A differentially-tuned CMOS LC VCO for low-voltage full-rate 10Gb/s CDR circuit. IEEE MTT-S International Microwave Symposium Digest, 2002, 2(6): 707
[5] Hajimiri A, Lee T H. Design issues in CMOS differential LC oscillators. IEEE J Solid-State Circuits, 1999, 34(5): 717
[6] Long J R, Copeland M A. The modeling, characterization, and design of monolithic inductors for silicon RF IC's. IEEE J Solid-State Circuits, 1997, 32(3): 357
[7] Danesh M, Long J R. Differentially driven symmetric microstrip inductors. IEEE Tran Microw Theory Tech, 2002, 50(1): 332
[8] Andreani P, Mattisson S. On the use of MOS varactors in RF VCO's. IEEE J Solid-State Circuits, 2000, 35(6): 905
[9] Bunch R L, Raman S. Large-signal analysis of MOS varactors in CMOS -Gm LC VCOs. IEEE J Solid-State Circuits, 2003, 38(8): 1325
[10] Hegazi E, Sjöland H, Abidi A. A filtering technique to lower oscillator phase noise. IEEE Int Solid-State Circuits Conf, 2001: 364
[11] Hajimiri A, Lee T H. A general theory of phase-noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179
[12] Plouchart J O, Ainspan H, Soyuer M, et al. A fully-monolithic SiGe differential voltage-controlled oscillator for 5GHz wireless applications. IEEE Radio Frequency Integrated Circuits Symposium, 2000, (6): 57
[13] Mostafa A H, El-Gamal M N. A CMOS VCO architecture suitable for sub-1 volt high-frequency (8.7～10GHz) RF applications. International Symposium on Low Power Electronics and Design, 2001, 8: 247
[14] Gu Z, Bartsch B, Thiede A, et al. Fully integrated 10GHz CMOS LC VCOs. 33rd European Microwave Conference, 2003: 583

10GHz 0.25μm CMOS LC 压控振荡器

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摘要： 采用标准 0.25μm CMOS 工艺实现了 10GHz LC 压控振荡器.为了适应高频工作,并实现低相位噪声,该压控振荡器采用了手动优化的带中心抽头的对称电感,将 A-MOS 变容二极管与无源金属-绝缘层-金属电容串联,并采用了带 LC 滤波器的尾电流源.测试结果显示,当振荡频率为 10.2GHz 时,在 1MHz 频偏处相位噪声为 −103.2dBc/Hz,调谐范围为 11.5%.供电电压为 3.3V 时,核心电路功耗为 9.0mW.芯片面积为 0.67mm×0.58mm.

关键词： 压控振荡器；LC 振荡器；CMOS 工艺

EEACC： 2560

中图分类号： TN772　　**文献标识码：** A　　**文章编号：** 0253-4177(2008)03-0484-06

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2007-08-11 收到,2007-10-19 定稿