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Effect of an Asymmetric Doping Channel on Partially Depleted SOI MOSFETs*

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Abstract: Asymmetric doping channel (AC) partially depleted (PD) silicon-on-insulator (SOI) devices are simulated using two-dimensional simulation software. The electrical characteristics such as the output characteristics and the breakdown voltage are studied in detail. Through simulations, it is found that the AC PD SOI device can suppress the floating effects and improve the breakdown characteristics over conventional partially depleted silicon-on-insulator devices. Also compared to the reported AC FD SOI device, the performance variation with device parameters is more predictable and operable in industrial applications. The AC FD SOI device has thinner silicon film, which causes parasitical effects such as coupling effects between the front gate and the back gate and hot electron degradation effects.

Key words: AC PD SOI MOSFETs; output characteristics; breakdown voltage
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1　Introduction

Since the 1970s, silicon-on-insulator (SOI) devices have attracted attention due to their superior performance: radiation hardness, reduction in parasitic capacitances, higher packing density, and latch-up-free operation[1]. There exist two kinds of SOI devices, namely, partially depleted (PD) SOI and fully depleted (FD) SOI according to the ratio between film thickness t_{Si} and vertical depletion width X_d, i.e., $t_{Si} > X_d$ for PD and $t_{Si} < X_d$ for FD.

According to the IBM Corporation reports, the PD SOI device has more advantages in application than the FD SOI device, since the FD SOI device is not manufacturable. Especially in submicron CMOS technology, control of the short channel effect (SCE) is critical. Adopting PD device design allows the use of many of the techniques developed for controlling SCE[2]. There are many other benefits associated with PD SOI: it is very difficult to design a high-threshold voltage (V_T) FD device, because if the film doping is increased in order to raise the V_T, the device is not fully depleted; it must be made thinner, then the V_T decreases and the fabrication of FD SOI becomes more complex[3]. However, the floating body effect becomes one of the barriers for SOI device applications, especially in PD SOI device[4,5]. Pavenello *et al*.[6] reported a new asymmetric-channel (AC) SOI MOSFET in an FD SOI device to suppress the floating body effect, as shown in Fig. 1. The AC SOI MOSFET has an asymmetric concentration profile inside the transistor channel region due to a small modification in the fabrication process of conventional SOI transistors, preserving total compatibility with the currently used SOI CMOS technology. In the AC SOI MOSFET, the channel region is divided into two parts: the first, beside the drain and with a reduced doping concentration, is designated as a low doped region (length L_{LD}). This region behaves as an extension of the drain region for positive values of front gate voltage, reducing the device effective channel length ($L_{eff} = L - L_{LD}$, where L is the mask channel

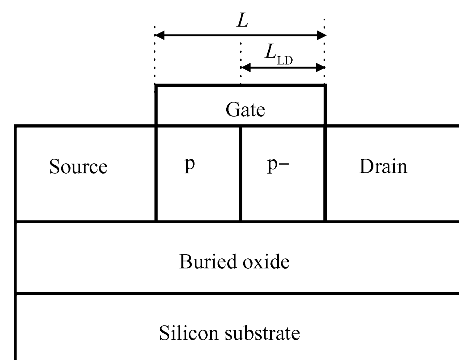

Fig.1　Cross section of the asymmetric channel SOI MOSFET

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Table 1　Parameters of AC PD SOI MOSFETs

Gate oxide thickness	15nm
Silicon film thickness	200nm
Substrate concentration	$1\times10^{15}\mathrm{cm}^{-3}$
Buried oxide thickness	400nm
Gate material	Aluminum

length)[6]. In order to find the impact of this new structure on the PD SOI device, the characteristics of AC partially depleted SOI MOSFETs are simulated in detail by SILVACO ATLAS software[8]. Compared with previous reports of AC FD SOI devices, it is found that the effects of an asymmetric doping channel on PD SOI devices abide by some rules[6], such as that increasing the ratio of L_{LD}/L or reducing the value of N_{LD} can suppress the floating effects and improve the breakdown characteristic monotonously. However, the case is quite different for FD SOI devices [6]. This is because the FD SOI devices have thinner silicon film, which makes the coupling effects between the front gate and back gate outstanding for some L_{LD}/L or N_{LD}. Actually, this is unpredictable for the AC FD SOI application due to its parasitical effects. The floating potential, surface electric field, and electron temperature are studied to confirm the results.

2　Device simulation

Two-dimensional numerical simulation is implemented by SILVACO ATLAS tools. Typical values of the AC PD SOI MOSFETs are listed in Table 1. In order to simulate the device correctly, the Shockley-Read-Hall recombination mechanism, Auger recombination, the CVT mobility model, band gap narrowing, electric field dependent impact ionization mechanism, hot carrier effects, and energy balance conditions are included in the simulation process[8].

2.1　Output characteristics

The analysis of output characteristics with different N_{LD} is shown in Fig. 2. The gate voltage is biased at 3V and the ratio of L_{LD}/L is 0.5. The figure indi-

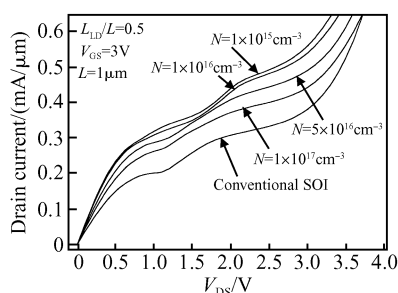

Fig. 2　Output characteristics curves with different N_{LD}

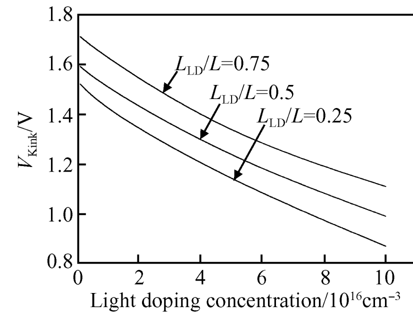

Fig. 3　V_{Kink} versus N_{LD} with different L_{LD}/L ratios

cates that reducing the N_{LD} can suppress the kink effects and improve the device breakdown characteristics. Figure 3 shows the curves of V_{Kink} versus N_{LD} (V_{Kink} is the drain voltage where the kink effect occurs.). This simulation result agrees well with the reports in Ref. [4]. The kink effects caused by the floating body potential are due to the accumulated holes by the injection of the hole current near the drain[4]. The hole concentration near the drain end is reduced at lower N_{LD} near the drain end. Therefore, the number of holes injected into the floating body decreases compared to the higher N_{LD}. Thus, the floating body potential is suppressed with lower N_{LD}.

Figure 4 illustrates the output characteristics with different L_{LD}/L ratios of 0.75, 0.5, and 0.25, with a channel length L of 1μm. Increasing the L_{LD}/L ratio can reduce the kink effects in AC PD SOI MOSFETs, which is different from the AC FD SOI MOSFETs[6,7]. This is because the AC FD SOI MOSFETs have a better coupling between the front gate and the back gate than that in AC PD SOI MOSFETs, and thinner silicon film causes hot electron degradation[9]. The longer L_{LD} can also increase the transistor breakdown voltage. As the L_{LD}/L ratio increases, the total hole concentration, which can be accelerated by the high electric field near the drain end, shows a reduction, as shown in Fig. 5. Figure 5 demonstrates that the length of the hole concentration region near the drain end increases with the L_{LD}/L ratio, although

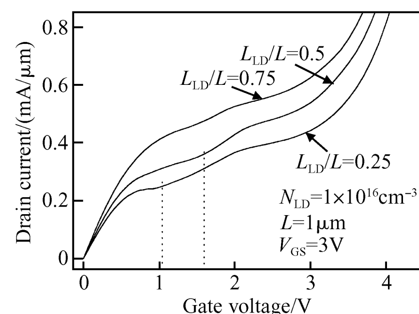

Fig. 4　Output characteristics curves with different L_{LD}/L ratios

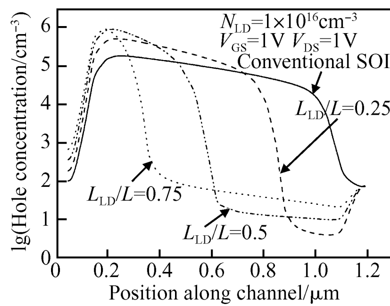

Fig. 5 Surface hole concentration along the channel with different L_{LD}/L ratios

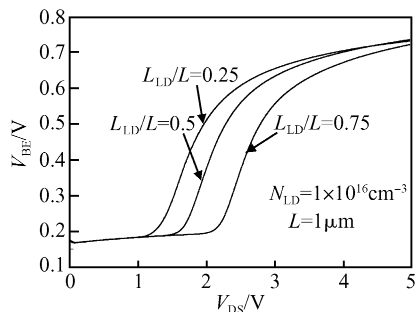

Fig. 6 Floating body potential versus V_{DS} with different L_{LD}/L ratios

the hole concentration with a small L_{LD}/L ratio near drain end is lower than that with a large L_{LD}/L ratio. This will cause the increase in breakdown voltage. Figure 6 presents the floating body potential (V_{BE}) versus the drain-to-source (V_{DS}) with different L_{LD}/L ratios, where the values of V_{BE} are extracted from the simulated AC SOI structure. This figure depicts that a small L_{LD}/L ratio causes the sudden increase of floating potential more easily than a large L_{LD}/L ratio, in accordance with the illustrations in Fig. 4.

Figure 7 shows the longitudinal electric field distribution along the channel with different L_{LD}/L ratios. This simulated result further confirms the conclusion in Fig. 4. The peak electric fields shift towards the source end when the L_{LD}/L ratio becomes large. This peak electric field is related to the impact ionization field and the accelerated electric field. When the

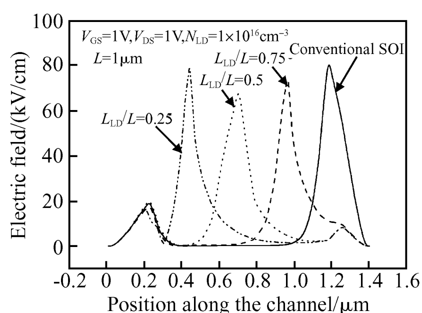

Fig. 7 Longitudinal electric field distribution along the channel with different L_{LD}/L ratios

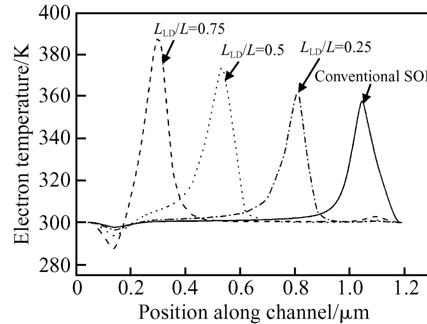

Fig. 8 Surface electron temperature along the channel with different L_{LD}/L ratios

peak electric field shifts towards the source end, the impact ionization field and the accelerated electric field near the drain end will be reduced. Therefore, the floating body effects and breakdown characteristics can be improved, as displayed in Fig. 4. Figure 8 gives the electron temperature along the channel for different L_{LD}/L ratios. The figure demonstrates that the peak values of electron temperature shifts towards the source end, which corresponds to the electric field distribution.

2.2 Breakdown characteristic analysis

From Fig. 2 and Fig. 4, AC PD SOI MOSFETs can suppress the floating effects and improve the breakdown characteristic. The performance for PD SOI devices with certain parameters can be easily forecasted according to our simulation results, compared with that for FD SOI devices. In this subsection, the breakdown characteristic of AC PD SOI MOSFETs is illustrated in detail.

The SOI device breakdown characteristic is related to the floating body structure, namely the parasitic bipolar structure, where the source corresponds to the emitter, the channel to the base, and the drain to the collector. When the drain voltage V_{DS} rises, the holes near the drain end are injected into the floating body region by the high electric field near the drain end. In order to investigate the inherent physical causes of

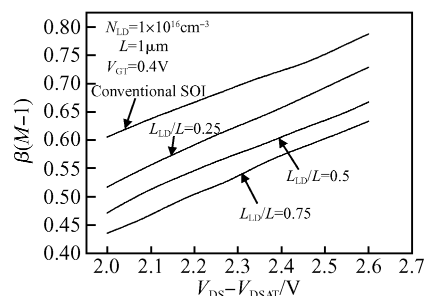

Fig. 9 $\beta(M-1)$ in function of the drain voltage ($V_{DS}-V_{DSAT}$) with different L_{LD}/L ratios

the breakdown characteristic, the factor $\beta(M-1)$ is used[10]. β is the current gain of the parasitic bipolar transistor[11]. M is the multiplication factor due to the high electric field, which is given by[7]:

$$M = \frac{I_\mathrm{I}}{I_\mathrm{DS} - I_\mathrm{I}} + 1 \quad (1)$$

where I_I is the hole current generated by the impact ionization, which can be extracted from the region near the drain end, and I_DS is total current that flows through the channel which involves the impact ionization. The total drain current can be expressed by[10]:

$$I_\mathrm{DS} = \frac{MI_\mathrm{ch}}{1-\beta(M-1)} \quad (2)$$

where I_ch is the MOS channel current, not considering the impact ionization. Following Eq. (2), the device reaches the breakdown voltage when the product $\beta(M-1)$ tends to one. When the value of $\beta(M-1)$ is larger, the breakdown voltage decreases.

Through two-dimensional simulation, it can extract the hole current near the drain end (I_I) generated by impact ionization. The total current I_DS involves the impact ionization mechanism. Therefore, the factor M can be determined according to Eq. (1). With the same simulation, it is possible to extract the current I_ch without the impact ionization mechanism. The value of β can be derived through Eq. (2).

Figure 9 illustrates the value of $\beta(M-1)$ in the function $V_\mathrm{DS} - V_\mathrm{DSAT}$ with different L_LD/L ratios. V_DSAT is the saturation voltage, which is equal to V_GT (V_GT is the difference between the gate voltage and the threshold voltage). All the AC configurations exhibit a smaller $\beta(M-1)$ than the conventional PD SOI MOSFETs, namely, the AC PD SOI MOSFETs can increase the breakdown voltage obviously. Larger ratios of L_LD/L for the AC PD SOI device result in larger breakdown voltages. The result is monotone, and thus more predictable for controlling the processing parameters in industrial application than that for FD SOI devices[6]. The simulation results explain the illustrations in Fig. 4 well.

3 Conclusion

In this work, AC PD SOI MOSFETs are simulated by SILVACO ATLAS tools. The output characteristics of the proposed device are presented with different N_LD and different ratios of L_LD/L. From the simulation, we find that the AC PD SOI MOSFETs can suppress the floating effects and improve the breakdown characteristics, and, further, the performance is more predictable in future industrial applications due to smaller parasitical effects than FD SOI MOSFETs. To some extent, the AC PD SOI MOSFETs are superior to conventional SOI MOSFETs and AC FD SOI MOSFETs.

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部分耗尽 SOI MOSFETs 中沟道的非对称掺杂效应*

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摘要：利用二维模拟软件对部分耗尽 SOI 器件中的非对称掺杂沟道效应进行了模拟.详细地研究了该结构器件的电学性能，如输出特性，击穿特性.通过本文模拟发现部分耗尽 SOI 非对称掺杂沟道相比传统的部分耗尽 SOI，能抑制浮体效应，改善器件的击穿特性.同时跟已有的全耗尽 SOI 非对称掺杂器件相比，部分耗尽器件性能随参数变化，在工业应用上具有可预见性和可操作性.因为全耗尽器件具有非常薄的硅膜，而这将引起如前栅极跟背栅极的耦合效应和热电子退化等寄生效应.

关键词：AC 部分耗尽 SOI MOSFETs；输出特性；击穿电压

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