$1/f^{\gamma}$ Noise Characteristics of an n-MOSFET Under DC Hot Carrier Stress

Liu Yu'an† and Yu Xiaoguang

(*Jinggangshan University, Ji'an 343009, China*)

Abstract: The $1/f^{\gamma}$ noise characteristic parameter Sf^{γ} model in an n-MOSFET under DC hot carrier stress is studied. A method characterizing the MOSFET abilities of an anti-hot carrier with noise parameter Sf^{γ} is presented. The hot carrier degradation effect of n-MOSFET in high-, mid-, and low gate stresses and its $1/f^{\gamma}$ noise feature are studied. Experimental results agree well with the developed model.

Key words: n-MOSFET; hot carrier; $1/f^{\gamma}$ noise
PACC: 7340Q; 5225G
CLC number: TN386.11 **Document code**: A **Article ID**: 0253-4177(2008)07-1263-05

1 Introduction

The increase of integration density needed in system miniaturization requires shrinking MOS device sizes and drastically reducing dimensions. Design and implementation of the recent developments in advanced MOS devices motivated investigations on new characterization techniques to give reliable device parameters and to take care of the physical and electrical induced gate/substrate currents, mainly SILC current and drain-source currents[1]. Previously, we used the ΔV_t and Δg_m character MOS device hot carrier effects based on the charge pumping technique. However, the charge pumping current is in direct proportion to the scale down gate area. With the reduction of device dimensions, it has become so small that it is difficult to measure. In order to overcome these limitations, an improved method is necessary. This method must give precise characteristics of the MOS device hot carrier effect. Developing the method is an important reliability issue. For example, Xu *et al*. researched the $1/f$ noise degradation mechanisms in three different stresses of the MOS device hot carrier effect[2]. But, a model that includes the physical meaning of $1/f$ noise degradation for the MOS device hot carrier effect still has not been developed.

In this paper, we research the $1/f$ noise parameter Sf^{γ} degradation in n-MOSFET under DC hot carrier stress. We perform an experiment for the n-MOSFET hot carrier effect under high-, middle-, and low gate voltage. We develop a method to characterize the MOS device anti-hot carrier effect using the $1/f$ noise parameter Sf^{γ}. We propose a nondestructive measure for n-MOSFET under DC hot carrier stress.

2 Theoretical model

When the MOS device is in DC stress, the energy of the carriers increases and some "lucky electrons" become hot carriers. High energy carriers near the gate oxide interrupt the Si—Si bond; low energy carriers interrupt the Si—H bond or Si—OH bond. They produce several kinds of defects, including oxide traps and deep and shallow energy level interface states. Their energy level is nearly the same as the Fermi energy level. After stress or other influences, an energy level transition occurs. Then, carriers capture or emit in the channel of a MOS device. New defects are produced that result in ΔV_t, Δg_m, and a change of the $1/f$ noise parameters, even device invalidation.

According to the excess noise model of channel resistance fluctuations, the dependency of the current noise of the n-channel devices on frequency, drain-voltage, and gate-voltage can be simply represented by[3]

$$S_V(f, \overline{V_d}, V_g) = \frac{K\,\overline{V_d^2}}{f^{\gamma}(V_g - V_T)^2} \tag{1}$$

where K is the "noise level" of a device. When $\gamma = 1$, the unit of K is V^2. If traps exist in the oxide with uniform energy and space, charge carriers tunnel in and out of these traps with a probability that decreases exponentially with distance into the oxide. The spatial distribution of traps results in a distribution of trap times, and a corresponding frequency spectrum for the $1/f$ noise is:

$$S_V(f, \overline{V_d}, V_g) = \frac{q^2}{(LWC_{ox})^2} \times \frac{\overline{V_d^2}}{f(V_g - V_T)} \times \frac{k_B TLWD_d(E_F)}{\ln(t_{max}/t_{min})} \tag{2}$$

† Corresponding author. Email: danu0012004@163.com
Received 31 August 2007, revised manuscript received 27 January 2008

where C_{ox} is the oxide capacitance per unit area, $D_d(E_F)$ is the defect density per unit energy per unit area at the trap quasi-Fermi level E_F, L and W are the transistor channel length and width, respectively, q is the magnitude of the electronic charge, k_B is the Boltzmann constant, and t_{min} and t_{max} are the minimum and maximum emit or capture times, respectively. Scofield *et al*.[4] found that the emitting time of changing carriers between the oxide traps and channels was 0.3～12μs; Militaru *et al*.[5] found that the capture time of changing carriers between the interface states and the channels was 10～10^4μs. The above spectrum is valid when $1/t_{max} < f < 1/t_{min}$. Equations (1) and (2) show that the model correctly describes the dependencies of the $1/f$ noise on f, $\overline{V_d}$, V_g for our n-channel devices. At a given temperature, only a small fraction of oxide traps, whose energies are within $k_B T$ of the quasi-Fermi level, contribute to the measured $1/f$ noise.

In order to understand the correlation between ΔV_t and the noise level K, we assume that both the hot carrier induced threshold shift V_t and the $1/f$ noise are related to $D_d(E)$. The threshold shift ΔV_t and the number per unit area of hot carrier induced defect charges ΔN_d are simply related by

$$|\Delta V_t| = \frac{q\Delta N_d}{C_{ox}} \tag{3}$$

ΔN_d is proportional to the total number of defects N_d, i.e.,

$$\Delta N_d = \lambda N_d = \int_{E_V}^{E_C} D_d(E)\mathrm{d}E \tag{4}$$

where E_V and E_C are the valence band and conduction band energies of the oxide. The proportionality constant $0<\lambda<1$ increases with the hot carrier damage. If the defects are uniformly distributed in energy, we then have

$$\Delta N_d \approx \lambda E_g D_d \tag{5}$$

where $E_g = E_C - E_V$ is the bandgap of the oxide and D_d is the (constant) defect density. Substituting Eqs. (3) and (5) into Eq. (2) and letting $C_{ox} = \varepsilon_{ox}/t_{ox}$, where t_{ox} is the thickness and ε_{ox} is the dielectric constant of the gate oxide, we have

$$S_V(f, \overline{V_d}, V_g) = \frac{qk_B T t_{ox} |\Delta V_d|}{\lambda\varepsilon_{ox} E_g LW \ln(t_{max}/t_{min})} \times \frac{\overline{V_d^2}}{f(V_g - V_T)^2} \tag{6}$$

Comparing Eqs. (6) and (1), we see that the above assumptions lead to the conclusion that the noise level K and defect threshold shift ΔV_t are related by

$$K \approx \frac{qk_B T t_{ox}}{\lambda\varepsilon_{ox} E_g LW \ln(t_{max}/t_{min})} |\Delta V_t| \tag{7}$$

Substituting Eq. (7) into Eq. (1), we have

$$S_V(f, \overline{V_d^2}, V_g) \times f^\gamma = \frac{\overline{V_d^2}}{(V_g - V_T)^2} \times \frac{qk_B T t_{ox}}{\lambda\varepsilon_{ox} E_g LW \ln(t_{max}/t_{min})} \times \frac{q\Delta N_d}{C_{ox}} \tag{8}$$

Given device and stress,

$$S_V(f, \overline{V_d^2}, V_g) \times f^\gamma = C\Delta N_d \tag{9}$$

where C is a constant. The left side of the above formula is the power spectrum and the right side is the product between the change in defects and a constant. From this, we find that the number of defects is in direct proportion to the power spectrum Sf^γ. So, the change of device power spectrum before and after hot carrier injection reflects the change of the defect number before and after hot carrier injection. Then, we can use the device power spectrum before hot carrier injection to characterize its anti-hot carrier effect ability. If the power spectrum of the device before hot carrier injection is greater, its anti-hot carrier effect ability is lower. On the contrary, if the power spectrum of the device before hot carrier injection is lower, its anti-hot carrier effect ability is higher.

3 Experiment

We use the change of traditional electronic parameter V_T and $g_{m(max)}$ as the standard to validate the relationship between device disfigurement and $1/f$ noise. According to the model of the $1/f$ noise parameter Sf^γ in MOS devices, there is a close relationship between the stress and $1/f$ noise. We carry out the experiment at three different stresses: high gate voltage, middle gate voltage, and low gate voltage. The devices are short channel n-MOSFETs fabricated by the Huajing corporation's 1.0CMOS process (the gate oxide thickness is 20 ± 1.5nm, and the proportion between width and length is 50/1.0). Its high gate voltage, middle gate voltage, and low gate voltage are V_D = 4.5V, $V_G - V_T$ = 0.2V, V_D = 4.5V, V_G = 2.25V, and $V_D = V_G$ = 4.5V, respectively.

We use the semiconductor parameter analyzer HP4156B to measure the electronic parameters V_T and $g_{m(max)}$ of the device before and after hot carrier injection. The change of electronic parameters before and after hot carrier injection is standard to validate the legitimacy of the experiment. We compare it with the noise parameter change to get the sensitivity characteristic of the device hot carrier effect. After annealing, some oxide traps are recovered in the device, but the interface state is unchanged. In order to distinguish them, the device is annealed after hot carrier injection. In the process of the experiment, the source and drain of the device are grounded, meaning $V_S = V_B$ = 0V. All tests are carried out in a shield room at room temperature.

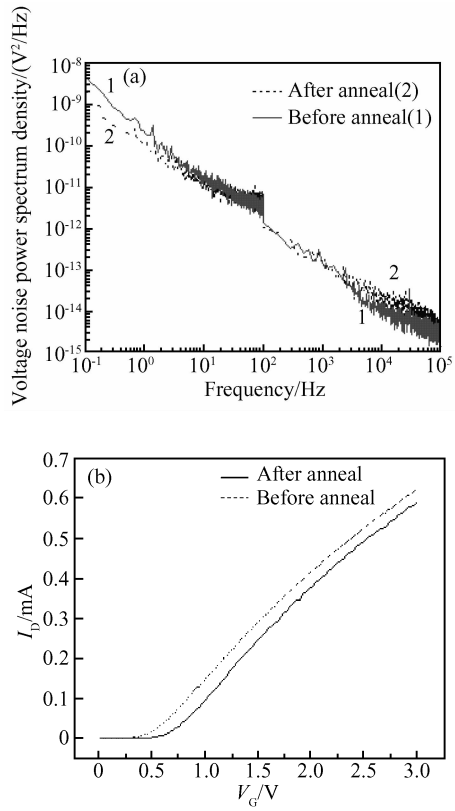

Fig. 1　(a) Noise power spectrum density of the device before and after annealing; (b) I_D-V_G plot of the device before and after annealing

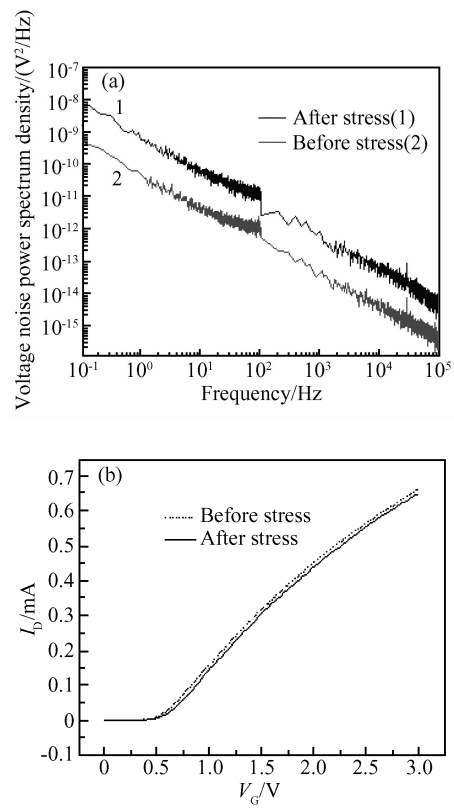

Fig. 2　(a) Noise power spectrum density of the device before and after stress; (b) I_D-V_G plot of the device before and after stress

4　Results

4.1　Device electronic parameter and noise parameter change under low gate voltage stress

First, hot carrier injection was performed under low gate stress $V_D = 4.5\text{V}$, $V_G - V_T = 0.2\text{V}$ for 1800s, followed by annealing at room temperature for 2000s, under $V_G = 1.2\text{V}$, $V_D = 0\text{V}$ stress. Figure 1 shows the noise power spectrum density plot and the I_D-V_G plot of the device. Table 1 shows the change of the parameters before and after annealing.

4.2　Device electronic parameter and noise parameter change under middle gate voltage stress

Hot carrier injection was performed under middle gate stress $V_D = 4.5\text{V}$, $V_G = 2.25\text{V}$ for 1800s.

Figure 2 shows the noise power spectrum density plot and the I_D-V_G plot of the device. Table 2 shows the change in the parameters before and after stress.

Table 1　Change of variety parameter before and after anneal at low gate stress

	Sf^{γ}	V_T	$g_{m(max)}$	γ
Before anneal	4.47×10^{-7}	5.01×10^{-1}	3.02×10^{-4}	1.03
After anneal	6.08×10^{-7}	6.05×10^{-1}	2.60×10^{-4}	0.95
Change ratio	36%	20.8%	−14.1%	−7.73%

4.3　Device electronic parameter and noise parameter change under high gate voltage stress

Hot carrier injection was performed under high gate stress $V_D = 4.5\text{V}$, $V_G = 4.5\text{V}$ for 1800s.

Figure 3 shows the noise power spectrum density plot and the I_D-V_G plot of the device. Table 3 shows the change of the parameters before and after stress.

5　Discussion

After hot carrier injection under low gate voltage stress ($V_G = V_D/5$), the short channel effect in the device produced a hot-hole and neutral electron trap. Because hot-holes can not enter into oxide deeply, most of them appear near the interface. A neutral oxide trap and tunnel electron from silicon substrate combining and forming an electronegative center is essential to annealing. Then, the electronegative center counteracts with a nearby positive electricity cen-

Table 2　Change of variety parameter before and after middle gate stress

	Sf^{γ}	V_T	$g_{m(max)}$	γ
Before stress	1.11×10^{-7}	5.47×10^{-1}	3.52×10^{-4}	1.06
After stress	1.39×10^{-6}	5.7×10^{-1}	3.29×10^{-4}	1.06
Change ratio	115%	4.84%	−6.57%	0.246%

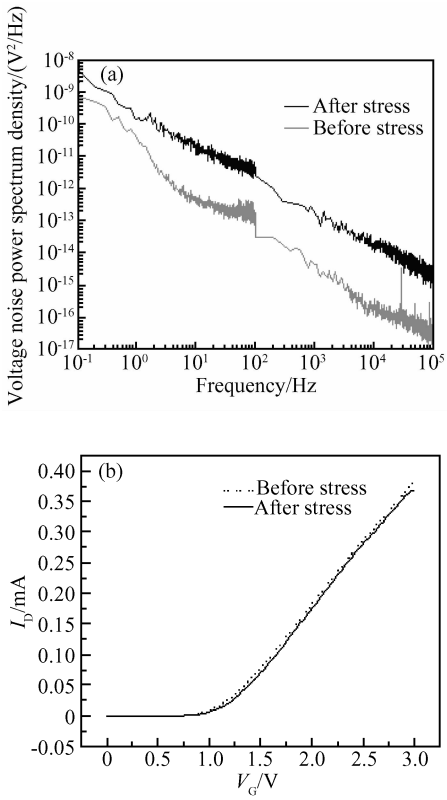

Fig. 3 (a) Noise power spectrum density of the device before and after stress; (b) I_D-V_G plot of the device before and after stress

Table 3 Change of variety parameter before and after high gate stress

	Sf^{γ}	V_T	$g_{m(max)}$	γ
Before stress	1.39×10^{-8}	1.11	2.50×10^{-4}	1.16
After stress	4.98×10^{-7}	1.14	2.49	1.04
Change ratio	349%	2.44%	−0.6%	−10.3%

ter[6]. The oxide trap decreases, and the interface state remains unchanged. Figure 1 shows that the $1/f$ noise power spectrum is elevated. From Table 1, compared to the electronic parameters, the $1/f$ noise parameter Sf^{γ} change ratio is 36%. It is the most sensitive parameter for the hot carrier effect under low gate voltage stress.

After hot carrier injection under middle gate voltage stress ($V_G = V_D/2$), both electrons and holes inject into the gate oxide near the interface. The electrons and holes recombine, which produces an oxide trap or interface state. Meanwhile, the quasi-Fermi energy level of electron debases. The injection hole and capture electron are conducted. So, after hot carrier injection under middle gate voltage stress, both the oxide trap and interface state increase. Figure 2 shows that the $1/f$ noise power spectrum is higher than before. From Table 2, compared to the electronic parameters, the $1/f$ noise parameter Sf^{γ} change ratio is 115%. It is the most sensitive parameter for middle gate voltage hot carrier stress.

After hot carrier injection under high gate voltage stress ($V_G = V_D$), electrons mostly inject. Capturing electrons in a gate oxide produces an oxide trap or interface state. Here, most defects are far from the interface. A number fluctuation of the carrier happened at an electron trap far from the gate oxide. Migratory fluctuation of the carrier happened between the old interface state and the new interface state. Figure 3 shows that the $1/f$ noise power spectrum is elevated. From Table 3, compared to the electronic parameters, the $1/f$ noise parameter Sf^{γ} change ratio is 349%. It is the most sensitive parameter for hot carrier effect under high gate voltage stress.

6 Conclusion

In this paper, we researched the characteristics of the $1/f$ noise parameter Sf^{γ} in n-MOSFET hot carrier degradation under low, middle, and high gate voltage stress, respectively. We developed a method to characterize the ability of the MOS device anti-hot carrier effect using the $1/f$ noise parameter Sf^{γ}. We performed an experiment on the n-MOSFET hot carrier effect under low, middle, and high gate voltage stress to validate its legitimacy and sensitivity. The result agrees well with the developed model. We proposed a nondestructive measure for n-MOSFET under DC hot carrier stress.

References

[1] Benfdila A. Critical dimensional MOSFETs and scope for reliable characterization techniques. First International Workshop on Semiconductor Nano-Crystals, 2005: 119

[2] Xu J P, Lai P T, Cheng Y C. $1/f$ noise in n-channel metal-oxide-semiconductor field-effect-transistors under different hot carrier stresses. J Appl Phys, 1999, 86: 5203

[3] Scofield J H, Doerr T P, Fleetwood D M. Correlation between preirradiation $1/f$ noise and postirradiation. IEEE Trans Nucl Sci, 1989, 36: 1946

[4] Scofield J H, Borland N, Fleetwood D M. Random telegraph signals in small gate-area P-MOS. AIP Conference Proceedings, 1993, 285: 386

[5] Militaru L, Souifi A. Study of a single dangling bond (P_{b0} center) at the SiO_2/Si interface in deep submicron MOS transistors. Villeurbanne: LPM-INSA, 2003: 6

[6] Lai Zuwu. Anti-radiation electronics. Beijing: National Defense Industry Press, 1998: 54 (in Chinese) [赖祖武. 抗辐射电子学. 北京: 国防工业出版社, 1998: 54]

DC 应力 n-MOSFET 热载流子退化的 $1/f$ 噪声特性

刘宇安†　余晓光

（井冈山大学数理学院，吉安　343009）

摘要：研究了 DC 应力 n-MOSFET 热载流子退化的 Sf^{γ} 噪声参量.提出了用噪声参数和 Sf^{γ} 表征高、中、低三种栅应力下 n-MOSFET 抗热载流子损伤能力的方法.进行了高、中、低三种栅压 DC 应力下热载流子退化实验.实验结果和本文模型符合较好.

关键词：n-MOSFET；热载流子效应；$1/f^{\gamma}$ 噪声
PACC：7340Q；5225G
中图分类号：TN386.11　　**文献标识码**：A　　**文章编号**：0253-4177(2008)07-1263-05

† 通信作者.Email:danu0012004@163.com
2007-08-31 收到，2008-01-27 定稿