A Novel SPICE Macro-Model for Power ICs

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Abstract: A novel macro-model of high-voltage DMOS for power ICs is proposed according to the canonical piecewise-linear model technique. The method describes nonlinear characteristics directly as functions of node voltage. We employ the Powell algorithm, which gives higher accuracy without the convergence problem and with lower analysis time. Finally, a comparison of simulation results and measurement results in application to power ICs is reported.

Key words: power IC; SPICE; macro-model; DMOS
PACC: 1230B **EEACC**: 1205
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2008)02-0229-05

1 Introduction

A large range of industrial and consumer circuits either require HV driving capabilities, or are intended to work in a high-voltage environment. This includes automotive, flat panel displays, robotics, etc. For proper circuit design, it is crucial that the switching transistors for the DMOS transistors be accurately simulated. Modeling accuracy, ease of parameterization, and, most importantly, compatibility with existing design flows are the main factors in the choice of modeling strategy. There exist four methods that are used to build macro-models for the power semiconductor devices[1]: the structural macro-model, the C code model, the AHDL model, and the analog behavioral macro-model.

In the last decade, more than 20 power DMOS structural macro-models were developed, all of them having the generic level 1 or 3 intrinsic MOSFET model[1~3] as a central element. The challenge in a power DMOS model is the accurate description of interelectrode capacitances, which exhibit hard nonlinear dependencies on terminal voltages. The intrinsic model gives major static and dynamic errors, as it does not simulate the specific power device phenomena. The main effects not modeled are: the quasi-saturation effect and the transconductance decay at high current levels, for the static regime; and nonlinear voltage dependencies of interelectrode capacitances, for the dynamic regime.

Customized physical device models[4~6], on the other hand, are one means of delivering better results, though often at the cost of a complicated model and cumbersome parameter extraction. Physical models widely used in design regions or research regimes for new devices are unavailable in commercial simulators and not portable because they pay more attention to the internal physical mechanisms.

In this paper, a novel macro-model has been proposed according to the canonical piecewise-linear modeling technique. Our novel approach features a standard SPICE compatible macro-model, which can be used with any SPICE simulator. It is a behavioral model which can be used as a netlist add-on to existing models such as MOS Level 3 or BSIM. The presented macro-model has a modular structure, each describing the device's internal static equations and the nonlinear interelectrode capacitance directly as functions of gate and drain voltage using VCCS and VCCAP available from SPICE. Powell's algorithm was employed in order to optimize the coefficients of functions which describe the electrical behavior of the device. The simulation results of the proposed macro-model are compared with those the existing intrinsic and structural models, and show better agreement with the experiments. Similar approaches can be applied to all the other power semiconductor devices (e.g. BJT, SCR, GTO, IGBT, and MCT).

2 Equivalent circuit and parasitic capacitance extraction

The schematic cross-section view of the DMOS structure using p-substrate and n-epitaxy considered here are shown in Ref. [7], which includes the HV nVDMOS and the pLDMOS. The thickness of the n-epitaxy layer is 25μm. For compatibility with the pLDMOS and the LVCMOS, the drain electrode of

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Received 3 September 2007, revised manuscript received 8 October 2007

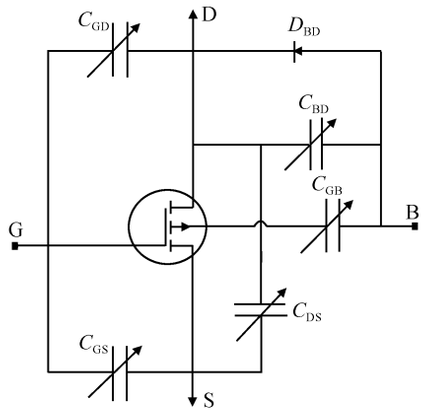

Fig. 1 Equivalent circuit of DMOS device

the nVDMOS is elicited to the surface via the n^+-bury layer and the n^+-sinker. The p-iso, biased to 0V, is used to separate nVDMOS from pLDMOS, LVCMOS, and other nVDMOSs. Here, the p^+n junction was used for the isolation. Although the junction-isolation area is larger than that of the trench isolation used in the SOI scan-driver IC[8~10], the p-iso can be formed with the same diffusion process of the n^+-sinker, saving process cost. The latch-up effect cased by the parasitic devices in the structure can be greatly reduced by adjusting the process parameters and by adding protection structures between the HV-DMOS and the LV-CMOS in the layout.

The proposed equivalent circuit shown in Fig. 1 is a physical and structural based circuit including the static and dynamic elements. The main difference from the structural modeling approach is that the internal elements are modeled with nonlinear controlled sources, instead of standard SPICE elements. Hence, this method will allow higher accuracy and an easier model parameter extraction algorithm. The static behavior was modeled with mathematical expressions that are functions of the gate and drain voltage using the voltage controlled current source available from SPICE. D_{BD} and C_{BD} model the parasitic diode current and p-n junction capacitance between the p-substrate and the drain, respectively. C_{GB} and C_{GS} are parasitic capacitance of gate-substrate and gate-source, respectively, and they are all nonlinear voltage dependent. Another two important capacitances are parasitic gate-drain C_{GD} and drain-source C_{DS}. They are modulated by gate and drain voltage synchronously, which show two dimensional continuous characteristics. These parasitic capacitive components can be extracted by simulation as reported in Ref. [11]. The capacitor is derived from Eq. (1).

$$C = \frac{\mathrm{d}Q}{\mathrm{d}U} = \frac{\frac{\mathrm{d}Q}{\mathrm{d}t}}{\frac{\mathrm{d}U}{\mathrm{d}t}} = \frac{I'(t)}{U'(t)} \tag{1}$$

where $I'(t)$ and $U'(t)$ are the differential coefficients with respect to time of current and voltage, respectively, and these two terms can be obtained by simulations such as MEDICI.

3 DMOS macro-model description

The static and dynamic behavior can be obtained from the data sheet, measurement data, and simulation methods. This gives us a clue that we could establish a macro-model from these external characteristics and that the internal physical equations do not need to be clarified. The challenge in the macro-model is the accurate description of interelectrode capacitances. The canonical piecewise-linear model technique[12] can be used to construct the macro-model without losing the continuity and nonlinear characteristics.

Starting from the measurement of the terminal *I-V* characteristic of device, we fit these measured data into a compact global piecewise-linear representation called a canonical piecewise-linear function[12,13]:

$$f(x) = \alpha + Bx + \sum_{i=1}^{\sigma} C_i |\langle \alpha_i, x \rangle - \beta_i| \tag{2}$$

where α, x, C_i and α_i are the n-dimensional vectors, B is an $n \times n$ matrix, β_i is a scalar, and "$\langle , \rangle$" denotes the inner product of two vectors. Because no redundant data is stored, this approach greatly reduces the memory space required for the storage of the device parameters. Moreover, the special structure of the associated canonical piecewise-linear equation allows us to develop a highly efficient algorithm for solving these equations. In this paper, in order to guarantee that the parameters obtained by the iteration algorithm will lead to a global minimal approximation error, we apply the Powell's optimization algorithm to find the parameters $\alpha, x, C_i, \alpha_i, B, \beta_i$ for a given σ (i.e., the number of boundaries in the domain space), such that the approximation error is minimized. In this way, the internal physical phenomena of the device are not required as long as the terminal voltage and current can be accurately measured.

Assume the set of data points $(x^{(l)}, y^{(l)})$, $l = 1, 2 \cdots N$ is obtained either by measuring the terminal *I-V* characteristic or by numerical simulations such as MEDICI. We want to find an optimal canonical piecewise-linear representation:

$$y = \hat{f}(x_1, x_2) = a + b_1 x_1 + b_2 x_2 + \sum_{i=1}^{\sigma} c_i |a_i x_1 + a_i x_2 + \beta_i| \tag{3}$$

Each transition in the measured data is modeled with this construct. Applying the optimization algorithm, we obtain the following canonical piece-wise

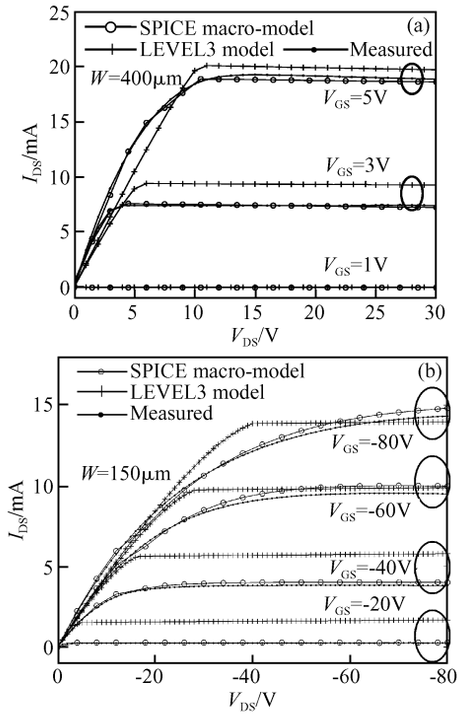

Fig. 2　Comparison *I-V* measured data and simulations of DMOS　(a) nVDMOS; (b) pLDMOS

model, which optimally fits the data points with $\sigma = 4$ boundary lines:

$$i = a + b_1 v_1 + b_2 v_2 + c_1 | m_1 v_1 - v_2 + t_1 | + c_2 | m_2 v_1 - v_2 + t_2 | + c_3 | m_3 v_1 - v_2 + t_3 | + c_4 | m_4 v_1 - v_2 + t_4 | \quad (4)$$

where a, b_i, c_i, m_i and t_i are a set of optimal parameters obtained through Powell's optimization algorithm, and v_1 and v_2 represent the gate voltage and drain voltage, respectively. Consequently, the drain-source current "i" can be modeled accurately without losing continuity.

Furthermore, the nonlinear capacitor modulated by gate and drain voltage can be modeled with the same method using the corresponding coefficients. The entire element in the proposed equivalent circuit as shown in Fig. 1 can be directly described with the above mathematical expressions. Finally, the macro-model is completed according to the structure of equivalent circuit using this technique. Each device's static and dynamic characteristics are described by a distinct set of parameters, which leads to a very clear and simple algorithm for parameter extraction from the data sheets characteristics.

4　Results and discussions

The proposed power DMOS macro-model was compared with those of the existing intrinsic and structural models. The static and dynamic simulations were performed with the SPICE simulator and the results for the proposed macro-model showed better agreement with the measured data and MEDICI's simulations.

4.1　Static results

The equivalent circuit shows that the power device has different elements. Each element can be characterized with a mathematic function. Depending on the terminal voltages and currents, the *I-V* characteristics can be modeled with VCCS like the format in Eq. (3). Figures 2 (a) and 2 (b) show the comparison of *I-V* measured data and simulation's result of nVDMOS and pLDMOS, respectively. Compared to the LEVEL3 model[14], our DMOS macro-model shows a better agreement with the measured data. The quasi-saturation characteristic is modeled accurately and the DC error is within 5%.

Although the static model[14] considers the mobility degradation through the THETA parameter, it cannot simulate the forward transconductance decay at the high current level of pLDMOS, as shown in Fig. 2 (b). Our proposed macro-model can simulate this characteristic accurately. The drain current calculated from Eq. (3) (the circled line in Fig. 2) matches the measured data fairly well, and in some regions of operation, it is even better than the measurement (dotted line). This comparison clearly demonstrates the versatility of the canonical piecewise-linear model approach. The proposed macro-model shows great superiority to the conventional macro-model based on standard elements built into SPICE.

4.2　Dynamic results

Power DMOS devices are employed as switches in power control circuits. To achieve an accurate description of DMOS switching waveforms, it is necessary to develop a high precision model for gate-drain (C_{GD}) and drain-source (C_{DS}) capacitances, which exhibit nonlinear variations with gate-drain and drain-source voltages. We now apply the optimization algorithm to the nonlinear capacitance. Depending on the result of MEDICI's simulations, the nonlinear capacitance can be modeled with the same method used for the static regime. Figures 3 (a) and 3 (b) present the nonlinear C_{GD} capacitance of nVDMOS and pLDMOS, respectively, generated by our macro-model. The macro-model gives a better agreement with the MEDICI results, and, at the same time, assures a higher continuity of $C(V)$ curves.

The great advantage of the proposed macro-model is that it gives an easy and direct way of modeling the nonlinear effects of power devices. Furthermore, the model parameter extraction algorithm was greatly

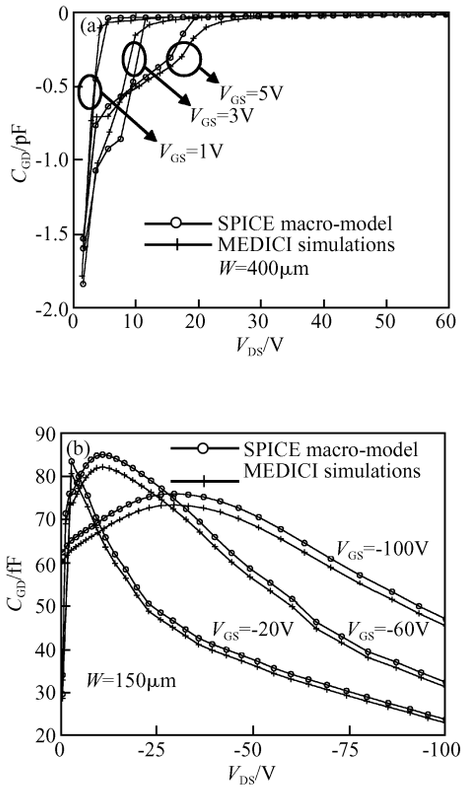

Fig. 3 Comparison of C_{GD} MEDICI data and macro model of DMOS (a) nVDMOS; (b) pLDMOS

simplified, as the nonlinear effects are directly specified with behavioral controlled sources. In the same way, the other nonlinear capacitances, including drain-source capacitance (C_{DS}), can be modeled with their behavioral functions.

4.3 Convergence problem

The transient simulation of a power semiconductor device may reveal, in many cases, a difficult convergence problem due to the hard nonlinearities, the model discontinuities, and the fast switching. Most of the problems appear in the bias point calculations and the transient analysis start-up. Both the drain-source current or gate-drain capacitance have nonlinear continuous characteristics. The three-dimensional plots for the I_{DS} surface over the V_{GS}-V_{DS} plane of the proposed nVDMOS macro-model are shown in Fig. 4. In order to guarantee convergence in the simulation, the continuity has been preserved well.

To improve the convergence, a partition boundary must be determined because different partitions would give rise to different optimal parameters and our goal is to choose a global minimal approximation error for the canonical piecewise-linear model representation. Furthermore, choosing an initial set of breakpoints and modifying the corresponding weighting factor are important in order to guarantee the convergence in the solution search.

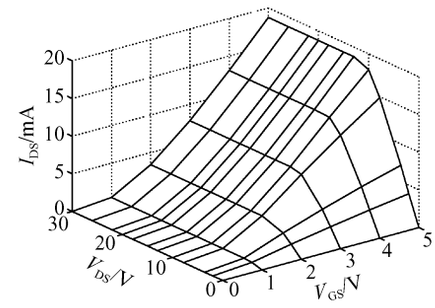

Fig. 4 Three-Dimensional plots for the IDS of HV-nVDMOS

5 Application to power ICs

In the recent years, several types of HV-output level-shift circuit construction, such as the MOS type output circuit and the BiCMOS-type output, have to maintain a high-level output current over a long distance and a larger magnitude of the current is required to obtain higher speed capability. Thus, the full-complementary type level-shift circuit, which can eliminate such static power dissipation and achieve high-speed operation, is widely used in PDP driver ICs[15]. The conventional full-complementary type level-shift circuit can be seen in Fig. 5, where the P1, P2, and P3 are the HV pLDMOS and the N1, N2, and N3 are the HV nVDMOS

Figures 6 (a) and 6 (b) show the rising time and the falling time of the switching waveforms of the developed 100V-rating PDP scan driver IC with 20pF capacitor on the condition of V_{PP} = 80V. The rising time and the falling time of the output stage is about 130 and 60ns, respectively. The proposed model greatly increases the accuracy of the transient switching simulation, due to a better description of the interelectrode capacitances.

6 Conclusion

This paper presents a new method of building a

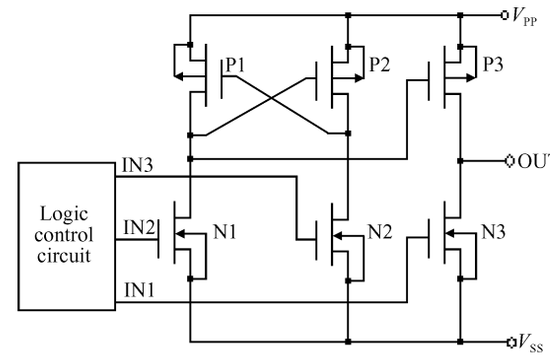

Fig. 5 Conventional schematic level-shift circuit of the PDP scan driver IC

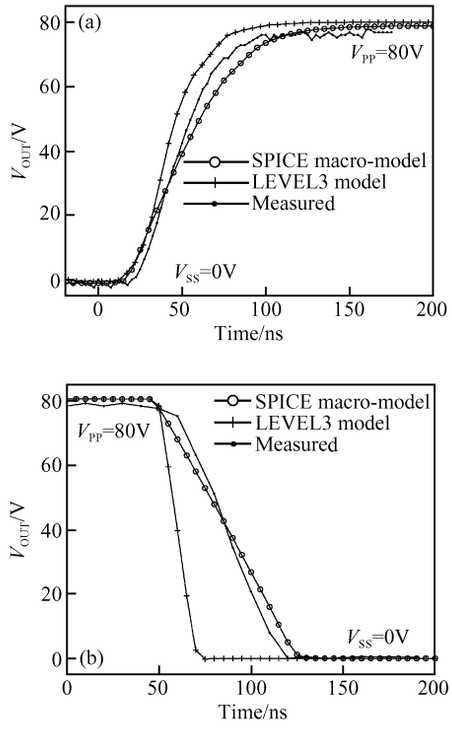

Fig.6　Comparison switching time waveforms of measured and simulations　(a) Rising time; (b) Falling time

high accuracy and efficient SPICE model for the power DMOS devices which can be implemented on all modern SPICE-like simulators. The presented macro-model describes static and the nonlinear interelectrode capacitance directly as functions of node voltage. The accuracy was greatly increased by the direct specification of the device's static and dynamic functions. This model leads to a reasonable analysis time, as it directly computes the mathematical functions instead of spending additional evaluation time on the device models in each iteration while computing the solution.

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一种用于功率 IC 的新型 SPICE 宏模型

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摘要： 基于规范化分段线性模型技术，建立了高压 DMOS 器件的 SPICE 宏模型用于功率集成电路的仿真. 从等效电路模型出发，利用 Powell 算法找到规范化分段线性模型的最佳系数，从而利用节点电压可以直接描述 DMOS 器件的各种非线性特性. 该模型不仅准确性高，而且仿真速度快、收敛性好. 最后，给出了仿真与测试的对比结果，证明了模型的有效性和准确性.

关键词： 功率 IC；SPICE；宏模型；双扩散 MOS

PACC： 1230B　　**EEACC：** 1205

中图分类号： TN402　　**文献标识码：** A　　**文章编号：** 0253-4177(2008)02-0229-05

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2007-09-03 收到，2007-10-08 定稿