Design and Analysis of a Gain-Enhanced, Fully Differential Telescopic Operational Transconductance Amplifier

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Abstract: This paper describes the design and analysis of a fully differential, gain-enhanced CMOS telescopic operational transconductance amplifier (OTA) used in a pipeline analog-to-digital converter (ADC). Specifications of the OTA are derived from the requirements of ADC. Simulation shows that for a 1pF load capacitance, this OTA achieves a high DC gain (approximately 145dB) and a wide unity-gain bandwidth (above 750MHz) at a phase margin 58°. In a configuration where the closed loop-gain is 4, the design spends about 18ns for settling with 0.05% accuracy. Simulations of this design are performed in SMIC CMOS 0.18μm technology.

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1 Introduction

As the channel lengths of MOSFET keep shrinking, the transistors are becoming smaller, faster, and more power efficient. This particularly favors portable handset applications, which the majority of the industry is focusing on. As a fundamental building block of analog designs, high-performance and low-power consumption OTAs operating at a supply voltage of 1.8V or below are required in portable mixed-signal systems. Progressing technology benefits OTA in speed, area, and power consumption. However, when the power supply is lowered, analog designers have to work to design a high-performance OTA. A trade-off among gain, speed, and power, amongst other performance parameters, is necessary. Speed and accuracy are the two most important characteristics in OTA design. For example, in switched-capacitor circuits, fast and high accuracy improves speed and complete charge transfer capability. Fast settling requires a high unity-gain frequency and a single-pole settling behavior of the amplifier, whereas accurate settling requires a high DC gain. However, optimizing OTA for speed and gain leads to contradictory demands. Thus, a trade-off has to be made. A detailed explanation will be given later.

Usually a single stage amplifier, especially telescopic topology, gives fast frequency response but less gain, and a two-stage amplifier can have large gain but medium unity-gain bandwidth. A gain-enhanced (also called gain-boosting, regulated-cascode) amplifier, which exploits the pros of a single stage and a two stage amplifier, gives a fast frequency response and high DC gain. In this technique, both the output resistance and the gain of the main amplifier are increased A_0 times, which is supplied by using a feedback amplifier (FA). However, if the FA is not properly designed, low-frequency pole-zero frequency doublets will appear in the transfer function of the main amplifier. Even though the doublet does not noticeably affect the frequency response, it introduces a slow-settling component, which is undesirable for many applications[1].

A number of gain-enhanced fully differential OTA designs exist in the literature, among which 161MHz GBW and 129dB DC gain at 3.3V were achieved using a 0.35μm CMOS process in Ref.[2]. A DC gain of 102dB and 822MHz GBW were achieved in Ref.[3] for an SMIC 0.25μm CMOS process, but with 35mW power consumption. The OTA designed in Ref.[4] achieved 560MHz GBW but only a DC gain of 92dB. Based on telescopic cascode amplifier designed with the gain-enhanced technique, this study achieves high gain (145dB) and wide unity-gain bandwidth (750MHz) simultaneously.

2 Principle and topology

An amplifier's DC gain is a product of circuit transconductance and output resistance. The transconductance is usually the transconductance of the input transistors. Changing the circuit implementation does not improve this. An effective way to improve gain is

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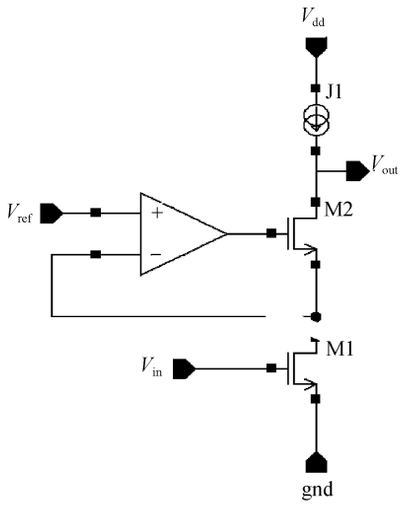

Fig. 1 Cascode gain stage with gain enhancement

by increasing the output resistance. Cascading can make output resistance bigger. But, this technique reduces output swing so that usually only one MOSFET cascades on another. To further improve the output resistance, the gain-enhanced cascode technique is promising.

Figure 1 gives a simple diagram of the gain-enhanced technique. The basic idea is based on a negative feedback loop to set the drain voltage of M2. In small signal analysis, M1 acts as a resistor. It senses a small signal voltage that is proportional to the drain current. This voltage is subtracted from the V_{ref}, so that M2 works in current to voltage feedback mechanism. This negative feedback drives the gate of M2 until the negative input terminal has little value variation from V_{ref}, so a small change of V_{out} does not affect the drain voltage of M1. As a result, the output resistance is amplified by the gain of the amplifier.

$$R_{out} \approx A_1 g_{m2} r_{o1} r_{o2} \tag{1}$$

Since A1 forms a closed loop with M2, stability problem may occur if it is too fast. The circuit has two poles: one is from the output node and the other is from the source of M2, which is also the non-dominant pole of the main amplifier. A doublet (pole and zero pair) quite often occurs in a gain-boosted op amp design. To solve these problems, as a rule of thumb, unity gain frequency of the additional amplifier is in a range between close-loop -3dB bandwidth and non dominant pole frequency of the main amplifier[5].

To implement this technique in a fully differential amplifier, the topology shown in Fig. 2 is used.

The main amplifier is telescopic. This structure can give the highest unity-gain bandwidth. Gain boosting amplifiers A1 and A2 are used to enhance the output impedance as indicated in the principal. This topology increases the output impedance, thus improving DC gain significantly while preserving the GBW.

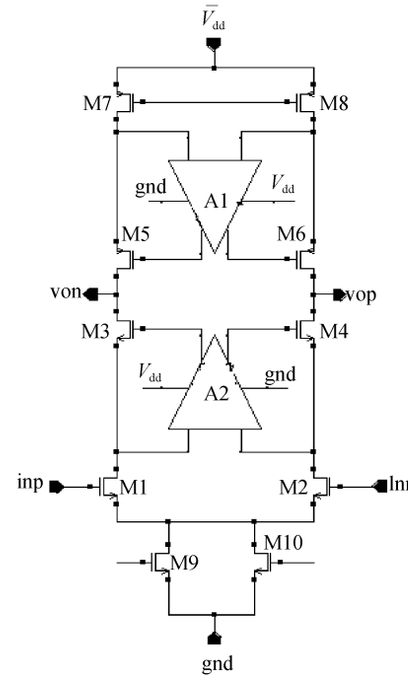

Fig. 2 Gain-enhanced fully differential amplifier without CMFB

3 Circuits design and analysis

Requirements of different applications in specifications vary dramatically. In this section, an example is provided. Design considerations are followed by the introduction of a detailed circuit topology analysis.

3.1 Specification derivation

Applications place constraints on circuit specifications. For use in a pipeline ADC system, the amplifier is designed as the ADC as required. For instance, in the case of designing a 10bit, 25MS/s pipeline ADC, the requirements for OTA is analyzed as follows. The 25M sampling rate per second gives a signal period T that is 40ns. To insure the signal settles to a final value within half of the period, the amplifier should have a settling time of less than 20ns to achieve 0.05% accuracy. This accuracy is due to the 10bit requirement. 2^{10} gives 1024, and its reciprocal is 0.000977. This means the amplifier must achieve at least 0.0977% by that amount of settling time. Obviously, it is better for the amplifier to have more redundancy. Therefore 0.05% accuracy was chosen. For a step input, the output response of the first-order system is given by:

$$V_0(t) = V(1 - e^{-t/\tau}) \tag{2}$$

For 0.05% accuracy, the exponential part $e^{-t/\tau}$ has to be less than it. Thus t is equal to 8τ. A τ is required

for slewing. So the total settling time is 9τ. A 1 V_{pp} is desired at the output so the V in Eq. (2) is 1. The slewing rate (SR) is thus given by 1V normalized by 1τ, the time for slewing. Hence, $9\tau \leqslant 20$ns, meaning that SR$\geqslant$450 V/μs.

Once the slew rate is obtained, for a fully differential OTA, the total current flowing through M9 and M10 is given by:

$$I_{tail} = SR \times 2C_L \tag{3}$$

C_L is the load capacitance on each output leg.

3.2 Circuit design and description

As mentioned above, unity-gain bandwidth (UGB) is against DC gain. The following equations prove that.

$$A_v = G_m R_{out} \tag{4}$$

$$\omega_u = g_m / C_L \tag{5}$$

$$g_m = (2K' I_D W/L)^{1/2} \tag{6}$$

$$r_{out} \approx 1/\lambda I_D \tag{7}$$

$$\lambda \propto 1/L \tag{8}$$

Substituting Eqs. (6)~(8) into Eqs. (4), (5) gives, respectively,

$$A_v \propto (WL/I_D)^{1/2} \tag{9}$$

$$\omega_u \propto (I_D W/L)^{1/2}/C_L \tag{10}$$

Clearly, the high-gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high-speed requirement calls for a single-stage design with short-channel devices biased at high current levels[1].

For stability, the tail MOS transistor is split into two equal parts. The tail MOS is chosen to be a common mode feedback point because of its large transconductance and, thus, its sufficient common mode gain. But because of the large parasitic capacitance of the CMFB load, stability problems may occur. A trade-off has to be made between the common mode gain and the phase margin of the common mode feedback loop. Splitting the tail MOS in two significantly reduces the load to CMFB while sacrificing g_m, but good phase margin can be obtained.

The gain-boosting amplifiers A1 and A2 supply additional gain to the main amplifier to achieve a high DC gain. They are all in folded-cascoded topology. An nMOS differential input pair is used in A1 and is shown in Fig. 3. A pMOS differential pair is used in A2, whose schematic is similar to A1 and thus not given here.

In A1, for example, the amplifier senses the drain voltages of M7 and M8 as input voltages for the differential pair. The differential outputs are connected to the gates of M5 and M6. Common mode voltages are required by the M5 and M6, so that the A1 does not need to have a wide output swing.

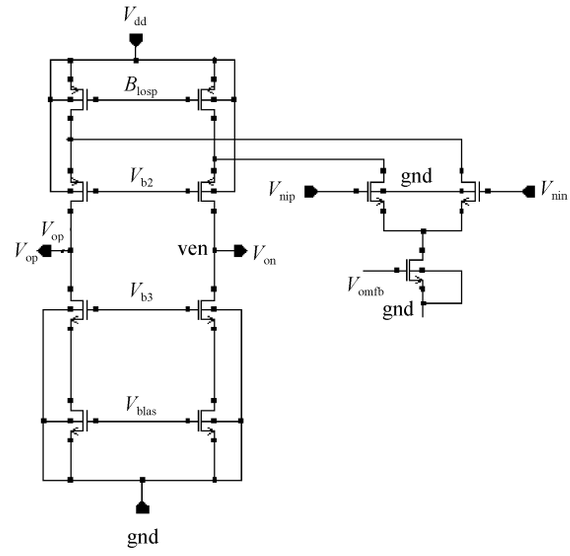

Fig. 3　Gain-boosting amplifier, A1

Gain-boosting amplifiers should have a unity gain bandwidth comparable to the main amplifier. To achieve that, more power will be consumed and larger transistors have to be used. Good stability and preservation of the main amplifier's UGB without gain-boosting can be obtained with less bandwidth. Conventionally,

$$\beta \omega_u \leqslant \omega_{u,add} \leqslant \omega_{nd} \tag{11}$$

β is the feedback factor of closed loop, ω_u denotes the unity gain frequency of the main amplifier, $\omega_{u,add}$ denotes the unity gain frequency of the additional amplifier, and ω_{nd} denotes the non-dominant pole frequency. With reasonable bandwidth, power consumption in this stage is reduced. Usually the power of gain boosting stage is one-fifth of the main circuit. Referring to Ref. [1], the phase margin of these stages has to be greater than 70° to achieve proper settling behavior.

3.3 Design considerations

Large transconductance offers better gain and bandwidth performance. Although for a gain-boost amplifier, the output impedance is increased by several orders, as the two-stage topology gain requirement does not place a critical rule on the design. However, high speed OTA demands larger transconductance. At certain power consumption, transconductance of nMOS is superior to that of pMOS. Therefore, nMOS differential pairs are chosen as the input pair.

We must consider that the load of A1 is the capacitance from the gates of M5 and M6. Similarly, the capacitance from the gates of M3 and M4 are the load of A2. Therefore, these transistors cannot be too big.

To obtain a good settling time performance, the main amplifier is designed to have a phase margin o-

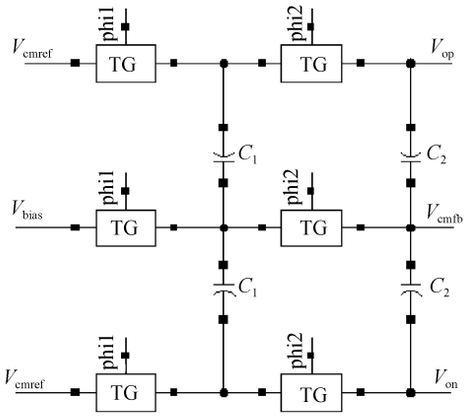

Fig. 4 SC-CMFB network

ver 80°. The phase margin of the auxiliary amplifier is required to be about 70°[1]. The CMFB circuit also affects settling performance. The circuit in Fig. 5 can shorten the settling time effectively.

4 Common mode feedback circuit

A common mode feedback circuit is necessary in a fully differential amplifier. Since this design is used in the pipeline ADC, a switched-capacitor CMFB is used in the main amplifier. A continuous-time CMFB is implemented in the gain-boosting amplifiers.

4.1 SC-CMFB

SC-CMFB is used in the main amplifier. The main advantages of the SC-CMFB are that they have no constraint on the maximum allowable differential input signals, have no additional parasitic poles in the common mode loop, and are highly linear[1]. It also has no static power consumption. Compared with its resistive CMFB counterpart, its capacitive impedance does not vary the output impedance so that it does not affect the DC gain. However, capacitors usually occupy a large area, and clocks are needed for the switching actions. Although charge injection can be reduced dramatically, nonlinear clock noise feeding through noise into the amplifier output nodes is still a problem. Additional capacitances are added to the output nodes, increasing the load of the amplifier. For these reasons, SC-CMFBs are typically only used in switched-capacitor applications rather than continuous time applications[7].

Figure 4 shows the SC-CMFB network. A simple working mechanism is presented. In the figure, TG represents the transmission gate. Phi 1 and phi 2 are two nonoverlapping clocks. "V_{op}" and "V_{on}" are connected to the positive output node and the negative output node of the amplifier, respectively. "V_{cmref}" is a desired common mode (CM) output DC voltage. "V_{cmfb}" connects the CM feedback point of the main circuit. "V_{bias}" is a desired DC voltage for the CM point. When phi 1 is high, C_1 charges to V_{cmref}-V_{bias} and the charge is preserved. When phi 2 is high, C_1 connects between V_{op} (V_{on}) and V_{cmfb}. In the steady state, V_{op}(V_{on}) is constant because the applied voltages V_{cmref} and V_{bias} are both DC voltages and because the switched-capacitor integrator operates in a negative feedback loop[8]. After V_{op} (V_{on}) becomes constant, C_1 does not transfer charge onto C_2. This forces $V_{op} - V_{cmfb} = V_{cmref} - V_{bias}$. Thus, once $V_{cmfb} = V_{bias}$ is satisfied, the output voltage is equal to the nominal DC voltage. In the circumstances here, "V_{bias}" can be generated employing a current mirror to replica the gate voltage of the original tail MOS.

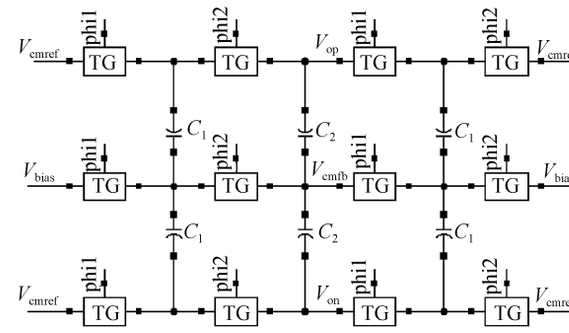

Fig. 5 SC-CMFB to improve settling time

To achieve better settling time behavior, a more complicated SC-CMFB is presented in Ref. [6]. The only drawback of this circuit is that it occupies more area. Figure 5 shows the schematic of the circuit. Usually, C_1 is designed to be 5～10 times of that C_2 for fast DC settling. But, the capacitances have to be chosen carefully to avoid overloading the amplifier or affecting the charge injection of the switches.

4.2 Continuous-time CMFB

Because the outputs of the gain boosting amplifier do not need to swing high, a continuous time CMFB circuits is used. In this paper, sources coupled differential pairs is adopted. The circuit is shown in the next page.

This topology is not suitable for high output swing amplifier. The requirement that MOSFETs of differential pairs remain during entire output swing imposes a limit on the output swing of the operational amplifier. The input range is related to the gate overdrive voltage of the transistors in the middle of Fig. 6. Assuming a high swing voltage for V_{op}(V_{on}) is demanded, a large overdrive voltage is needed for the differential input pairs. To keep the differential pairs on, $2^{1/2}$ V_{ov} is set to be equal to the output swing range. This result, in turn, may give an unacceptable

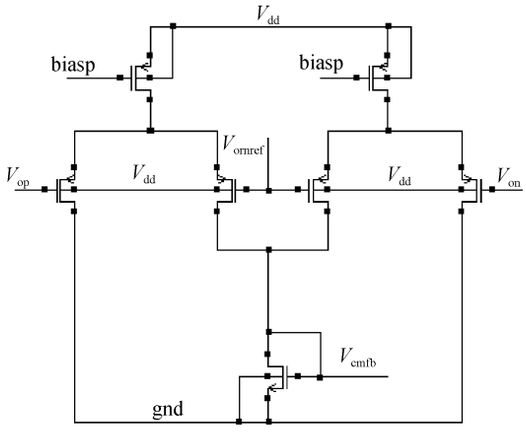

Fig. 6　Sources-coupled differential pair CMFB

W/L ratio. We adopt this circuit to be the CMFB for the gain-boosting amplifier because it does not need a large output variation. The top pMOSs are biased from a current mirror. The middle pMOSs are designed to have the same configuration. Half of the total current flows through the diode connected nMOS. An nMOS in the gain-boosting amplifier and the diode-connected nMOS in the CMFB form a current mirror. Thus，once the current of gain-boosting amplifier is assigned，the W/L of diode-connected nMOS also is determined. The total current in CMFB is obtained，and therefore the top pMOSs are set. With the output swing and the amount of current flowing through，there is not much freedom for adjusting the differential input pairs.

5　Simulation results

Simulations of the OTA were done within the cadence design environment by employing the Spectre simulator. A 0.18μm standard CMOS process from SMIC is used. The gain and phase margin performances are shown in Fig. 7. The figure indicates that the DC gain is 144.7dB. The unity gain frequency is slightly above 750MHz. A phase margin of 58° is achieved at the unity-gain frequency.

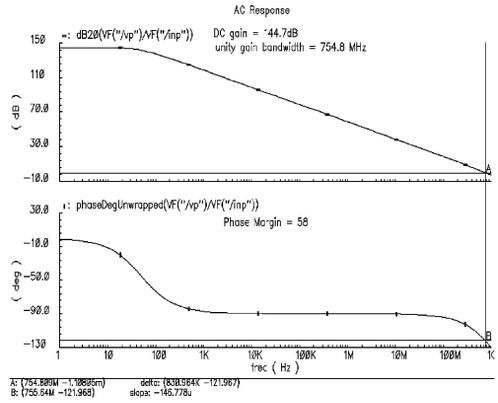

Fig. 7　Gain and PM performance

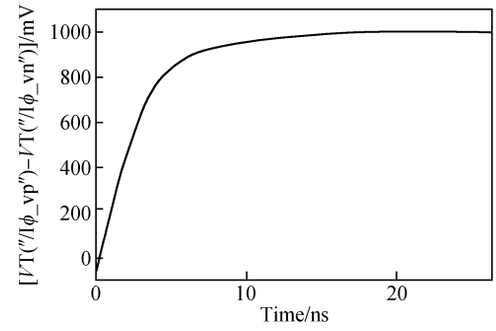

Fig. 8　OTA step response (closed loop gain = 4)

To measure the settling time of the OTA，it is in a closed loop of gain 4. One 250mV step signal is applied on the differential inputs of the OTA. One 1 volt step response is settled after 18ns. The plot is shown in Fig. 8.

Table 1 lists a brief comparison between this work and Refs.[1～3]. The OTA designed in Ref.[3] had very good performance，but power category is unacceptable. The design from Ref.[2] gave the best power performance but with only 161MHz bandwidth. The design reported in Ref.[1] may be a fairly good choice if it could achieve higher gain. Compared to Ref.[2]，without increasing the power too much，the bandwidth is expanded significantly in this work. Also，comparable with Ref.[2]，a 2 pF load is used. The bandwidth is 564MHz，which is much wider than that in Ref.[1].

Table 1　Performance comparison

References	Ref.[2]	Ref.[3]	Ref.[1]	This work
Process/μm	0.35	0.25	0.18	0.18
Supply voltage /V	3.3	2.5	1.8	1.8
DC gain /dB	129	102	80	144.7
Phase margin /(°)	70.4	62.5	73	58
C_L/pF	2	4	1	1
Bandwidth /MHz	161	822	660	754
Power dissipation /mW	3.9	35	3.8	4.46

6　Conclusion

A 144.7dB 754MHz OTA has been designed. The circuit is based on the single-stage，gain-boosting topology. This design consumes only about 4.5mW. Its high gain，wide bandwidth，and low power consumption make it a good choice for pipeline ADC applications. This work will be employed in a 10bit pipeline ADC design.

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增益提高型套筒式全差分跨导放大器的设计与分析

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摘要：提出了一种应用于流水线型模数转换器(ADC)的增益提高型套筒式全差分跨导放大器(OTA)的设计与分析方法.通过 ADC 的性能要求推导出 OTA 的设计指标.该设计中 OTA 的架构由主运放、增益辅助运放及共模反馈电路 3 部分子电路组成.设计采用 SMIC CMOS 0.18mm 工艺平台.该设计方法的实验结果表明：1pF 负载下，跨导放大器的直流增益达到 145dB，单位增益带宽超过 750MHz，相位裕度达到 58°.闭环增益为 4 时，放大器在 20ns 内稳定到 0.05%的精度.

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