A Novel Interconnect Crosstalk Parallel RLC Analyzable Model Based on the 65nm CMOS Process*

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Abstract: Based on the 65nm CMOS process, a novel parallel RLC coupling interconnect analytical model is presented synthetically considering parasitical capacitive and parasitical inductive effects. Applying function approximation and model order-reduction to the model, we derive a closed-form and time-domain waveform for the far-end crosstalk of a victim line under ramp input transition. For various interconnect coupling sizes, the proposed RLC coupling analytical model enables the estimation of the crosstalk voltage within 2.50% error compared with Hspice simulation in a 65nm CMOS process. This model can be used in computer-aided-design of nanometer SOCs.

Key words: nanometer CMOS; interconnect coupling crosstalk; parallel RLC analytical model; parameter extraction; function approximation

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1 Introduction

Rapid advancement in VLSI technology has enabled the CMOS integrated circuit to enter the nanometer process. The feature size on a chip is decreasing and the operating frequency is increasing. In conjunction with ASIC development of SOC and NOC, the crosstalk noise between the adjacent interconnect lines has become a critical factor for circuit performance and signal integrity[1~13]. Furthermore, with present VLSI technology, on chip interconnects are best modeled as a network of coupling lines. Hence, it is important to establish a simple and efficient model to accurately evaluate the crosstalk voltage, which not only provides a reference for IC designers in high speed CMOS design to avoid logic error or time functional failure, but also offers excellent advantages for the exploitation of EDA software.

Prior to the present nanometer CMOS process, many analysis techniques and tools had been developed for crosstalk noise estimation. Sakurai[7] proposed a partial differential equation metric to solve the expression of peak noise between interconnect lines coupled with capacitance. Pillage[3] introduced asymptotic waveform evaluation (AWE) for RC networks. His technique was based on explicitly matching the first '2q-1' moments of the transfer function using pade's approximation. In the circuit structure, References [4~6] extended a π crosstalk analyzable model to a 4π model to accurately calculate noise, which include the aggressor distributed line characteristics. Based on the KCL law, Devgan[2] modeled each aggressor and victim net by a distributed RC model and obtained the maximum noise value under ramp signal. Later, extensions to his model were made by Martin to consider arbitrary input signals, while assuming the effect of parasitical coupled inductance. However, under the previous CMOS process, the coupled inductance was so negligible for noise that can be ignored. Thus, all above models were obtained based on RC circuits.

With the feature size of CMOS device shrinking to 90nm, parasitical inductance plays a significant role in determining the crosstalk noise and an RLC interconnect crosstalk model has become necessary. Therefore, References [10~13] introduced inductance into the 0.18μm CMOS process, and then References [10, 14] researched interconnect line optimization and gate delay in the 90nm CMOS process. However, for the mass produced 65nm CMOS process, we are still lacking a related study.

The paper presents a novel parallel RLC coupling interconnect analytical model based on the 65nm CMOS process, synthetically considering parasitical capacitive coupling and parasitical inductive coupling.

2 RLC parameter extraction

A coplanar interconnect section with a homologi-

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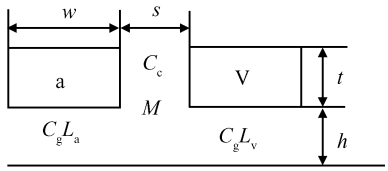

Fig. 1 Coplanar interconnect section

cal dimension is depicted in Fig. 1. w, t, l correspond to the width, thickness, and length of interconnect line, s is the space between adjacent lines, and h is the distance between wire and ground. In the 65nm CMOS process, traditional aluminum is replaced by a copper interconnect line with low k. Ignoring the skin effect, the interconnect resistance can be expressed as:

$$R_a = R_v = \frac{pl}{wt} \tag{1}$$

where p is the resistivity. For Cu, resistivity = 2.2$\mu\Omega$ · cm; For Al, resistivity = 3.3$\mu\Omega$ · cm.

Parasitical inductance is one of basic parasitical parameters in the 65nm CMOS process and plays a critical role in the transmission of high speed signals. Especially when the operating frequency increases and higher conductance materials are used, parasitical inductance has become the dominant factor in clock net resistance. Considering this, the parasitical inductance model needs to be modified according to advanced technology. The self and mutual inductances are respectively expressed as[9]:

$$L_s = \frac{ul}{2\pi}\left[\ln\frac{2l}{w+t} + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{2}$$

$$M = \frac{ul}{2\pi}\left[\ln\frac{2l}{s} - 1 + \frac{s}{l}\right] \tag{3}$$

where μ is the vacuum magnetic permeability and $\mu = 4\pi \times 10^{-7}$ H/m.

Referring to the extraction metrics of the 65nm CMOS parasitical capacitance in the Berkeley predictive technology model, the self and mutual capacitances in the 65nm CMOS interconnect are expressed respectively as[15]:

$$C_g = \varepsilon\left[\frac{w}{h} + 2.22\left(\frac{s}{s+0.70h}\right)^{3.19} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right] \tag{4}$$

Table 1 Typical interconnect dimensions and parasitical parameters in 65nm CMOS process

	Dimension/μm	RLC
Local	w = 0.10 s = 0.10 t = 0.20 L = 30 h = 0.20 k = 2.2	R = 33Ω, L = 34pH M = 32.4pH, C_g = 1.195fF C_c = 3.68fF
Intermediate	w = 0.14 s = 0.14 t = 0.35 L = 500 h = 0.20 k = 2.2	R = 224.5Ω, L = 0.81nH M = 0.79nH, C_g = 27.6fF C_c = 70.56fF
Global	w = 0.45 s = 0.45 t = 1.20 L = 1500 h = 0.20 k = 2.2	R = 61.1Ω, L = 2.4nH M = 2.34nH, C_g = 218.1fF C_c = 194.71fF

$$C_c = \varepsilon\left[1.14\left(\frac{t}{s}\right)\left(\frac{h}{h+2.06s}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s}\right)^{1.14} + 1.16\left(\frac{w}{w+1.87s}\right)^{0.16}\left(\frac{h}{h+0.98s}\right)^{1.18}\right] \tag{5}$$

where ε is the dielectric constant of SiO_2.

Based on the above RLC extraction methods, the typical interconnect dimensions and RLC parameters are presented in Table 1.

3 Distributed RLC crosstalk model

The distributed-coupled RLC interconnects with a coupled capacitance C_c per unit length, mutual inductance l_m, resistance r, self-inductance l, and ground capacitance C_g, respectively, are shown in Fig. 2. For noise coupling, the aggressor net is the net that switches state, whereas the victim net is quiet or maintains its present state. Through the Thevennin model[13], the aggressor driver can be modeled as a voltage source series with a resistance R_{th}, and the victim driver is a pure resistance R_s. The receivers of interconnect lines are modeled as capacitance loads $C_f(a)$ and $C_f(v)$. In order to make the RLC model close to the transmission characteristic, the number of unit RLC segments N is determined by the signal edge fastest rate change. Generally, the shortest delay ($T_d = \sqrt{LC}$) of unit RLC segments less than one in ten of rise (fall) time can satisfy the need. N can be obtained by

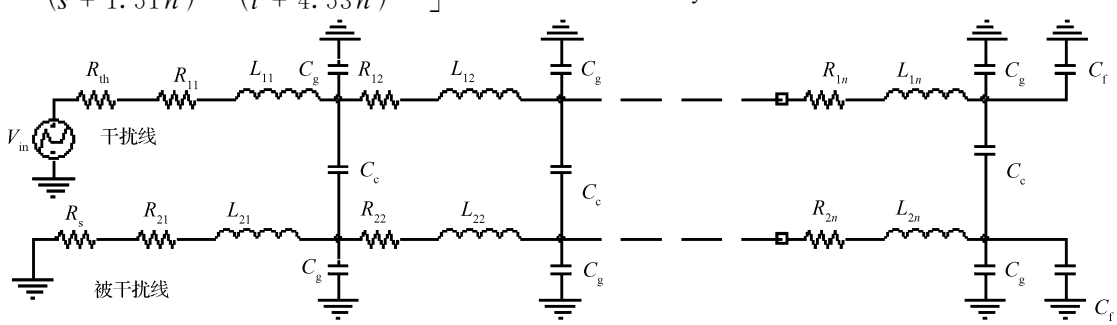

Fig. 2 RLC coupling interconnect model

$$N \geqslant 10\left(\frac{x}{T_r v}\right) \tag{6}$$

where x and v correspond to the length and speed of the interconnect, and T_r is the rise (fall) time of the input.

Applying KCL and KVL law to analyze a unit length RLC segment, then extending to the case with N aggressor and victim segments, we obtain the following matrix equation:

$$\begin{bmatrix} C_1 & -C_c & 0 & 0 \\ -C_c & C_2 & 0 & 0 \\ 0 & 0 & L_a & M \\ 0 & 0 & M & L_v \end{bmatrix} \begin{bmatrix} \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \\ \frac{di_1}{dt} \\ \frac{di_2}{dt} \end{bmatrix} =$$

$$\begin{bmatrix} \alpha & 0 & 0 & 0 \\ 0 & \alpha & 0 & 0 \\ -R_a & 0 & \beta & 0 \\ 0 & -R_v & 0 & \beta \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ b \\ 0 \end{bmatrix} \times V_{in}$$

where $C_1 = C_a + C_c$; $C_2 = C_v + C_c$; R_a/R_v: diagonal matrix ($N \times N$) of aggressor/victim resistance. L_a/L_v: diagonal matrix ($N \times N$) of aggressor/victim inductance. C_a/C_v: diagonal matrix ($N \times N$) of aggressor/victim capacitance. C_c/L_m: diagonal matrix ($N \times N$) of mutual capacitance/mutual inductance between aggressor and victim line. v_1/i_1: vector of node voltage/node current in the aggressor line. v_2/i_2: vector of node voltage/node current in the victim line. V_{in}: input to aggressor line. α, β and b: constant matrix ($N \times N$), described as follows respectively.

$$\alpha = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & -1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & -1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},$$

$$\beta = \begin{bmatrix} -1 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 1 & -1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & -1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix}, b = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix}$$

By substituting the constant matrix into the above matrix equation, vector i is removed, and we can obtain a voltage differential equation. Assuming all initial conditions are zero, invert the equation into a Laplace domain and change them, then v_1 and v_2 are expressed respectively as:

$$(s^2 A_{11} + sB_{11} - \beta) v_1(s) + (s^2 A_{12} + sB_{12}) v_2(s) = b v_{in}(s) \tag{7}$$

$$(s^2 A_{21} + sB_{21}) v_1(s) + (s^2 A_{22} + sB_{22} - \beta) v_2(s) = 0 \tag{8}$$

where $A_{11} = L_a \alpha^{-1} C_1 - M\alpha^{-1} C_c$, $A_{12} = -L_a \alpha^{-1} C_c + M\alpha^{-1} C_2$, $A_{21} = M\alpha^{-1} C_1 - L_v \alpha^{-1} C_c$, $A_{22} = -M\alpha^{-1} C_1 + L_v \alpha^{-1} C_c$, $B_{11} = R_a \alpha^{-1} C_1$, $B_{12} = -R_a \alpha^{-1} C_c$, $B_{21} = -R_v \alpha^{-1} C_c$, $B_{22} = R_v \alpha^{-1} C_2$ (matrix α^{-1} is inverse matrix of matrix α).

We assume the input to the aggressor is a saturated ramp signal of rise time T_r as given below, $V_{in} = \frac{V_{dd}}{T_r}[tU(t) - (t - T_r)U(t - T_r)]$, where $U(t)$ represents the step function.

For a ramp input, we may expand $v_1(s)$ using the series:

$$v_1(s) = v_{10} s^{-1} + v_{11} + v_{12} s + v_{13} s^2 \cdots + v_{1n} s^{n-1} \tag{9}$$

Similarly, the voltage $v_2(s)$ can be represented as:

$$v_2(s) = v_{20} + v_{21} s + v_{22} s^2 + v_{23} s^3 \cdots + v_{2n} s^n \tag{10}$$

These specific forms for the series have been chosen to be consistent with the final value theorem. When a ramp input with amplitude V_{dd} is applied to the aggressor, the response $V_1(t)$ on the aggressor will converge toward V_{dd} as $t \to +\infty$. Similarly, the response $V_2(t)$ will approach to zero as its finial value is $t \to +\infty$.

By substituting Eqs. (9), (10) into Eqs. (7), (8), and using the coefficients of all S^i on the left hand side that are the same as those on the right hand side, we obtain v_{1i}:

$$v_{10} = \beta^{-1} b v_{dd} \qquad v_{11} = \beta^{-1} B_{11} v_{10}$$

$$v_{12} = \beta^{-1}[A_{11} v_{10} + B_{11} v_{11} + B_{12} v_{20}]$$

$$v_{1i} = \beta^{-1}[A_{11} v_{1(i-2)} + B_{11} v_{1(i-1)} + A_{12} v_{2(i-3)} + B_{12} v_{2(i-2)}]$$

Similarly, the value of v_{2i} can be solved:

$$v_{20} = \beta^{-1} B_{21} v_{10} \qquad v_{21} = \beta^{-1}[A_{21} v_{10} + B_{21} v_{11} + B_{22} v_{20}]$$

$$v_{22} = \beta^{-1}[A_{21} v_{11} + B_{21} v_{12} + A_{22} v_{20} + B_{22} v_{21}]$$

$$v_{2i} = \beta^{-1}[A_{21} v_{1(i-1)} + B_{21} v_{1i} + A_{22} v_{2(i-2)} + B_{22} v_{2(i-1)}]$$

In order to obtain a closed form for crosstalk $V_2(t)$, consider its response to a ramp input. For $t \to 0$, $V_2(t)$ is zero and for $t \to +\infty$, $V_2(t)$ is zero. Using the initial and final value theorems, the following voltage function is appropriate.

$$V_2(s) = \frac{a_0 + a_1 s \cdots + a_{n-2} s^{n-2}}{1 + b_1 s \cdots + b_{n-1} s^{n-1} + b_n s^n} \tag{11}$$

Focusing on system stability and computational efficiency, we choose a second-order crosstalk model of the following form:

$$V_2(s) = \frac{a_0}{1 + b_1 s + b_2 s^2} \tag{12}$$

$$a_0 = v_{20j} \tag{13}$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} v_{20j} & 0 \\ v_{21j} & v_{20j} \end{bmatrix}^{-1} \times \begin{bmatrix} -v_{21j} \\ -v_{22j} \end{bmatrix}$$

(j represents the j th on the line) (14)

which has the inverse Laplace transform:

$$v_2(t) = c_1 \times e^{-t/k_1} + c_2 \times e^{-t/k_2} \tag{15}$$

where $1/k_1$ and $1/k_2$ are the poles of the crosstalk

voltage function. Using MATLAB for $V_2(t)$, we obtain the time-domain waveform of crosstalk noise, and the noise peak voltage and peak time are acquired as follows.

$$v_{2\max} = c_1 \times e^{-t_m/k_1} + c_2 \times e^{-t_m/k_2} \quad (16)$$

4 Model verification and discussion

The proposed RLC model has been tested by comparing its result with those obtained from Hspice. The source resistance and load capacitance are 100Ω and 50fF. The crosstalk noise based on the RLC model in the 65nm CMOS process is computed using a ramp input rise of 100ps and an amplitude of 0.75V (which is a typical voltage). According to the typical interconnect line dimension and parasitical parameters listed in Table 1, Table 2 shows the verification results of SPICE simulations and the data obtained from our RLC analyzable model. The relative error compared to SPICE is also presented for the 65nm CMOS process. Not only for local interconnect between logical gates, but also for global interconnect on-chips, the proposed model has good accuracy compared to Hspice. The average error magnitude is less than 2.5%, significantly more accurate than the model proposed in Ref. [13], for which the corresponding error is 10%.

Table 2 Comparison of noise as computed by circuit stimulation and the proposed model

	RLC $V_{\max}$/mV	Hspice $V_{\max}$/mV	Error/%
Local	3.299	3.3065	−2.30
Intermediate	101.3	103.085	−1.73
Global	127.6	130.664	−2.34

5 Conclusion

In this paper, we present an efficient interconnect crosstalk RLC analyzable model for the capacitive and inductive crosstalk computation in the 65nm CMOS process. Based on function approximation and model order reduction, we derive a closed-form expression and the time-domain waveform of crosstalk noise. For various interconnect coupling sizes, the proposed RLC coupling interconnect analytical model enables the estimation of the crosstalk voltage with less than 2.50% error compared with Hspice simulation in a 65nm CMOS process. It can be used as an algorithm for the computer-aided-design (CAD) of nanometer SOCs.

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一种 65nm CMOS 互连线串扰分布式 RLC 解析模型*

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摘要：基于 65nm CMOS 工艺，综合考虑电容耦合与电感耦合效应，提出了一种互连线耦合串扰分布式 RLC 解析模型.采用函数逼近理论与降阶技术，在斜阶跃输入信号下，提出了被干扰线远端的串扰数值表达式.基于 65nm CMOS 工艺，对不同的互连耦合尺寸下的分布式 RLC 串扰解析模型和 Hspice 仿真结果进行了比较，误差绝对值都在 2.50%内，能应用于纳米级 SOC 的计算机辅助设计.

关键词：纳米 CMOS；互连耦合串扰；分布式 RLC 解析模型；参数提取；函数逼近

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