Simulation of Gate-All-Around Cylindrical Transistors for Sub-10 Nanometer Scaling

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Abstract: A gate-all-around cylindrical (GAAC) transistor for sub-10nm scaling is proposed. The GAAC transistor device physics, TCAD simulation, and proposed fabrication procedure are reported for the first time. Among all other novel FinFET devices, the gate-all-around cylindrical device can be particularly applied for reducing the problems of the conventional multi-gate FinFET and improving the device performance and the scale down capability. According to our simulation, the gate-all-around cylindrical device shows many benefits over conventional multi-gate FinFET, including gate-all-around rectangular (GAAR) devices. With gate-all-around cylindrical architecture, the transistor is controlled by an essentially infinite number of gates surrounding the entire cylinder-shaped channel. The electrical integrity within the channel is improved by reducing the leakage current due to the non-symmetrical field accumulation such as the corner effect. The proposed fabrication procedures for devices having GAAC device architecture are also discussed. The method is characterized by its simplicity and full compatibility with conventional planar CMOS technology.

Key words: gate-all-around cylindrical transistor; device physics; TCAD simulation; fabrication procedure
EEACC: 2550
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2008)03-0447-11

1 Introduction

CMOS processes and technology at reduced gate lengths with conventional CMOS device have increasing difficulty in maintaining high drive currents with low off-current leakage and threshold voltage stability. The short-channel effect becomes a big hurdle to further scale down conventional CMOS devices. This results in a degradation of the device performance and determines the limits of miniaturalization. It is important for the transistors with nanoscale physical gate length that the channel conductance is controlled predominantly by the gate electrode instead of the drain electrode. For SOI devices, this is achieved by reducing the silicon body thickness from partial depletion mode to full depletion mode. Double gate transistors[1], tri-gate transistosr[2], and omega FinFETs[3] are alternative device structures with excellent short channel control ability.

Figure 1 illustrates a simplified diagram showing the evolution of device structures from a series of gate structure cross-sections for various evolved multi-gate devices in terms of their equivalent number of gates, from traditional bulk single gate MOSFET to double gate transistor, tri-gate transistor, gate-all-around rectangular (GAAR) transistor, and the gate-all-around cylindrical (GAAC) transistor. In this work, we propose a GAAC transistor device for sub-10nm scaling. The GAAC device physics, TCAD simulation, and proposed fabrication procedure are reported for the first time.

2 GAAC device architecture and device physics

The simplified perspective view of a gate-all-around cylindrical semiconductor device architecture is shown in Fig. 2. The device includes an SOI wafer substrate that consists of an SOI layer, a buried oxide layer and a bottom substrate, a first insulation layer overlaying the substrate, and a semiconductor cylindrical wire overlying the first insulation layer. The device further includes a source region within the first end section and a drain region within the second end section. Additionally, the device includes a channel region within the middle section. The channel region connects the source region and the drain region and is a cylindrical shape with a radius and a length. The device further includes a second insulation layer surrounding the cylindrical channel region. Moreover, the device includes a gate electrode overlaying the second insulation layer all around the channel region and overlaying the first insulation layer along the direction that is substantially perpendicular to the channel direction. The ultimate gate-all-around cylindrical

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Received 17 September 2007, revised manuscript received 6 November 2007

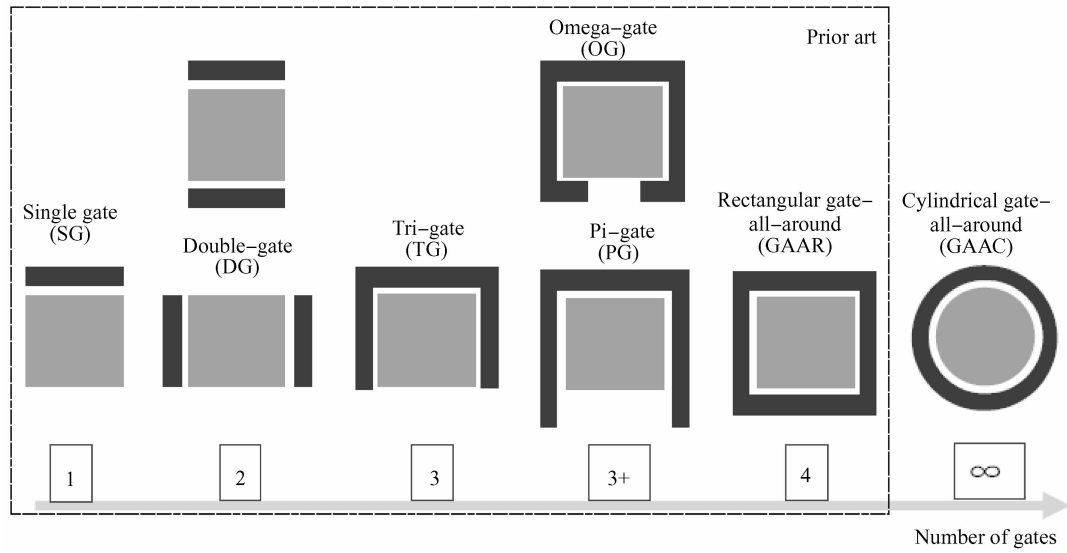


Fig. 1 Schematic cross-sections of the multiple-gate devices classified as a function of the "equivalent gate number" (EGN) From left to right: single gate, double-gate, tri-gate, pi-gate, omega-gate, rectangular gate-all-around, and cylindrical gate-all-around structures.

device implements a physical oxide with a large bandgap to isolate the gate from the conducting channel. By applying biased gate voltages to control the semiconductor channel and form a channel inversion layer, the device produces channel current when the drain electrode is also biased.

The device as illustrated has various characteristics, which include that the channel region of the semiconductor wire has an ideal cylinder shape with a length of L and a diameter of $2a$; that the gate is a metal gate with a bias voltage V_G applied; that the gate insulation layer is a high-k oxide; that the channel region is a p-type silicon; That the source region is N^+ implanted and is grounded; and that the drain region is N^+ implanted with bias voltage V_D applied. The bias voltages V_G applied to the gate electrode helps create a channel inversion layer that is triggered at a certain threshold. A current flow is produced from the source region across the channel region to the drain region. The electric field inside the channel can be modulated by the applied gate bias V_G to control the drain current. The total channel current flow from source to drain can be expressed by:

$$I_D = \frac{2\pi a}{L}\mu_n C_o\left\{\left(V_G - 2\Psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\times \frac{\sqrt{2\varepsilon_s eN_A}}{C_o}\left[(V_D + 2\Psi_B)^{3/2} - (2\Psi_B)^{3/2}\right]\right\} \quad (1)$$

where $\Psi_B = \frac{kT}{e}\ln\left(\frac{N_A}{n_i}\right)$; a: silicon cylinder radius; L: gate length; C_o: gate oxide capacitance per area; N_A: density of acceptor impurity atoms; n_i: intrinsic concentration of electrons; μ_n: electron mobility; k: Boltzmann's constant; e: electronic charge; ε_s: dielectric constant; and V_D and V_G are the voltages applied to the drain and the gate, respectively.

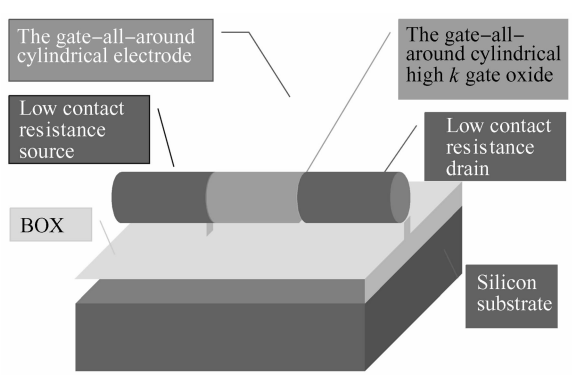


Fig. 2 Simplified perspective view of a gate-all-around cylindrical semiconductor device architecture

3 GAAC device 3D device TCAD simulation

Sub-threshold conduction in a gate-all-around cylindrical device is governed by the potential distribution in the entire device. The Synopsys 3D Devise and Dessis TCAD simulation tools were used in our simulations. A floating silicon body is applied to act as the device channel, with gate dielectrics and metal gate wrapped around. S/D to gate overlap is zero. The main dimension and device simulation parameters are listed in Table 1. A hydrodynamic model is applied in case ballistic transport takes place and velocity over shoots. Since high-k dielectric is applied, gate tunneling is ignored to save computation time.

Table 1　Fully encapsulated FinFET structure and parameters used for simulation

Channel length	10nm	Channel thickness	10nm
Gate oxide thickness	1nm	Gate oxide to S/D	Non-overlapping
Channel doping	10^{18} cm^{-3}	S/D doping	10^{20} cm^{-3}
Gate work function	5.5eV	V_{dd}	0.7V

Table 2　Electrical properties for fully encapsulated FinFET with different shapes in cross section

	S/(mV/dec)	DIBL	V_{ti}/V	V_{tsat}/V	I_{on}/μA	I_{off}/nA
Circular	107	0.22	0.414	0.268	155.800	0.303
Octangular	120	0.29	0.391	0.205	109.100	1.48
Rectangular	123	0.30	0.375	0.183	117.900	2.61

3.1　Corner effect

Three types of geometry in the channel region are simulated for comparison: circular (infinite), octuple, and quadruple. The thickness of the channel region is the same in all cases (10nm). The circular gate device exhibits the best performance, as shown in Table 2. It has the highest V_t and I_{on} and the lowest I_{off}. More importantly, its sub-threshold performance is much better than the other two because of the uniformity of gate dielectrics around the channel. As shown in Fig. 3, dielectrics thickness is higher at corners in the quadruple and octuple cases, but uniform in the circular case (which does not have corners). Though the perimeter is larger in the angled case, the loss in gate capacitance leads to larger trade off in gate control. As described in Eq. (2), as T_{ox} increases, sub-threshold swing degrades. Figure 4 shows that there is more electrostatic potential drop along the angled edge in the quadruple case than in the octuple case. The electrostatic potential distribution is uniform in the circular case. The results suggest circular is most suitable for fully encapsulated FinFET. Dielectric thickness non-uniformity is the major cause of device degradation. From the process point of view, angled edges should be avoided to prevent high dielectrics thickness in these regions during deposition or oxidation.

$$S = 2.3\frac{k_B T}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \tag{2}$$

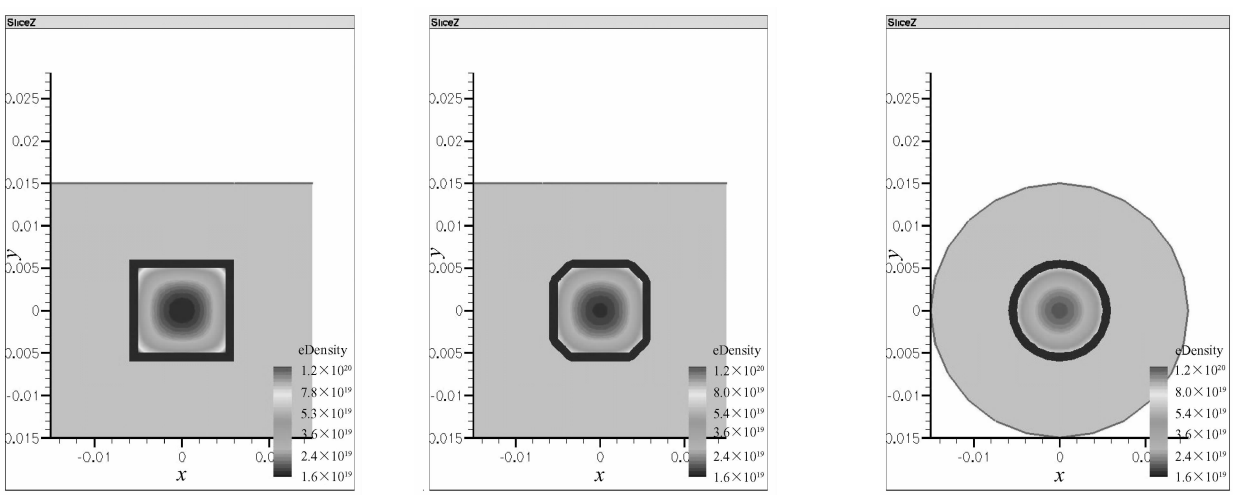


Fig. 3　Electron density for fully encapsulated FinFET with different shapes in cross section

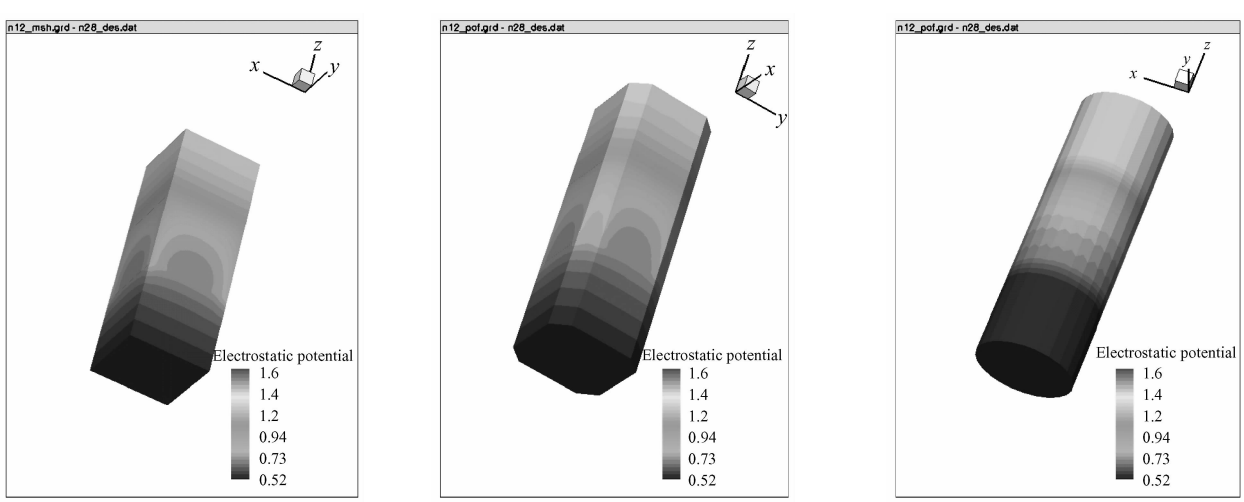


Fig. 4　Electrostatic potential for fully encapsulated FinFET with different cross sections

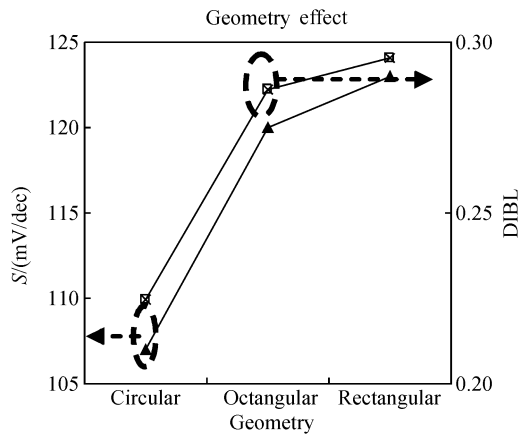


Fig. 5 Sub-threshold swing and DIBL for fully encapsulated FinFET with different cross sections

3.2 Gate enclosure effect

As illustrated in Fig. 3, the effective gate number for omega gate FinFET is 3+, and is infinite for fully encapsulated FinFET. In our simulation, omega FinFETs[4] with gate gaps at 0.5, 5, and 8nm together with a fully encapsulated FinFET are used for comparison. As the gap shrinks, device performances are improved, as shown in Table 3. Figure 6 shows that the channel electron density near the gate gap region is much less than that away from the gap. Thus, the I_{dsat} reaches to its highest point with the gate gap closed. This shows that the short channel effects improve as the gate enclosure increases because the drain electric field line penetrating into the channel region is successfully shielded, as shown in Fig. 7[5].

Table 3 Electrical properties for fully encapsulated FinFET with different gate gaps

Spacing/nm	S/(mV/dec)	DIBL	V_{ti}/V	V_{tsat}/V	I_{on}/μA	I_{off}/nA
no	123	0.30	0.375	0.183	117.900	2.61
0.5	125	0.32	0.368	0.161	119.300	4.60
5	137	0.38	0.346	0.100	112.800	18
8	150	0.46	0.318	0.022	109.3	78

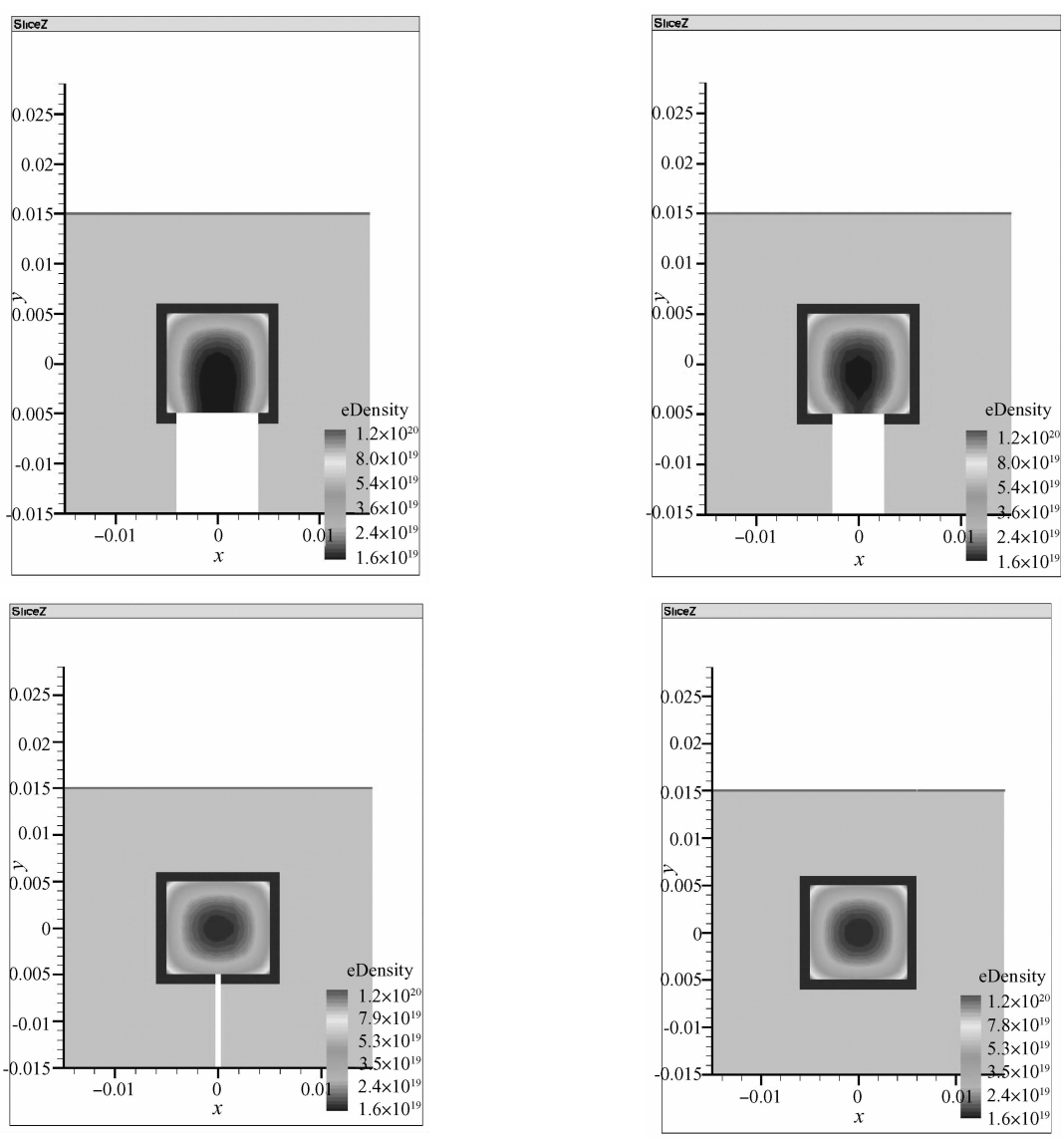


Fig. 6 Electron density for fully encapsulated FinFET with different gate gaps

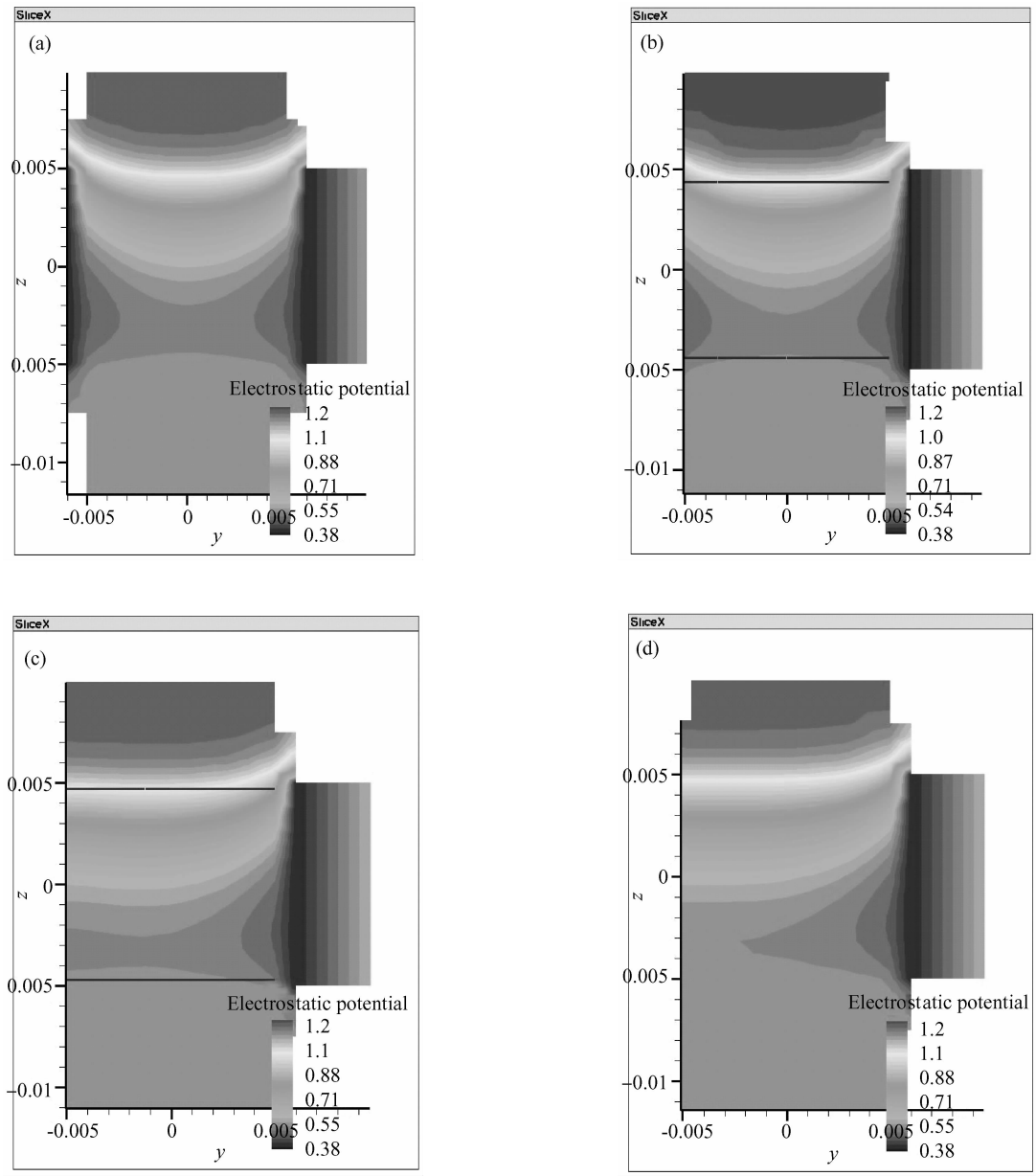


Fig. 7　Electricstatic potential for fully encapsulated FinFET with different gates　(a) Gap = 0nm; (b) Gap = 0.5nm; (c) Gap = 5nm; (d) Gap = 8nm

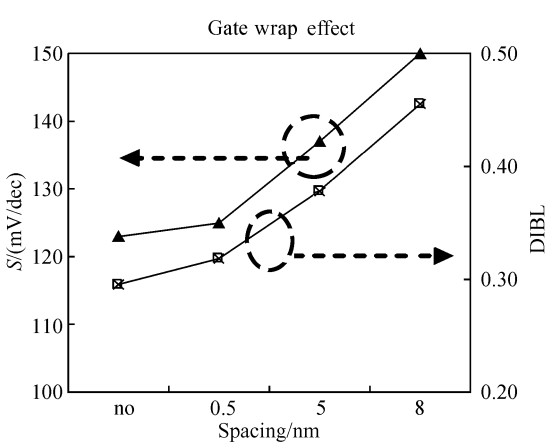


Fig. 8　Sub-threshold swing and DIBL for fully encapsulated FinFET with different gate enclosures

3.3　Channel doping effect

Table 4 and Figure 9 show that the device performance is not obviously improved as channel doping is reduced, but the DIBL and sub-threshold swing in the non-doped channel are slightly reduced compared to the heavily doped channel. There are two factors that dominant device performance as channel doping

Table 4　Electrical properties for fully encapsulated FinFET and FinFET with different channel dopings

Ch doping /cm^{-3}	S/(mV/dec)	DIBL	V_{ti}/V	V_{tsat}/V	I_{on}/μA	I_{off}/nA
1.00×10^{18}	107	0.22	0.413	0.269	156.000	0.3
1.00×10^{15}	113	0.24	0.395	0.242	119.000	0.5
0	103	0.21	0.422	0.287	98.000	0.1

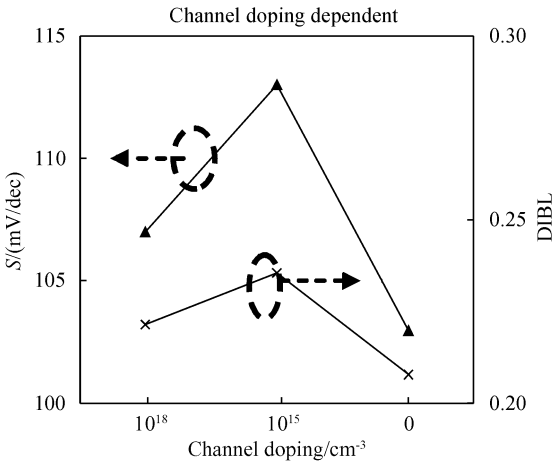


Fig. 9 Sub-threshold swing and DIBL on fully encapsulated FinFET with different channel dopings

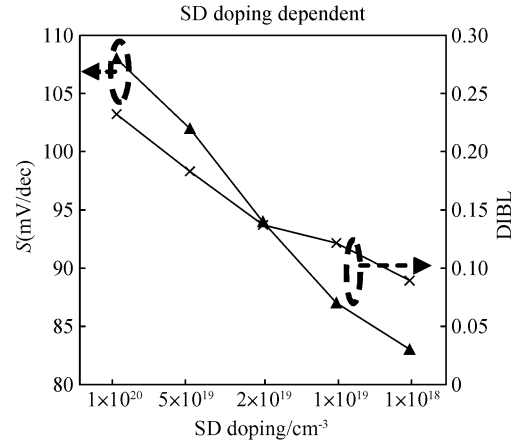


Fig. 10 Sub-threshold swing and DIBL for fully encapsulated FinFET with different channel dopings

varies. One is the flat band shift due to channel doping: as channel doping drops, the flat band shifts negatively and leads to a drop in V_t and a rise in I_{off}. With the decrease of channel doping, the depletion thickness increases and the sub-threshold performance is improved. A non-doped channel is usually used in fully-depleted SOI devices to reduce surface scattering of carriers with the scaling down of the channel thickness[6].

3.4 Source drain doping effect

The source drain doping dependence of device performance is more obvious than that of channel doping. As the source drain doping (non-doped channel experiment) decreases, sub-threshold swing, I_{off}, and DIBL greatly improve (Table 5, Figure 10, channel is intrinsic silicon). The only trade-off is I_{on}.

3.5 Gate oxide thickness effect

To avoid mobility degradation and achieve better I_{on}, intrinsic silicon (non-doped) is used as a channel. The device is naturally depleted according to Eq. (3). To achieve better short channel and sub-threshold performance, T_{ox} must be reduced according to Eq. (2). Once C_{ox} is improved, the total sub-threshold swing will be reduced. Table 6 and Figure 10 show that when T_{ox} is decreased, device performance is greatly improved. Figure 11 shows that in the non-doped channel and the heavily doped channel (10^{18} cm^{-3}), there is great improvement.

$$W_{dep} = \sqrt{4\varepsilon_{Si}\Psi_F / qN_a} \tag{3}$$

Table 5 Electrical properties for fully encapsulated FinFET and FinFET with different S/D dopings (non-doped channel)

SD doipng /cm^{-3}	S/(mV/dec)	DIBL	V_{ti}/V	V_{tsat}/V	I_{on}/μA	I_{off}/pA
1.00×10^{20}	108	0.23	0.413	0.262	101.000	139
5.00×10^{19}	102	0.18	0.438	0.319	87.000	40.1
2.00×10^{19}	94	0.14	0.467	0.378	61.600	3.73
1.00×10^{19}	87	0.12	0.487	0.408	42.300	1.19
1.00×10^{18}	83	0.09	0.508	0.450	9.100	0.296

Table 6 Electrical properties for fully encapsulated FinFET and FinFET with different T_{ox} (non-doped channel)

Ch doipng	T_{ox} /nm	S/(mV /dec)	DIBL	V_{ti}/V	V_{tsat}/V	I_{on}/μA	I_{off}/pA
0	1	103	0.20	0.422	0.289	97.700	4.86
	0.5	84	0.13	0.463	0.380	111.000	3.40
	0.1	74	0.08	0.491	0.442	148.000	11.5

3.6 Performance comparison on different FinFETs

Figure 12 shows the simulated plot of source to drain current flow I_D at different gate voltage V_G biases. For the curves with the solid line and dashed line, the drain voltage bias of 0.05 and 0.8V are applied, respectively. For either case with different drain biases, as the gate separation width (SPA) is reduced from 5 to 1 nm and to 0, the drain current de-

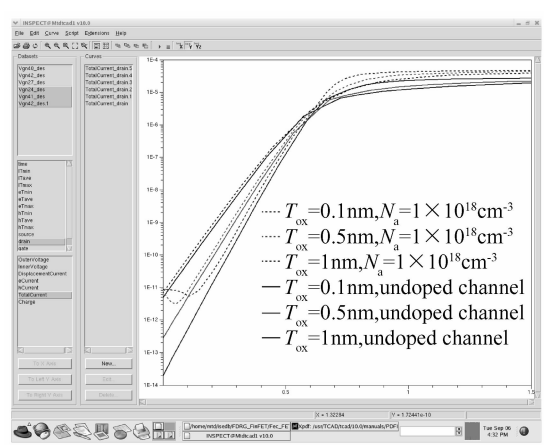


Fig. 11 I_d-V_g curves for fully encapsulated FinFET with different T_{ox} (V_d = 0.05V)

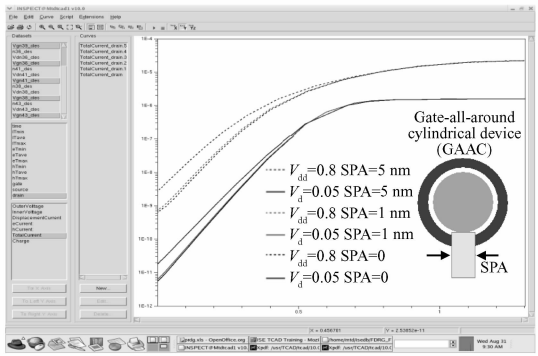


Fig. 12　Simulated plot of I_D versus V_G at different gate SPA

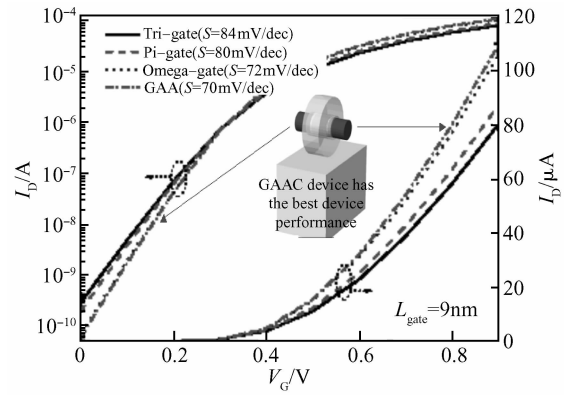


Fig. 13　Simulations on sub-threshold characteristics for four kinds of device architectures (Tri-gate, Pi-gate, Omega-gate and GAAC device)　V_D = 0.5V, T_{Si} = W_{Si} = 4nm, d_{ge} = 0.8nm for Pi-gate and L_{bgate} = 0.4nm for Omega-gate, L_{gate} = 9nm

creases at a fixed sub-threshold gate voltage. The drain current decreasing as a function of SPA decrease indicates a better performance in terms of off-current leakage for GAA type than others with a gate gap. This proves the clear advantage of the GAAC device over the conventional multi-gate devices in terms of short-channel effect suppression.

Figure 5 is a simplified diagram illustrating drain current as a function of gate voltage for a GAAC with that of rectangular tri-gate, pi-gate, or omega-gate device, respectively. As shown in Fig. 5, a horizontal axis represents the bias voltage applied to the gate. The vertical axis represents the drain current on a logarithmic scale. A second vertical axis on the right side represents the same current in linear scale. Curves are shown in the legend and represent the results for the rectangular tri-gate device, pi-gate device, omega-gate device, and GAAC device under fixed conditions, respectively. The fixed conditions are the same for all devices above, including a 0.5V bias applied to the drain region, a channel width of 4nm (diameter of 4nm in GAAC), a gate length of 9nm, and other intrinsic physical properties of the material. The gate separation is 0.8nm for the pi-gate device and 0.4nm for the omega-gate device. In comparison, a GAAC device has no gate separation (SPA = 0). The GAAC device shows a lower leakage current than the other devices, with the sub-threshold swing value S = 70, 72, 80, and 84mV/dec, respectively, indicated within the bracket in the legend. The GAAC device also shows the highest drain current with the same applied gate voltage and the same gate dimensions, demonstrating a better performance of the GAAC device over the conventional multi-gate devices.

Deca-nanometric FinFETs (with a channel encapsulated by gate structure) are simulated. Device performance is found to have high correlation with device configuration. A circular channel cross-section is better than polygonal, and the channel should be encapsulated by the gate as fully as possible to ensure the channel controllability.

To avoid mobility degradation, intrinsic silicon is recommended to act as a channel. A lightly doped source drain will lead to better device performance, especially sub-threshold swing and DIBL. Meanwhile, reducing S/D doping has a trade off in I_{on}. To aggressively improve short channel effect and sub-threshold performance, T_{ox} should be further reduced. The recommended device for manufacturing is a circular gate fully encapsulated FinFET with $T_{ox} < 0.5$nm, a non-doped channel, and source drain doping $< 10^{20}\,cm^{-3}$.

The GAAC device can be particularly applied for reducing the problems of the conventional multi-gate fin field effect transistor (FinFET) and improving the device performance and the scale down capability. According to the simulation, the GAAC device shows many benefits over convention multi-gate FinFETs, including the gate-all-around rectangular (GAAR) type device. With a GAAC architecture, the transistor is controlled by an essentially infinite number of gates surrounding the entire cylinder-shaped channel. For example, the electrical integrity within the channel is improved by reducing the leakage current due to the non-symmetrical field accumulation such as the corner effect.

4　GAAC device fabrication procedure

Recently, gate-all-around (GAA) devices have been developed in which the gate region surrounds the channel region completely without leaving a gap as previous multi-gate devices did. However, due to process limitations, the channel regions of these GAA type devices are rectangular. In other words, the GAA device is an equivalent 4-gate type device called a gate-all-around rectangular (GAAR) device. When making a GAAR type device, there are some process difficulties existing for forming a channel bridge due

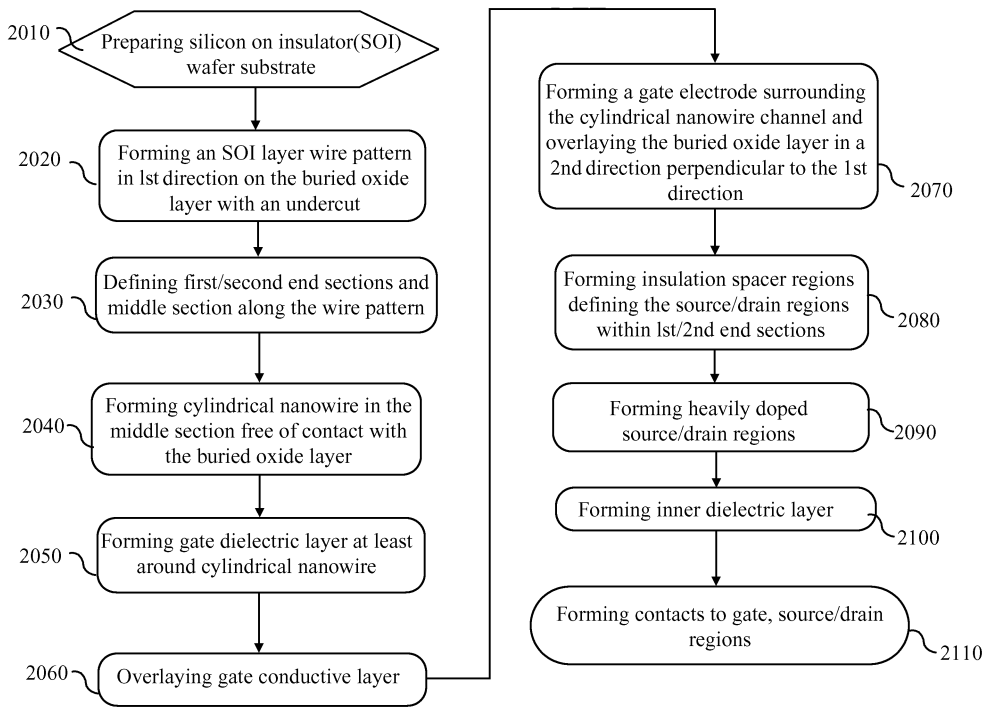


Fig. 14 Proposed fabrication process flow for making gate-all-around cylindrical (GAAC) devices

to the relative large width of the channel structure. For example the well-established planar CMOS process technology cannot be applied to form the required GAAR structure in some proposed designs. Additionally, the electrical field in the rectangular channel is still not uniform due to the unavoidable corner effect. The wire pattern includes a first end section, a middle section, and a second end section. The method further includes forming an undercut structure of the buried oxide layer underneath the wire pattern and selectively removing the undercut structure underneath the middle-section to form a cavity having a first length and a first height. Additionally, the method includes forming a channel region by shaping the middle section above the cavity to a substantially cylindrical shape. The proposed fabrication process flow for devices having gate-all-around cylindrical (GAAC) device architecture is shown in Fig. 14. The method is characterized by its simplicity and full compatibility with conventional planar CMOS technology.

The detailed fabrication procedures are described schematically below. Figures 15 (a) and (b) illustrate a perspective view and a side view (cutting along the A-A' plane) of a portion of an SOI wafer, respectively.

Figures 16 (a), (b), and (c) show a simplified method for forming a wire pattern of the SOI layer on the buried oxide layer for making device with a GAAC architecture.

Figures 17 (a), (b), and (c) show a simplified method for defining the first/second end sections and the middle section of the wire pattern of the SOI layer on the buried oxide layer for making a device with a GAAC architecture. As shown in Fig. 17 (a), the unexposed resist patterns remain to cover the two end sections of the wire pattern, including portions of the undercut structure and the surface of the etched oxide layer on both sides thereof. Thus, three regions are defined along the wire pattern. Specifically, the undercut portion possesses the same length of L as the middle section of the wire pattern. Nevertheless, at the end of the process, the undercut portions are still covered by the resist layers, while the undercut portion is revealed. Referring to Fig. 17 (a), the region not covered by the resist layer records a pattern registry that will be used for defining a gate region in one of the later processes. After that, a cylindrical shaped nanowire with a cavity underneath is formed.

Figures 18 (a), (b), and (c) show a simplified method for forming cylindrical nanowire with no contact to the buried oxide layer for making a device with a gate-all-around cylindrical nanowire architecture. A lateral oxide etching process is performed using buffered oxide etchant (BOE) to remove selectively the revealed undercut portion with rest of the surface covered by etch-stop layer mask. Due to the narrowed width of the undercut structure created in an earlier process, this oxide etching process becomes greatly simplified. This process results in the formation of a cavity, as shown in Fig. 18 (c). The cavity has the same length L as the middle section. Silicon

plasma etching followed by a hydrogen annealing process at 1000～1200℃ is performed to transform the middle section of the wire pattern into a substantially cylindrical shape by mass transportation around its periphery body. This hydrogen annealing process also eliminates damage to the wire body caused by the silicon etching process. The combination of the etching and annealing process provides a well controlled cylindrical radius r. A gate dielectric layer is formed covering the wire pattern at least around the cylindrical nanowire.

Figures 19 (a), (b), and (c) show a simplified method for a forming gate dielectric layer at least around the cylindrical nanowire for making a device with a GAAC nanowire architecture.

Figures 20 (a), (b), and (c) show a simplified method for a overlaying gate conductive layer for making a device with a GAAC nanowire architecture. Figures 21 (a), (b), and (c) show a simplified method for forming a gate electrode surrounding the cylindrical nanowire channel and overlaying the buried oxide layer in a 2nd direction perpendicular to the 1st direction for making a device with a GAAC nanowire architecture. Figures 22 (a), (b), and (c) show a simplified method for forming spacer regions and defining the source and drain regions for a device with a GAAC nanowire architecture. Figures 23 (a) and (b) show a simplified method for forming an inner dielectric layer for making a device with a GAAC nanowire architecture.

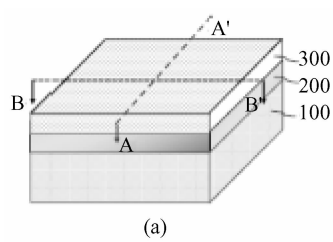


Fig. 15(a)

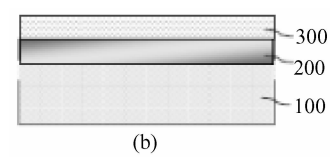


Fig. 15(b)

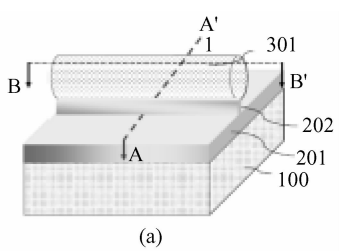


Fig. 16(a)

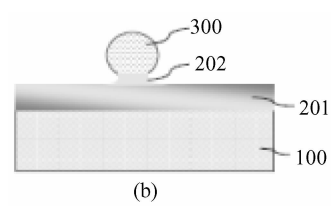


Fig. 16(b)

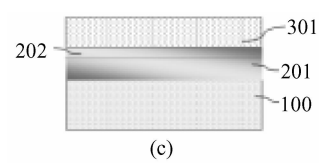


Fig. 16(c)

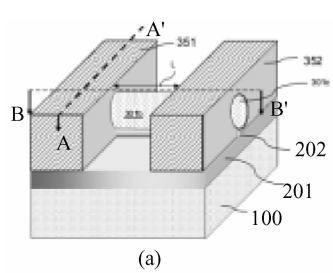


Fig. 17(a)

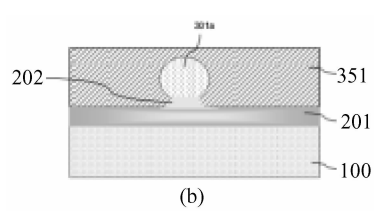
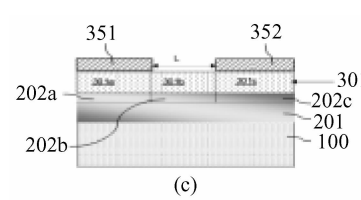


Fig. 17(b)



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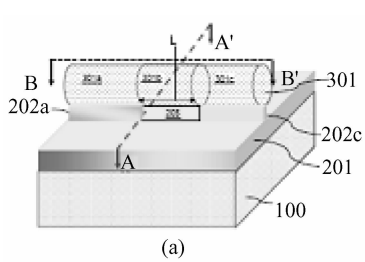
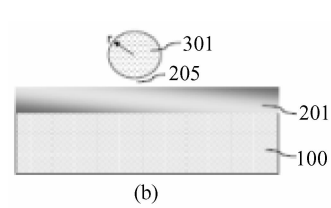


Fig. 18(a)



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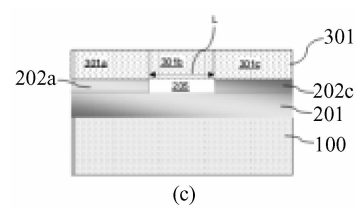

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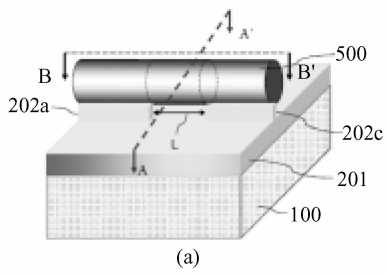


Fig. 19(a)

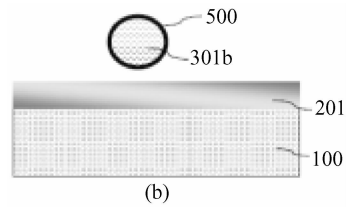


Fig. 19(b)

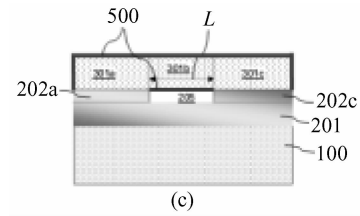


Fig. 19(c)

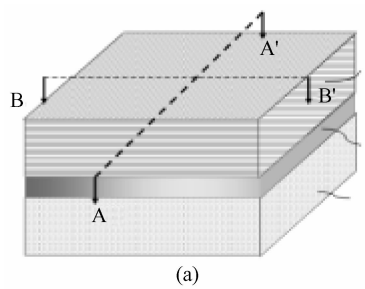


Fig. 20(a)

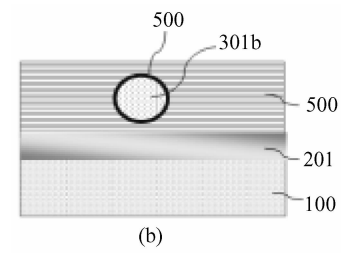


Fig. 20(b)

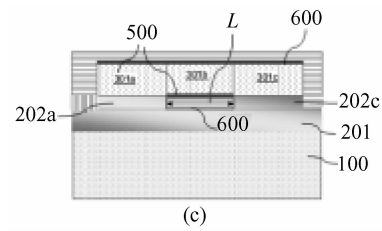
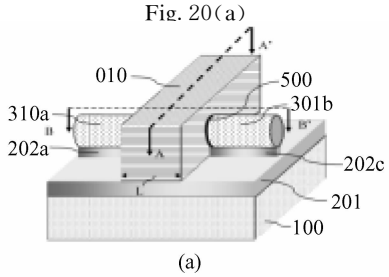


Fig. 20(c)



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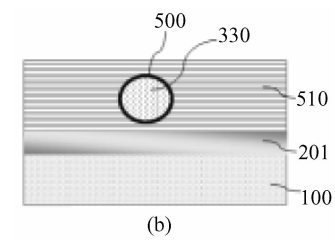

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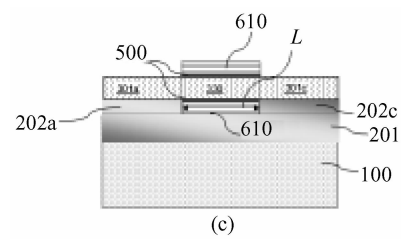

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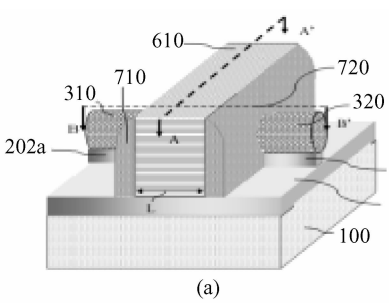

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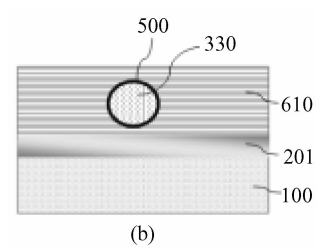

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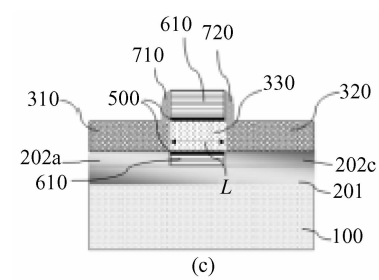

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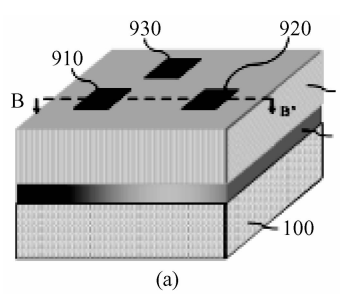

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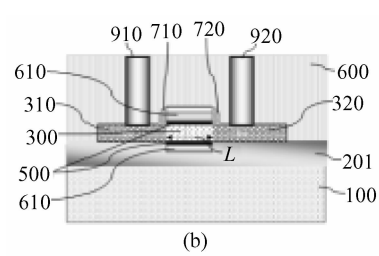

Fig. 23(b)

Figs. 15 (a), 16 (a), 17 (a), 18 (a), 19 (a), 20 (a), 21 (a), and 22 (a) are the simplified perspective views, illustrating the process steps in Fig. 14.

Figs. 15 (b), 16 (b), 17 (b), 18 (b), 19 (b), 20 (b), 21 (b), and 22 (b) are the simplified cross-sectional views taken along the A-A' plane of Figs. 15 (a), 16 (a), 17 (a), 18 (a), 19 (a), 20 (a), 21 (a), and 22 (a), respectively.

Figs. 16 (c), 17 (c), 18 (c), 19 (c), 20 (c), 21 (c), and 22 (c) are the simplified cross-sectional views taken along the B-B' plane of Figs. 16 (a), 17 (a), 18 (a), 19 (a), 20 (a), 21 (a), and 22 (a), respectively.

Fig. 23 (a) Simplified perspective view of an integrated circuit unit showing three contact pads for a GAAC device within an inner dielectric layer; (b) Simplified cross-sectional view on cutting along the B-B' plane of Fig. 23 (a).

5 Conclusion

We have proposed a gate-all-around cylindrical (GAAC) transistor device suitable for sub-10nm scaling. The GAAC transistor device physics, TCAD simulation, and proposed fabrication procedure have been reported for the first time. Among all other novel FinFET devices, the GAAC device can be particularly applied for reducing the problems of the conventional multi-gate fin field effect transistor and improving the device performance and the scale down capability. The proposed fabrication procedures for devices having GAAC device architecture are quite simple and fully compatible with conventional planar CMOS technology.

Acknowledgements The authors would like to thank Dr. Sean Xing and David Yuan from Synopsys for help in TCAD simulation.

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适用于按比例缩小至亚 10nm 的圆柱体全包围栅场效应管仿真

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摘要：提出了一种适用于按比例缩小至亚 10nm 的圆柱体全包围栅场效应管.报道了圆柱体全包围栅场效应管器件物理分析、技术仿真结果以及器件制作详细工艺流程.与其他常规鳍形场效应管器件(FinFET)相比，该器件特别适用于解决常规鳍形场效应管器件所面临的问题，进一步提高器件性能及按比例缩小能力.技术仿真结果显示，圆柱体全包围栅场效应管具备许多常规鳍形场效应管器件，其中包括长方体全包围栅场效应管所不具备的优点.就圆柱体全包围栅场效应管器件结构而言，该器件由无数多个将圆柱体形沟道全部包围的栅所控制.由于克服了由不对称场的积聚，如锐角效应所导致的漏电，器件沟道的电完整性得到很大改善.详细讨论了器件制作工艺流程，提出的工艺流程简单并且与常规 CMOS 工艺流程兼容.

关键词：亚 10nm 器件；圆柱体全包围栅场效应管；器件物理；器件工艺仿真
EEACC：2550
中图分类号：TN386　　**文献标识码**：A　　**文章编号**：0253-4177(2008)03-0447-11

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2007-09-17 收到，2007-11-06 定稿