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The Bipolar Field-Effect Transistor: I. Electrochemical Current Theory (Two-MOS-Gates on Pure-Base)*

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Abstract: This paper describes the bipolar field-effect transistor (BiFET) and its theory. Analytical solution is obtained from partitioning the two-dimensional transistor into two one-dimensional transistors. The analysis employs the parametric surface-electric-potential and the electrochemical (quasi-Fermi) potential-gradient driving force to compute the current. Output and transfer D.C. current and conductance versus voltage are presented over practical ranges of terminal D.C. voltages and device parameters. Electron and hole surface channel currents are present simultaneously, a new feature which could provide circuit functions in one physical transistor such as the CMOS inverter and SRAM memory.

Key words: bipolar field-effect transistor theory; MOS field-effect transistor; bipolar junction transistor; simultaneous hole and electron surface channel; volume channel; surface potential

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1 Introduction

The nanometer multiple-metal-oxide-gate silicon-thin-base (MOS) field-effect transistor (FET) could be a best candidate to replace the single-MOS-gate semi-infinite-thick-base bulk silicon FET, in order to extend the downward scaling into the deep nanometer range[1]. The double and triple MOS-gate FETs with rectangular-shape thin base are known as the FinFET due to its fish-fin-like geometry when many are connected in an array.

The bipolar nature of the experimental current-voltage (I-V) characteristics of recent nanometer double-gate thin-base silicon FinFETs reported by IMEC + Assignees in 2005[2] was just recognized by us in mid-2007[3]. The bipolar conduction in a FET or in the bipolar FET (We propose the use of the acronym BiFET, BFET or 2FET in this introductory paper.) was defined by us in Ref.[3], following but contrasting the historical usage of the term "unipolar" introduced in 1952[4] and "bipolar" in 1949[5] both by Shockley. Our broadened and application-specific device-physics-based definition given in Ref.[3] of the word "bipolar" for FETs contained the following features. (1) It denotes the simultaneous conduction by both electrons and holes in electrical conduction channels, at one set of voltages applied to terminals of a FET structure. (2) The electron and hole channels can be physically separated but connected at a boundary surface, in series or in parallel, or the channels can be physically located in the same region of the transistor structure, for examples, the surface, interface and volume channels. (3) These two carrier species and the many physical geometries, when combined, produce very many possible combinations of physically separated and connected electron and hole channels. (3.1) For example, it was recently noticed that the double-gate MOSFETs, such as the thin and nearly-pure base, silicon nanometer FinFETs[2],

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have six conduction channels between the two contacts (drain and source contacts) to the semiconductor base layer[3], consisting of two electron and two hole surface channels and one electron and one hole volume channel. (3.2) Similarly, there are four channels in the silicon WireFET with one surrounding gate (a surface and a volume electron and hole channel) and (3.3) there are six channels in the carbon nanotube FET, CNFET, with a conductor-core covered by a thin insulated sheath or gate-insulator, electrically separated from the surrounding conductor gate on the outer surface of the nanotube[3]. (3.4) For transistor structures having more than one drain and source contacts, the number of channels multiplies[3]. (4) Realization of multi-transistor circuit functions in one physical FinFET structure. (4.1) The CMOS inverter[3] and (4.2) the bistable SRAM memory function[3], and (4.3) other digital and analog signal processing functions. (5) For transistor structures having more than one drain and source contacts, the number of channels multiplies[3] and so is the number of circuit functions.

The cause of this delayed recognition of bipolar conduction in FETs originated from Shockley's 1952 invention of FET which he coined as a unipolar FET[4] (We propose the use of the acronyms UniFET, UFET or 1FET in this introductory paper.) because his elegant theory of the p/n-junction-gate FET (JGFET or JFET)[4] described the modulation of the conductance of majority carriers of a semiconductor by electrically controlling the electrical thickness of the majority-carrier-dominated conduction channel in the volume of the semiconductor (He neglected the diffusance or diffusion resistance or diffusion conductance due to diffusion current.). Thus, he needed to retain only one carrier species, the majority carrier, in his development of the novel JGFET theory and named it accordingly "A Unipolar 'Field-Effect' Transistor"[4]. The minority carrier was ignored. However, even in JGFETs, currents from diffusion-limited minority-carrier generation and recombination at traps or generation-recombination-trapping centers are important. This could be known to Shockley since it was analyzed by him in details three-years earlier in his 1949 bipolar junction transistor (BJT) theory[5], based on minority-carrier diffusion and electron-hole generation-recombination at traps in the bulk and at the surfaces and interfaces. This minority carrier current has been known later to JGFET designers as the source of leakage and standby currents when the JGFET is switched off to the subthreshold drain current range by applying sufficiently high reverse voltages to the gate-drain and gate-source p/n junctions to completely deplete the majority carriers in the volume conduction channel. This minority carrier current in the JGFET is just like the leakage current in the turned-off mode of the bipolar junction transistor which was invented and coined by Shockley in 1949[5].

There are similarities and differences in the control of the minority carrier current in BJT and MOSFET in the active or on mode. BJT conducts by increasing the minority carrier concentration in the base layer via lowering the potential barrier height of the p+emitter/n-base or n+emitter/p-base junction to inject the minority carriers into the base layer from the p+emitter or n+emitter, by conductively connecting a forward voltage to the two terminals of the p/n junction. MOSFET works the same way via minority-carrier injection by lowering the p/n-junction potential barrier, except that the forward bias is applied to the metal or highly conductive gate which is electrically insulated by a very thin insulator or oxide from the semiconductor (MIS or MOS) and which capacitively couples to the source or source-emitter p/n junction via the MIS or MOS capacitor.

Historically, the bipolar structure or multiple electrical conduction channels in an FET structure was recognized as early as 1970 by one of us. A bipolar FET, BiFET, was soon experimentally realized in silicon[6]. It contained a p-surface channel MOSFET (pMOSFET or pMOST) and an n-volume channel JGFET (nJGFET or nJFET). They are distributedly coupled by sharing the n-base-body of the pMOST with the n-volume-channel of the nJFET. It was fabricated in one of the first academic (University of Illinois at Urbana-Champaign) semiconductor device-research fabrication laboratories using the then standard silicon-based CMOS technology. The p-surface-inversion MOSFET was fabricated on an n-silicon layer on a 3-inch diameter p-type Si substrate. The n-Si layer was obtained by diffusion, ion-implantation, or

epitaxially growth.

The BiFET theory of the double-gate on thin pure-base FETs[3] was corroborated[3,7] with the recent experimental data reported in 2005-IMEC +Assignees[2]. The IMEC transistors were double-gate FinFETs on nearly-pure thin-silicon-base. They included the three types of contacts to the drain and source terminals of the thin base layer. These were recognized and defined by us as the three generic types of contact[3] to all BiFETs, following Shockley's 1949 definition[5]: the n-type (or electron-source), p-type (or hole-source), and ohmic-type. The ohmic-type of contact was coined by Shockley[5]. The quantitative description was given by us in Ref.[3] as a contact or interface with infinite sources and sinks of electrons and holes. It is mathematically defined by an infinite surface or interface electron-hole recombination-generation velocity $\sim 10^6$ cm/s, via an infinite density of interface traps $\sim 10^{14}$ traps/cm^2, both have fundamental limits, $\sim 10^7$ cm/s phonon scattering limited, and $\sim 10^{15}$ bonds/cm^2 bond-density limited. A p/n junction picture with a very high density of traps at the p/n interface was shown in Figs. 1 (c), 8 (a) and 8 (c) by Shockley in 1949[5], which he labeled "ohmic" and gave only some brief qualitative descriptions on what is meant "ohmic"[5]. Although understood by Shockley in 1949 and 1952[4,5], it has not been recognized until recently in 2007 55-years later, reported in Ref.[3], that the conduction type and geometry of the contacts have dominant influences on the electrical characteristics of the FET, regardless of the details of the make-up of the FET, whether p/n-junction-gate or metal/semiconductor-junction-gate or conductor/insulator insulated-MOS-gate, single, double or multiple gates, pure or impure base or body, and other geometric aspects and features. The contact effect is mathematically treated in the fifth report of this series on the generic (or x, y, z rectilinear geometry independent via partitioning) analytic theory of the Bipolar FETs with the MOS gates.

This paper is the first of a five-report series. It presents the derivation of the bipolar FET current-voltage (I-V) equations that were used in Refs.[3,7], from which families of current and conductance versus voltage curves are computed and presented for the example BiFET with two identical MOS gates on a thin pure-silicon-base. Fundamental aspects of the bipolar theory are also described concerning the electron and hole surface and volume channels. Our mathematical derivation, presented in this first paper, uses the classical method described in 1966-Sah-Pao[8,9], which calculated the current from the electrochemical potential-gradient or Shockley's quasi-Fermi potential-gradient[5], using the surface electrical potential (surface potential) at the gate-oxide/basewell-body interface as the independent variable.

The second paper of this series[10] uses the traditional classical method of drift and diffusion[11~14] to give the BiFET current-voltage and conductance-voltage characteristics. Both the electrochemical potential gradient current in this, the first paper, and traditional drift and diffusion current in the next, the second paper, are exact. And they are exactly equivalent as first introduced and also proven in Shockley's derivation given in 1949 for p/n junctions[5], one of which (the electrochemical potential or drift-diffusion theory) was often erroneously asserted as approximation to the other by some recent and past device-physicist authors. However, the drift-diffusion theory had experienced undue numerical difficulties in computing the drift-current-reduction term, due to the presence of impurity ions (impure base)[11] known in 1966-Sah-Pao as the "bulk-charge"[8,9], that had plagued generations of transistor theorists for four decades and compact model developers for three decades[11] because it required an analytical approximation, $E_X(x, y) \approx E_X(x=0, y)$,[11,13,14] to enable any analytical solutions and numerical integration. This analytical approximation was erroneously termed as "charge-sheet" by Brews in 1978[11] and his followers. Such numerical integration difficulties, however, are absent in the electrochemical or quasi-Fermi potential theory[8,9,11,13,14].

The proposed third paper describes the short channel theory[15] which is mandatory for pure-base and base with low-impurity-concentrations because the Debye screening length (pure base in the room temperature range in silicon is $\sim 25\mu$m to 30μm) is a thousand times larger than the dimensions of the nanometer FET in the present and future generations (135nm down to 45nm just

announced by Intel for its 2007-Winter delivery of processor chips). The proposed fourth paper describes the deviation of the unipolar theory from the bipolar theory[16] since the unipolar theory using the drift-diffusion approach is the popular one for developing compact models, in spite of the analytical complexity and numerical difficulty of the drift current term. The proposed fifth paper describes the contact theory[17] which completes the quantitative description (theory and numerical examples) of the generic transistor that contains all necessary parts. Other analyses for benchmark applications of this bipolar FET theory are also envisioned, such as the impure base, two not-identical gates, the capacitances, the frequency dependences of the small-signal equivalent circuit immittance parameters (including the distributed delay, interface traps, and higher order derivatives for noise characterization), the realistic spatial distribution of the impurity in the base, $P_{IM}(x, y)$, the intrinsic hot carrier effects (interband generation-recombination of secondary electrons and holes by energetic primary electrons or holes), and others, all within the context of the Partitioning Scheme to provide the generic or geometry-independent and mobility-independent benchmarks of the intrinsic transistor for compact model development by others, but their undertaken by us is indefinite.

This first paper will set up the presentation format for the computed results to be followed in the remaining four papers of this series. Thus, given in this first paper are sample families of transfer and output current-voltage (I_D-V_{GS}, I_D-V_{DS}) and conductance-voltage (g_{ds}-V_{GS}, g_{ms}-V_{DS}) characteristics. The curves will cover the practical ranges of terminal voltages (V_{DS} or V_{GS}) and physical parameters (gate-oxide and pure-base thicknesses, x_O and x_B). The curves will demonstrate that the Bipolar FET theory predicts and accounts for the simultaneous presence of both the electron and hole surface channels. This unique feature of the FinFET has been present but has not recognized in previous and recent experimental[2] and recent theoretical investigations[18]. The presence of multiple bipolar channels could provide circuit functions, such as CMOS inverter and SRAM memory, in one physical transistor[3,6,7] utilizing recent and future nanometer research-fabrication and production technologies.

2 Theory of Double-Gate on Pure-Base Transistors

2.1 Background

The BiFET equations governing the double-gate on thin pure-base MOS transistor, presented in Refs. [3,7], can be obtained from our analyses and solutions for the single-gate on thick impure-base[8,9,11~14], (1) by setting the impurity concentration to zero, $P_{IM}=0$, (2) by not setting the net space charge to zero, $\rho=q(P-N-P_{IM})=q(P-N)\neq 0$, at the remote or any boundary, known as the electrical charge neutrality condition, which is very important and missed by most recent investigators[18], because the carrier space charge concentrations could be very high and not equal, $qP\neq qN$, due to a large divergence of the electric field or electrical displacement, $\mathrm{div}\cdot\boldsymbol{D}\equiv\nabla\cdot\varepsilon\boldsymbol{E}=\varepsilon[(\partial E_X/\partial x)+(\partial E_Y/\partial y)]=\varepsilon[-(\partial^2V/\partial x^2)-(\partial^2V/\partial y^2)]=\rho=q(P-N)\neq 0$, just like the high-injection-level effects in BJT[11,19], with a difference in electron and hole mobilities and diffusivities in the quasi-neural base layer of the BJT, traditionally known for more than half of a century as ambipolar conduction in one physical region or mainly 1-D volume channel, in contrast to the conduction in multiple physical regions and channels in our present Bipolar FET, and (3) by moving the remote potential reference, for example, from the vacuum level into the base layer or base film, in this case of the identical double-gate, to a point (such as $y=0$) in the mid-base plane $x=x_B/2$ and by increasing it to a value of U_0 denoted by $U(x,y)=qV_I(x,y)/kT=U(x=x_B/2,y)=U_0(y)$ to account for high injection level, i. e. $N\gg n_i$ or/and $P\gg=n_i$, which could still be referenced to some point (x,y,z), selected by the analyst arbitrarily since the solution of the potential theory is uncertain by an additive constant.

We shall use our notation and rectangular coordinate for forty years, previously used in Refs. [7~11,13,14], with the gate-voltage induced electric field in the x-axis direction, and perpendicular to the surface channels at the two SiO_2/Si interfaces, on the thin base along the y-axis, and the base layer's source and drain contacts at $y=0$ and

$y = L$. Used by all followers[18] and also here, is our assumption of the x-independence[8,9,11,13,14] of the electron and hole quasi-Fermi or electrochemical potentials, $U_P(x,y) = U_P(y)$ and $U_N(x,y) = U_N(y)$, which is akin to the gradual approximation but a necessary condition for the Partitioning Method to decompose the 2-D problem into two 1-D problems that are amendable to analytical solutions. They were qualitatively justified[8,9,11] for thin surface inversion channels with currents flowing in the y-direction and no electron-hole generation-recombination-trapping centers in the bulk. This x-independence of the electrochemical potential for electrons and holes is at the heart of the Partition Technique for solving the 2-D MOSFET by two 1-D problems and it is related to the gradual approximation which was introduced by Shockley in 1952 for his master-class analysis of the Junction-Gate FETs[4], containing only the drift current, hence no electrochemical potentials which come from diffusion. The gradual approximation or gradual condition is not synonymous with physically long channels, which has been assumed by most subsequent FET theorists[11,12,18] as the basis of justification of their analyses of the FETs with physically long channels, which is untenable for pure-base or nearly pure-base due to the very large Debye carrier screening length (~25μm to ~30μm) compared with the nanometer even micrometer transistor dimensions. Physical length of the channel or region, long compared with its thickness or width, is neither the necessary nor the sufficient condition to meet the definition of the gradual approximation. The mathematically exact gradual conditions, as used by Shockley in 1952[4] to enable Partitioning, are defined by the two inequalities, given below in (1) and (2), in order to solve the 2-D electric potential problem described by the Poisson Equation for the electron and hole currents flowing from one terminal to the second terminal, through the device body, in the y-direction, which in the FETs are labeled as Source and Drain terminals, also coined by Shockley[4]. The two inequalities are: (1) in the emitter section or region, $|E_X(x,y)| \gg |E_Y(x,y)|$ and $|\partial E_X/\partial x| \gg |\partial E_Y/\partial y|$ and (2) in the collector section or region, $|E_X(x,y)| \ll |E_Y(x,y)|$ and $|\partial E_X/\partial x| \ll |\partial E_Y/\partial y|$. So in the emitter section or region specified by (1), the 2-D Poisson Equation is simplified, as the zeroth approximation, to the 1-D Poisson Equation in the x-direction, $\varepsilon(\partial E_X/\partial x) = -\varepsilon(\partial^2 V/\partial x^2) = \rho = q(P - N - P_{IM})$. Second order but still 1-D effects (no longer small in pure-base) are taken into account by including the dropped, $\varepsilon(\partial E_y/\partial y)$ term which is huge (~25%) for the drift current in the pure-base[10], but accounted for by the electrochemical potential gradient current employed here. Similarly, in the collector section or region specified by (2), the Poisson Equation becomes y-directed 1-D and given by $\varepsilon(\partial E_Y/\partial y) = -\varepsilon(\partial^2 V/\partial y^2) = \rho = q(P - N - P_{IM})$, although in the JGFET, this 1-D simplification of the 2-D collector region, named by Shockley as expop (extrapolated pinch off point)[4] was not possible, however, space-charge neutrality could still be assumed at low carrier concentrations, just like the depletion assumption of the space-charge layer of a reverse-biased p/n junction, in order to allow the Fourier series expansion of the 2-D Poisson and Laplace Equation $\mathrm{div} \cdot \boldsymbol{D} \equiv \nabla \cdot \varepsilon \boldsymbol{E} = \varepsilon[(\partial E_X/\partial x) + (\partial E_Y/\partial y)] = \varepsilon[-(\partial^2 V/\partial x^2) - (\partial^2 V/\partial y^2)] = \rho = q(P - N - P_{IM}) = q(-P_{IM}) \approx 0$, in an expop that could have an odd (not symmetrical) geometry. Here, $E_X = -\partial V/\partial x$ and $E_Y = -\partial V/\partial y$ are the x- and y-component respectively of the DC steady-state electric field vector in 2-D, $E(x,y)$, assuming uniformity in the z-direction, for a field vector which is derivable from a scalar potential function, $V(x,y)$. ε is the electrical permittivity of the section or region, q, the magnitude of the electron charge, P and N, are respectively the DC steady-state concentrations of holes and electrons, and $P_{IM}(x,y)$, the concentration of the negatively charged impurity ions less the concentration of the positively charge impurity ions. We have $P_{IM} = P_{A^-} - N_{D^+} = 0$ for the pure base region which has no acceptor impurities, $P_{AA} = 0$ and no donor impurities $N_{DD} = 0$, then $P_{A^-} = P_{AA} \times f_A = 0$ and $N_{D^-} = N_{DD} \times f_D = 0$ where f_A and f_D are the fractions of the acceptors and donors in their respective charge states.

In transistors with pure base, the transistors are almost always electrically short as recognized and pointed out by us recently in Ref. [3] because there are so few electrons and holes to screen the charges (whether fixed ions and electrode charges, or even the mobile electron and hole charges themselves), so the linear carrier-screening dis-

tance or the Debye Length, $L_D = \{\varepsilon_{Si} kT/[q^2(n_i + n_i)]\}^{1/2} \cong 25\mu$m ($25\mu$m to 30μm at room temperature), is so much larger than the make-ups and dimensions of the transistor. Previous authors[18] arbitrarily defined a characteristic length, which they erroneously called the Debye length, and which is twice the correct value, $2\times L_D = 2\times 25 = 50\mu$m[3]. For impure base, the local linear carrier-screening Debye length, $L_D = \{\varepsilon_{Si} kT/[q^2(P + N)]\}^{1/2}$, decreases with increasing impurity concentration from $P \cong P_{AA}$ for p-type region and $N \cong N_{DD}$ for n-type region. In a p-type silicon region with $P \cong P_{AA} = 10^{16}\text{cm}^{-3}$ and $(P_{AA}/n_i)^{1/2} = (10^{16}/10^{10})^{1/2} = 10^3$, thus, the screening distance is decreased by 1000 to $25\mu\text{m}\times 10^{-3} = 25$nm, but this is still comparable to and not much smaller than the dimension of nanometer impure-base FinFETs. It is too large to produce effective carrier screening of the charge distributions on the device geometric features. For the pure-base, this electrically short channel is expected to significantly affect transistor characteristics, and it is analyzed in the third report of this series[15].

2.2 The Surface-Potential-Based Parametric Voltage and Current Equations

The x-Voltage Equation[8,11] and the y-Current Equation[9,11] for the two-MOS gates on thin pure-base BiFETs are similar to those derived for the long-wide-channel thick-impure-base transistor[13,14], with the base impurity concentration set to zero, $P_{IM} = 0$, and the boundary conditions $E_X(x,y) = -\partial V(x,y)/\partial x = 0$ and $V(x,y) = V_0(y)$ set at the symmetry or mid plane $x = x_B/2$ of the thin base layer ($0 \leqslant x \leqslant x_B$). These can be simply modified if the two gates and the two voltages applied to the two gates are dissimilar. When the two gate voltages (all contact potential differences are included) are opposite in sign, these two boundary conditions are replaced by the single new boundary condition $V(x_0, y) = 0$ where x_0 is located somewhere in the base layer, $0 \leqslant x_0 \leqslant x_B$, varying along the length y, i.e., $x_0 = x_0(y)$. On account of equation simplicity and device physics, they are normalized to the Debye Length, $X = x/L_D$ and $Y = y/L_D$. The three potential variables are also normalized, to the thermal voltage, kT/q,[11,13,14]: the electron and hole electrochemical or quasi-Fermi potentials, V_N and V_P, by $U_N(x,y) = qV_N(x,y)/kT$ and $U_P(x,y) = qV_P(x,y)/kT$, and the electric potential $V(x,y)$, set to the intrinsic Fermi level position $V(x,y) = V_I(x,y) = E_I(x,y)/(-q)$ of the pure base, by $U(x,y) \equiv U_I(x,y) = qV(x,y)/kT = qV_I(x,y)/kT$. The electron and hole currents flowing through the entire thin base from source ($y=0$) to drain ($y=L$) are normalized to $I_{N0} = 2\times(W/L)\mu_n C_O(kT/q)^2$ and $I_{P0} = 2(W/L)\mu_p C_O \times(kT/q)^2$ where 2 comes from two gates or two electron and two hole surface channels, (W/L) = SQUARE = SQ, is the aspect ratio or the ratio of the channel width (z-direction) to length (y-direction). It is the number of squares, SQ, for specifying the conductance and resistance of thin conductors. It is used in the y-axis or current and conductance axis in the figures. μ_n and μ_p are the electron and hole mobilities, taken as constant, as required by benchmarking compact models, since mobilities are fundamental materials parameters, defying exact quantum statistical mechanics treatments in reality transistors of high non-uniformities, and are proprietary specialties of each manufacturer, if not also the pastimes for freedom of expression of each of its engineers. Hence they are best treated as optional compact modeling parameters. $C_O = \varepsilon_O/x_O$, is the oxide capacitance per unit area with electrical thickness x_O.

The transistor characteristics are strongly dependent on the ratio of the pure-silicon Debye Capacitance to the Oxide Capacitance C_D/C_O or the ratio of the 'effective' thickness (scaled to Si dielectric) of the gate oxide to the silicon Debye Length, $C_D/C_O = (\varepsilon_{Si}/L_D)/(\varepsilon_{Ox}/x_O) = (\varepsilon_{Si}/\varepsilon_{Ox})\times(x_O/L_D) = 3.0(1.5\text{nm}/28.7435\mu\text{m}) = 1.5656\times 10^{-4} \approx 10^{-4}$. For example, this ratio determines the "threshold" gate voltage near the source end of the channel, $V_{GSth} = -(kT/q)\log_e(C_D/C_O)^2 \cong 18(kT/q) \cong 500$mV, which is confirmed by the numerical results to be presented in figures and discussed later. The ratio of the silicon to silicon dioxide dielectric constants is given by $(\varepsilon_{Si}/\varepsilon_{Ox}) = (11.7/3.9) = 3.0$ and the Debye Length is defined by the static (i.e. low-frequency) linear response theory of a many-body system of electrons and holes, $L_D = \{\varepsilon_{Si} kT/[q^2(n_i + n_i)]\}^{1/2} = 28.7435\mu$m at $T = 296.57$K where the electron and hole concentrations in the pure silicon base is given by $n_i = 1.000000\times 10^{10}\text{cm}^{-3}$, which gives $\cong 25\mu$m at

~300K. The Boltzmann constant is $k = k_B = 1.380662\times10^{-23}$ J/K = 8.617346×10^{-5} eV/K. The electron charge is $q = 1.6021892\times10^{-19}$ C. At T = 296.57K = 23.42C = 74.156F, we have k_BT/q = 25.55646mV.

In the theoretical analysis, we ground the source to the external voltage reference, denoted by B, so $V_{SB} = 0$. The space point $B(x, y, z)$ could be a physical contact point to the thin base at the source end, or the vacuum level on one side of the semi-infinite 1-dimensional device model, or on the distant surround (such as the electrostatic shield of a wafer probe station) of a two- or three-dimensional device model from which the workfunction is measured. We also lump the contact potential difference of each contact into the voltage applied to the terminal of the contact relative to the reference point, $B(x, y, z)$. For example, U_{FB} is the flatband voltage of the two identical gates. $G_1 = G_2 = G$, so that $U_{GB} - U_{FB} = U_{GF} = U_{GS} - U_{BS} - U_{FB} = U_{GS} - U_{FB}$ which is indicated in the figures as V_{GS} with the flatband voltage, V_{FB}, understood. Overlooking this potential reference has resulted in erroneous solutions which is valid only at $V_{DS} = 0$[18].

Based on the foregoing definitions and considerations, the twelve surface-potential-based parametric voltage and current equations of the bipolar field-effect transistor[3,7], and the differential transconductance and drain conductance equations are then given by

$$U_{GB} - U_{FB} - U_S = U_{GS} - U_S = (\mathrm{sgn}U_S)(C_D/C_O)\times\{\exp(-U_N)[\exp(+U_S) - \exp(+U_0)] + \exp(+U_P)[\exp(-U_S) - \exp(-U_0)]\}^{1/2} \quad (1)$$

$$I_D = I_{D\text{-electron}} + I_{D\text{-hole}} = \{\text{integration of } X = 0 \text{ to } X_B \text{ and } Y = 0 \text{ to } Y_L = L/L_D\}$$
$$= I_{N0}\iint\exp(U - U_N)(-\partial U_N/\partial Y)\partial Y\partial X + I_{P0}\iint\exp(U_P - U)(-\partial U_P/\partial Y)\partial Y\partial X \quad (2)$$

$$g_m = \partial I_D/\partial V_{GS} \quad (V_{DS} = \text{constant}) \quad (3)$$

$$g_d = \partial I_D/\partial V_{DS} \quad (V_{GS} = \text{constant}) \quad (4)$$

2.3 For the Electron Channel ($U_S > U_0 > 0$)

$$X_B \equiv (x_B/L_D) \equiv \chi_B$$
$$(\text{integration of } U = U_0 \text{ to } U_S)$$
$$\chi_B \equiv 2\int\{\exp(-U_N)[\exp(+U) - \exp(+U_0)] + \exp(+U_P)[\exp(-U) - \exp(-U_0)]\}^{1/2}dU \quad (5)$$

$$I_{N6} = I_{N0}\int(U_{GB} - U_{FB} - U_S)dU_N \quad (U_N = 0 \text{ to } U_{DS}) \quad (6)$$

$$I_{P7} = I_{P0}\int -(U_{GB} - U_{FB} - U_S)dU_P \approx 0 \quad (U_P = U_{GS} \text{ to } U_{DS}) \quad (7)$$

$$I_{N8} = I_{N0}\int(U_{GB} - U_{FB} - U_S)dU_N \quad (U_N = 0 \text{ to } U_{GS}) \quad (8)$$

2.4 For the Hole Channel ($U_S < U_0 < 0$)

$$X_B \equiv (x_B/L_D) \equiv \chi_B$$
$$(\text{integration of } U = -U_0 \text{ to } -U_S)$$
$$\chi_B \equiv 2\int\{\exp(-U_N)[\exp(+U) - \exp(+U_0)] + \exp(+U_P)[\exp(-U) - \exp(-U_0)]\}^{-1/2}dU \quad (9)$$

$$I_{P10} = I_{P0}\int -(U_{GB} - U_{FB} - U_S)\,dU_P \quad (U_P = U_{GS} \text{ to } U_{DS}) \quad (10)$$

The drain terminal current, positive current flowing into the drain contact, is then given by

$$I_D = I_{N6} + I_{P7} \approx I_{N6} \quad (U_{GS} > U_{DS}) \quad (11)$$

$$I_D = I_{N8} + I_{P10} \approx I_{N8sat} + I_{P10} \quad (U_{GS} < U_{DS}) \quad (12)$$

3 Computed Current Voltage Characteristics

The transfer and output current-voltage and conductance-voltage characteristics are computed from these twelve equations. A Lenovo-IBM T60 Thinkpad Notebook computer is used with a 1.6GHz Intel Core-Dual (90nm) processor and 1.5GB of memory, running the 32-bit Windows XP Professional Operating System. The computations are made using the recently released (May 4, 2007) 64-bit Intel Visual FORTRAN (IVF) Version v10.00xx, with the library subroutines IMSL (v8) and MKL (v7). Numerical accuracy and computation speed are both quite adequate (a few minutes per curve). The computation speed could be improved slightly if the 64-bit Windows XP is used to take advantage of the 64-bit registers of the Core-Dual processor. Slight speed gain could also be obtained using the later T60 models with the recent Core-2-Dual (65nm) processor or the even smaller (45nm) processor technology. Sample results are plotted by ORIGIN (v7). They are presented in figures described in the following sections for the two identical MOS-gates on pure-base BiFET. The electron and hole mobilities are taken as 400cm²/(V·s). Their difference will

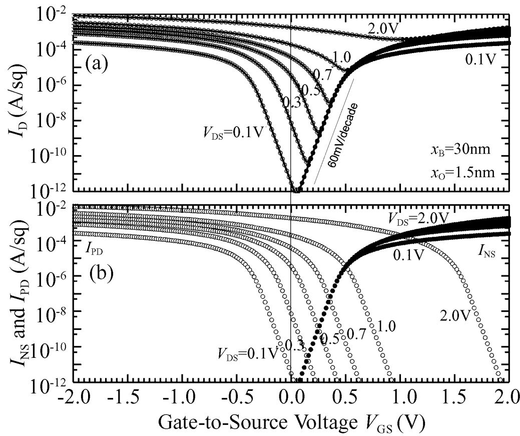

Fig. 1 Drain-source voltage V_{DS} dependence of the DC transfer current-voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS gates on a thin pure-silicon base. (a) Total drain terminal current. (b) Electron and hole channel current components of the drain terminal current.

just scale the currents and conductances. Their field and position dependences in real transistors are the subjects of compact modeling, not our baseline benchmark model aimed for optimizing their compact models and their accuracies. One square or $W/L=1$ is assumed or used as the normalization.

3.1 Transfer Characteristics

Figure 1 (a) shows the drain-source voltage, V_{DS}, dependence of the transfer characteristics, I_D versus $V_{GS}=V_{GB}-V_{BS}-V_{FB}$, with $V_{DS}=V_{DB}-V_{BS}=0.1, 0.3, 0.5, 0.7, 1.0$ and $2.0V$, at a pure-silicon-base thickness of $x_B=30nm$, and a gate insulator electrical thickness of $x_O=1.5nm$. Figure 1 (b) shows the electron I_{NS} and hole I_{PD} surface channel current components. Some salient features are noted from these two figures which are also present in the following figures on other transistor characteristics. (1) The minimum of the drain terminal current and the symmetry centered at the minimum are due to simultaneous presence of the electron channel and hole channel currents. These were observed in recent FinFETs by IMEC+Assignees[2,3] and WireFETs by Samsung and IME-Singapore[3]. (2) The ideal subthreshold swing of 60mV/decade is easily anticipated by the back-of-the-envelope calculation: $U_{GS}=U_S-(C_D/C_O)\times(\mathrm{sgn}U_S)\{\text{see Eq. (1)}\}^{1/2}\cong U_S$ because the silicon Debye length ($\sim 25\mu m$) is so much larger than the gate oxide thickness (1.5nm) or $C_D/C_O\sim 10^{-4}\ll 1$ so that most of the voltage applied between the gate-source terminals appears across the oxide to control the barrier height at the source contact. Then, because the subthreshold range is dominated by diffusion, we have, $I_{DN}=\text{drift}+\text{diffusion}\propto\text{diffusion}=-qD_n(\partial N/\partial y)=-qD_n n_i\times\exp(U_S-U_N)\times(\partial/\partial y)(U_S-U_N)\propto\exp(U_S)=\exp(U_{GS})=\exp(qV_{GS}/kT)$. This is the ideal subthreshold slope with the gate-voltage (V_{GS}) swing of $S=(kT/q)\log_e 10=25.55646mV\times 2.302585=58.84592mV$. (3) The theoretical threshold voltage can be defined as the point when the (C_D/C_O) term in the voltage equation (1) dominates, for example, 10 times larger than the first term, U_S, following the classic definition proposed one of us in 1964～1965[8]. This is the region dominated by the carrier-space-charge-limited drift current[20]. Thus, the threshold voltage at the source (or the drain) for the pure-base silicon BiFET transistor is given by $V_{GS\text{-}th}=(kT/q)[2-\log_e(C_D/C_O)^2]\cong(25.56)\times[2-2\times\log_e 1.5656\times 10^{-4}]=(25.56)\times(19.524)=499mV$. This is close to the value shown in Fig. 1(a) for the I_D at all $V_{DS}\geqslant 0.1V\sim 4kT/q$ and it coincides with the gate voltage at the minimum I_D at $V_{DS}=1.0V$ in Fig. 1(a). For experimental data analyses and compact modeling, Zhou[21] gave a more general and operational (amendable to experimental applications) definition of the threshold voltage in 2001 as the intercept of the extension of the high channel current with the extension of the subthreshold current, which can also be computed theoretically, and a theoretical definition was given by Ortiz-Conde in 2003[18]. (4) The parallel shift of the hole channel current, $I_{PD}(V_{GD}, V_{SD})$, by V_{DS} as indicated in Figs. 1 (a) and 1 (b) comes from the change of the hole barrier height at the drain with the change of V_{DS}, $V_{GD}=V_{GS}-V_{DS}$. (5) Asymmetry was also observed in FinFETs fabricated by IMEC+Assignees[2,3] when $I_{PD}\ll I_{NS}$ in n-FinFETs and when $I_{PD}\gg I_{NS}$ in p-FinFETs due to the difference between the barrier heights of the contacts to the source and the drain ends of the pure-base. This was simulated by us using several models and presented by us[3,7]. A theoretical analysis will be reported[17].

Figure 2 (a) shows the V_{DS} dependence of the differential transconductance versus gate voltage, g_m vs V_{GS}, and Fig. 2(b) the electron and hole

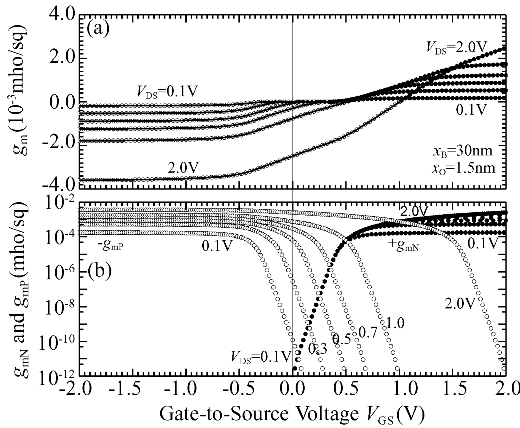

Fig. 2 The V_{DS} dependence of the differential transconductance versus gate voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS gates on a thin pure-silicon base. (a) Total transconductance. (b) The electron and hole components of the transconductance.

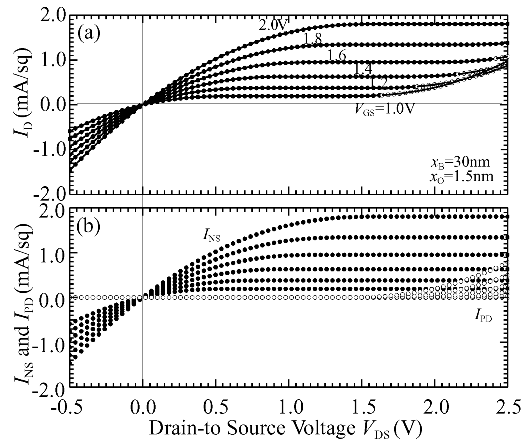

Fig. 4 Gate-source voltage V_{GS} dependence of the DC output current-voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS gates on a thin pure-silicon base. (a) Total drain terminal current. (b) Electron and hole channel current components of the drain terminal current.

components of the differential transconductance. The negative differential transconductance from hole currents is definitional and comes from the reduction of the hole currents when V_{GS} increases at a constant V_{DS}. For example, $V_{GD} (= V_{GS} - V_{DS} = V_{GS} - 2.0\text{V})$ increases when V_{GS} increases, which decreases the hole barrier height at the drain end of the channel and the surface hole concentration and hole channel current or hole current in the drain terminal.

Figure 3 (a) shows the V_{DS} dependence of the differential output conductance versus gate voltage characteristics, g_d vs V_{GS}, and Fig. 3(b) the

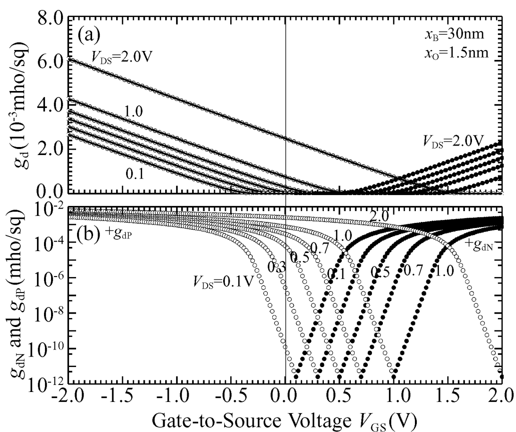

Fig. 3 The V_{DS} dependence of the differential output conductance versus gate voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS-gates on a thin pure-silicon base. (a) Total output conductance. (b) The electron and hole components of the output conductance.

electron and hole contributions. The important result is that drain conductance increases from the small or nearly zero value in the initial drain current saturation range, shown by the solid lines in Fig. 3(a), but it rapidly increases when the hole current started to flow at higher drain voltages or higher drain-to-gate voltages, above the threshold for the two hole surface channels (two from identical double gates), which increases the hole concentration in the hole surface channel and the hole component of I_D.

3.2 Output Characteristics

The output characteristics, drain current, conductance and transconductance, as a function of output voltage, V_{DS}, are shown in Figs. 4, 5, and 6, in the same format as transfer characteristics just described in Figs. 1, 2, and 3. Figure 4 (a) shows that I_D increases after saturation as V_{DS} increases beyond saturation, defined by $V_{DSth} = V_{DSsat} + V_{GSth} = V_{GS} + V_{GSth}$, because the hole current, I_{PD} in Fig. 4 (b), starts to take off, parabolically, in the electron channel current saturation range, when $V_{DS} > V_{DSsat} = V_{GS} + V_{GSth} = V_{GS} + 0.499\text{V}$ where 0.499V was just computed from $(kT/q)[2 + \log_e(C_O/C_D)^2]$. The large and increasing differential output conductance, g_d, with increasing V_{DS} as shown in Fig. 5 (a) comes from the increasing hole conductance, shown in Fig. 5(b), due to the increasing hole surface concentration from the

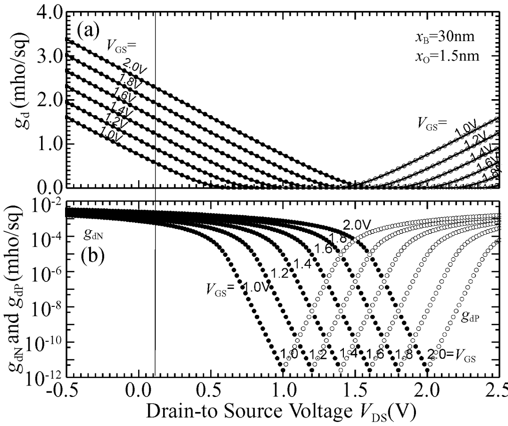

Fig. 5 The V_{GS} dependence of the differential output conductance versus drain voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS gates and a thin pure-silicon base. (a) Total output conductance. (b) The electron and hole components of the output conductance.

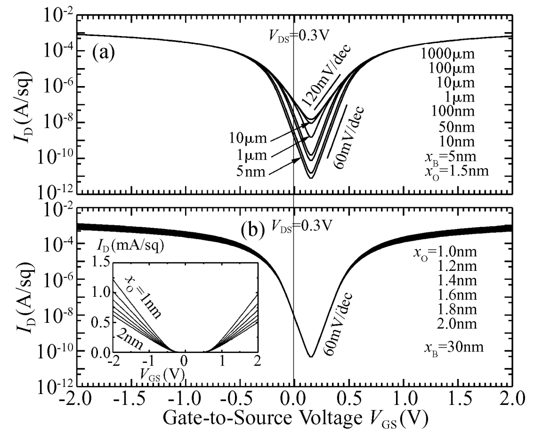

Fig. 7 (a) Base layer thickness x_B and (b) oxide thickness x_O dependences of the DC transfer current-voltage characteristics of silicon bipolar field-effect transistors (BiFETs) with two identical MOS gates on a thin to thick pure-silicon base.

more negative gate-drain voltage, $V_{GD} = V_{GS} - V_{DS}$ as V_{DS} increases. This decreases the differential transconductance, as shown in Fig. 6 (a) due to the negative differential transconductance from the increasing hole current.

3.3 Base Layer and Oxide Thickness Dependences

Figures 7, 8, and 9 show the base layer and oxide thickness dependences of the transfer current-voltage and conductance-voltage characteristics. The base layer thickness covers the very thick range, $x_B = 1\mu m$ to $1000\mu m$, corresponding to the thickness of 12-inch silicon wafers ($\sim 1000\mu m$) in order to show two intrinsic properties when $x_B > L_D \sim 25\mu m$: (1) The characteristics of the double gate are just the sum of that of two single-gate bulk transistor, such as half of the SOI (Silicon on Insulator), asymptotically approached by the present case of pure-base or lowly doped base with P_{IM} (or N_{IM}) $< \sim n_i = 10^{10} cm^{-3}$; (2) The BJT-like source (emitter) to drain (collector) leakage current in the off condition from the thick-and-short MOST base (or the wide-and-thin BJT base).

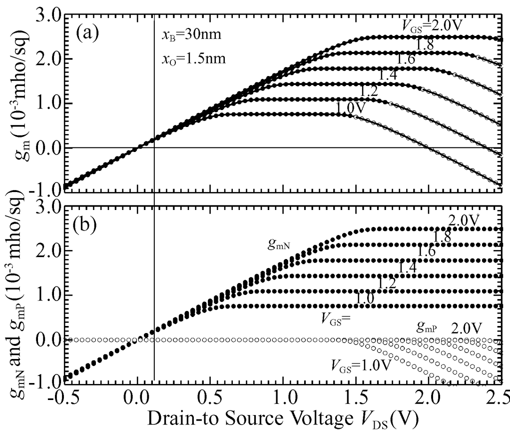

Fig. 6 The V_{GS} dependence of the differential transconductance versus drain voltage characteristics of a silicon bipolar field-effect transistor (BiFET) with two identical MOS gates on a thin pure-silicon base. (a) Total transconductance. (b) The electron and hole components of the transconductance.

Figure 7 (a) shows that the subthreshold characteristics are greatly affected by the base layer thickness. (1) In the thin base range, the ideal voltage swing of 60mV per decade was discussed in the detail with Figs. 1 (a) and 1 (b). (2) In the thick base range, there is the 120mV per decade range from diffusion-limited body current at high-level injection in the volume channel region in the middle part of the thick base, making $N \sim P \sim \exp(qV_{GS}/2kT)$, which gives $I_{NS} \propto N/L \propto \exp(qV_{GS}/2kT)$ for the electron surface channels and $I_{PD} \propto P/L \propto \exp(-qV_{GD}/2kT) = \exp(-qV_{GS}/2kT) \times \exp(+qV_{DS}/2kT)$ for the hole surface channels. (3) In the thick bases, the electron and hole surface channel currents would each continue to decrease as gate-voltage reaches flatband and then into the "accumulation" of the other carrier type, but which would give the second carrier-species channel current, that causes the rise of the total current from the minimum.

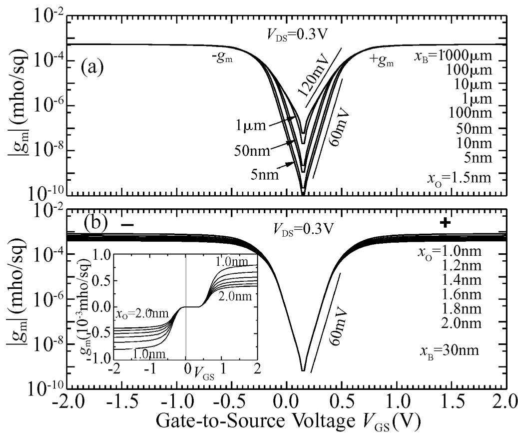

Fig. 8　(a) Base layer thickness x_B and (b) oxide thickness x_O dependences of the differential transconductance versus gate voltage characteristics of silicon bipolar field effect transistors (BiFETs) with two identical MOS gates on a thin to thick pure-silicon base.

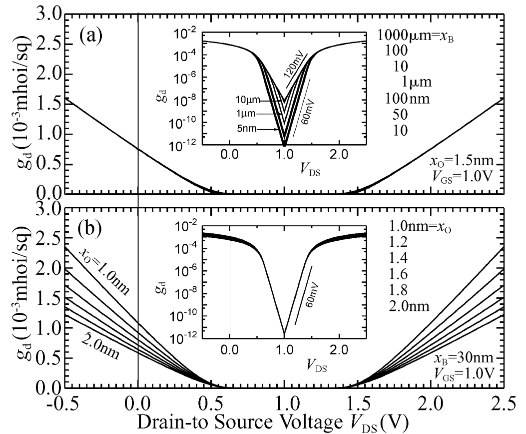

Fig. 9　(a) Base layer thickness x_B and (b) oxide thickness x_O dependences of the differential output conductance versus drain voltage characteristics of silicon bipolar field-effect transistors (BiFETs) with two identical MOS gates on a thin to thick pure-silicon base.

(4) The additional JGFET-like bulk-channel current, calculated using $N = P = n_i$ would increase to a maximum at flatband and then decrease, reflecting the change of the electrical thickness of the bulk or volume channel, however, it could be masked by the surface channel currents. (5) The base-thickness has little or no effect on the high current range which is dominated by electron and hole drift currents in the surface channels.

Figure 7 (b) shows that the subthreshold characteristics are not noticeably changed by the oxide thickness in the range from x_O = 1nm to 2nm. The small shift in V_{GSth} from $(kT/q) \times \log_e(C_D/C_O)^2 = (kT/q)\log_e 4 = 25.56\text{mV} \times 1.386 = 35.43\text{mV}$ is not evident in the displayed scale of this figure. However, as expected, the large electron and hole surface channels, dominated by drift, increases nearly linearly with the gate oxide capacitance or inversely with the gate oxide thickness, as indicated by the linear plot in the inset of the semilog plot of Fig. 7 (b).

The differential transconductance, g_m, shown in Figs. 8 (a) and 8 (b) tracks that of the drain current, I_D, just described for Figs. 7 (a) and 7 (b) in both base and oxide thickness dependencies, except that it tends to saturate at high V_{GS}, as shown by the inset in Fig. 8 (b), rather than the continued rise in semi-infinite bulk transistor, or the very thick base double gate, $x_B \gg L_D \sim 25\mu$m, such as the $x_B = 100\mu$m and 1000μm curve which are not presented in these figures. This is expected because the tied double gates raises the base potential, U_0 from the zero of the thick base, which would be overcome if the two gates are biased in opposite polarity.

The dependence of the output or drain conductance on the base and oxide thicknesses are shown in Figs. 9 (a) and 9 (b). These are very similar to those of the drain current, I_D, described in Figs. 7 (a) and 7 (b) in both the subthreshold and strong ‘inversion’ surface-channel current ranges.

4　Summary

Theoretical DC current-voltage and differential conductance-voltage characteristics are obtained for the nanometer double-gate on thin pure-silicon-base MOSFET, showing the simultaneous presence of both electron and hole surface channels, hence the new acronym bipolar field-effect transistor, BiFET. This previously not recognized BiFET characteristics could provide circuit functions in one physical transistor, such as the CMOS inverter and the SRAM-like bistable current-voltage characteristics.

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nanometer technology such as the double-gate and thin base, and who questioned the references they used for the electric potential and the electron and hole electrochemical potentials. We thank Professor Chenming Hu (University of California, Berkeley, USA) for a copy of his invited talk cited in Ref. [1]. We are especially thankful to Professor Gennady Gildenblat (Arizona State University, USA) for an in-depth discussion of the bipolar field-effect phenomena and his reminder of the traditional and precise usage of the term "volume" channel instead of "bulk" channel in contrast to and in paring with the term "surface channel". We also thank Professors Mitiko Miura-Mattausch (Hiroshima University, Japan), Xing Zhou and Gennady Gildenblatt, and Drs. Colin McAndrew (Freescale Semiconductor Company, USA), Jin Cai, Tak H. Ning, Lewis M. Terman, and Hwa-Nien Yu (IBM, New York, USA), for encouragements to undertake these investigations and for their comments and suggestions. We also thank Professors Marcel D. Profirescu (University Politechnica of Bucharest, Romania), Adelmo Ortiz-Conde and Francisco J. Garcia Sanchez (Universidad Simon Bolivar, Venezuela) and Juin J. Liou (University of Central Florida, USA) for inviting us to present our results at their IEEE EDS Mini-Colloquium and ICCDCS conferences. The senior author is especially thankful to Professor Xing Zhou for inviting him back into the compact modeling community after more than 40-years of absence.

References

[1] Chenming Hu, "From CMOS to Nanotechnology," Keynote, 17th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference, May 22—24 2006, Boston, Massachusetts.

[2] T. Hoffmann, G. Doornbos, I. Ferain, N. Collaert, P. Zimmerman, M. Goodwin, R. Rooyackers, A. Kottantharayil, Y. Yim, A. Dixit, K. De Meyer, M. Jurczak, and S. Biesemans, "GIDL (Gate-Induced Drain Leakage) and Parasitic Schottky Barrier Leakage Elimination in Aggressively Scaled HfO_2/TiN FinFET Devices," IEDM Technical Digest, 743—746, Dec. 2005.

[3] Chih-Tang Sah and Bin B. Jie, "Double-Gate Thin-Base MOS Transistor: The Correct Theory," and Bin B. Jie and Chih-Tang Sah, "Double-Gate Thin-Base MOS Transistor: Characteristics for the Short Channel," Late-News Papers Presented on May 23, 2007 at the Workshop on Compact Modeling (WCM20070523) of the NSTI Nanotechnology Conference and Trade Show, May 22—24, 2007, hosted by the Nano Science and Technology Institute, Cambridge, MA 02139, USA. http://www. nsti. org/Nanotech2007/WCM2007/.

[4] William Shockley, 'A Unipolar "Field Effect" Transistor,' Proceedings of the IRE, 40(11), 1365—1376, November 1952. For experimental reduction to practice, see George C. Dacey and Ian M. Ross, "Unipolar 'Field-Effect' Transistor," Proceedings of the IRE, 41(8), 970—979, August, 1953.

[5] William Shockley, "The Theory of p-n Junction in Semiconductors and p-n Junction Transistor," Bell System Technical Journal 28(5), 435—489, July, 1949.

[6] H. S. Fu and C. T. Sah, "A Distributed-Gate Bistable MOS Transistor," Solid-State Electronics 14(9), 799—804, September 1971.

[7] Chih-Tang Sah and Bin B. Jie, "Bipolar Theory of MOS Field-Effect Transistors and Experiments," Chinese J. Semiconductors, 28(10), 1497—1502, October, 2007.

[8] Chih-Tang Sah and Henry C. Pao, "The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistor," IEEE Transaction on Electron Devices, 13(4), 410—415, April 1966. (1965-Sah-Pao.) Together with [9] to be referred to as 1966-Sah-Pao.

[9] Henry C. Pao and Chih-Tang Sah, "The Effects of Diffusion Current on the Characteristics of MOS Transistors," Solid-State Electronics, 9(10), 927—938, October 1, 1966. (1966-Pao-Sah)

[10] Chih-Tang Sah and Bin B. Jie, "The Bipolar Field-Effect Transistor: the Drift and Diffusion Current Theory," CJS 28 (12), December 2007.

[11] Chih-Tang Sah and Bin B. Jie, "A History of MOS Transistor Compact Modeling," Keynote. Technical Proceedings Workshop on Compact Modeling (WCM), Abstract on pp. 1—2 and full text on pp. 349—390. Editors: Xing Zhou, Matthew Laudon and Bart Romanowicz. NSTI Nanotech 2005. The NSTI Nanotechnology Conference and Trade Show, May 8—12, 2005. Nano Science and Technology Institute, Cambridge, MA 02139, USA. # PCP05040394. On-line: http://www. nsti. org/publ/Nanotech2005WCM/1429. pdf

[12] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios and C.-T. Sah, "Advanced Compact Models for MOSFETs," Technical Proceedings Workshop on Compact Modeling (WCM), 3—12. Editors: Xing Zhou, Matthew Laudon and Bart Romanowicz. NSTI Nanotech 2005. The NSTI Nanotechnology Conference and Trade Show, May 8—12, 2005. Nano Science and Technology Institute, Cambridge, MA 02139, USA. # PCP05040394. On-line: See [11] above.

[13] Bin B. Jie and Chih-Tang Sah, "Evaluation of Surface-potential-Based Bulk-Charge Compact MOS Transistor Model," IEEE Transactions on Electron Devices, 52(8), 1787—1794, Aug 2005.

[14] Bin B. Jie and Chih-Tang Sah, "Accuracy of Surface-potential-based Long-wide-channel Thick-base MOS Transistor Models," IEEE Transactions on Electron Devices, 54(8), 1897—1909, August 2007.

[15] Bin B. Jie and Chih-Tang Sah, "The Bipolar Field-Effect Transistor: Short Channel Theory," CJS 29(1), January 2008.

[16] Bin B. Jie and Chih-Tang Sah, "The Bipolar Field-Effect Transistor: Deviation of the Unipolar Theory," CJS 29(2),

February 2008.

[17] Bin B. Jie and Chih-Tang Sah，“The Bipolar Field-Effect Transistor：Contact Theory，” CJS 29(3)，March 2008.

[18] A. Ortiz-Conde，F. J. Garcia-Sanchez，J. Muci，S. Malobabic，J. Liou，“A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs，” IEEE Transactions on Electron Devices，54(1)，131—139，January 2007.

[19] Chih-Tang Sah，Robert N. Noyce，and William Shockley，“Carrier Recombination in p/n Junctions and p/n Junction Characteristics，” Proceedings of the IRE，45 (9)，1228—1243，September 1957.

[20] Chih-Tang Sah，“Space Charge Theory of the MOS Transistor，” Intel Grant Report，Dec. 12，1996. Derivations were reproduced and reconfirmed in [13] and [14].

[21] Xing Zhou，K. Y. Lim and W. Qian，“Threshold Voltage Definition and Extraction for Deep-Submicron MOSFETs，” Solid-State Electronics 45，507—510，2001.

双极场引晶体管:I. 电化电流理论(双 MOS 栅纯基)*,**

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摘要： 本文描述双极场引晶体管(BiFET)及其理论. 把两维晶体管分解成两个一维晶体管，得到解析方程. 以表面势为参变量，采用电化(准费米)势梯度驱动力计算电流. 提供实用电极直流电压及器件参数范围，随直流电压变化，输出和转移电流和电导. 电子和空穴表面沟道同时存在，这新特点可以用来在单管实现 CMOS 电路倒相和 SRAM 存储电路.

关键词： 双极场引晶体管理论；MOS 场引晶体管；双极结型晶体管；同时并存空穴电子表面沟道；体积沟道；表面势

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