Top-Down Design of 260k Color TFT-LCD One-Chip Driver ICs*

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Abstract: A top-down design methodology is proposed for the design of TFT-LCD one-chip driver ICs, and a 260k color, 176RGB×220-dot TFT-LCD one-chip driver IC is successfully developed with silicon verification. This IC is a typical mixed-signal VLSI and is implemented by a 0.18μm HV CMOS process. The static power dissipation is about 5mW for 260k color display mode, and the settling time of the output grayscale voltages within 0.2% error is less than 26μs.

Key words: TFT-LCD; driver IC; top-down design; driving circuit; mixed-signal VLSI
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1 Introduction

Increasing time-to-market (TTM) pressures and process technologies scaling are the two fundamental forces driving designers, design methodologies, and EDA tools today[1]. A top-down design methodology is adopted to design mixed-signal VLSI for shrinking design period and enhancing productivity.

A one-chip driver IC for thin film transistor-liquid crystal display (TFT-LCD) is a typical mixed-signal VLSI including different kinds of blocks, such as a standard logic circuit, DAC, OPAMP, DC-DC converters, SRAM, and etc. These blocks have different voltage level signals and are fabricated by a hybrid voltage CMOS process.

Driver ICs are a key part in an LCD Module and have been widely applied to all kinds of portable electronic devices. A low power 260k color TFT-LCD one-chip driver IC was presented[2,3]. The driving buffers of a 402-output TFT-LCD driver IC are arranged at the outputs of 64 grayscale voltages and the settling time of the output grayscale voltage within 0.2% error is 28.3μs when 402-line loads are driven[4]. To reduce power consumption and chip size, a sub-pixel rendering and a data compression algorithm were proposed[5]. However, a top-down design methodology for a TFT-LCD one-chip driver IC has not yet been reported.

In this paper, a top-down design methodology is proposed for the design of TFT-LCD one-chip driver ICs. The architecture of a TFT-LCD one-chip driver IC is presented in the second section, the top-down design methodology of a one-chip driver IC is discussed in the third section, and the development of key function blocks is described in the fourth section. Finally, the results of tests and measurements are given in the fifth section.

2 Architecture of TFT-LCD one-chip driver IC

A TFT-LCD one-chip driver IC, shown in Fig. 1,

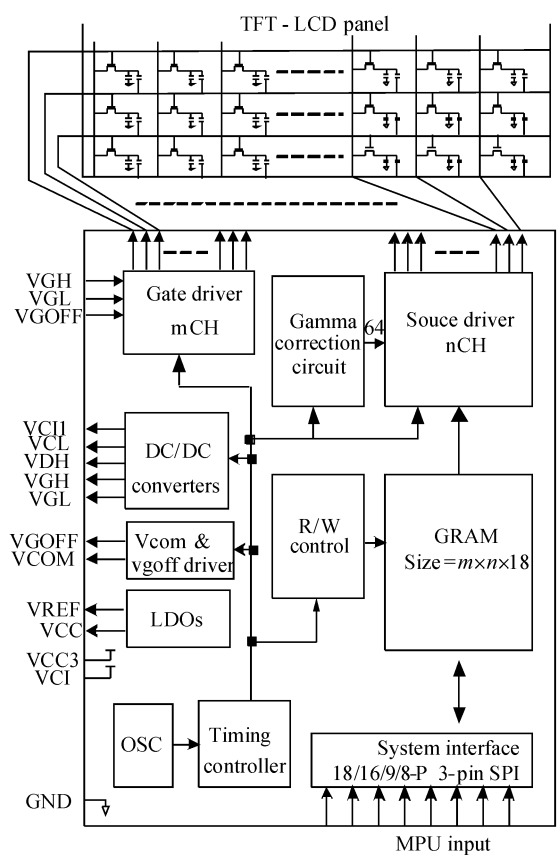

Fig. 1 Block diagram of TFT-LCD one-chip driver IC

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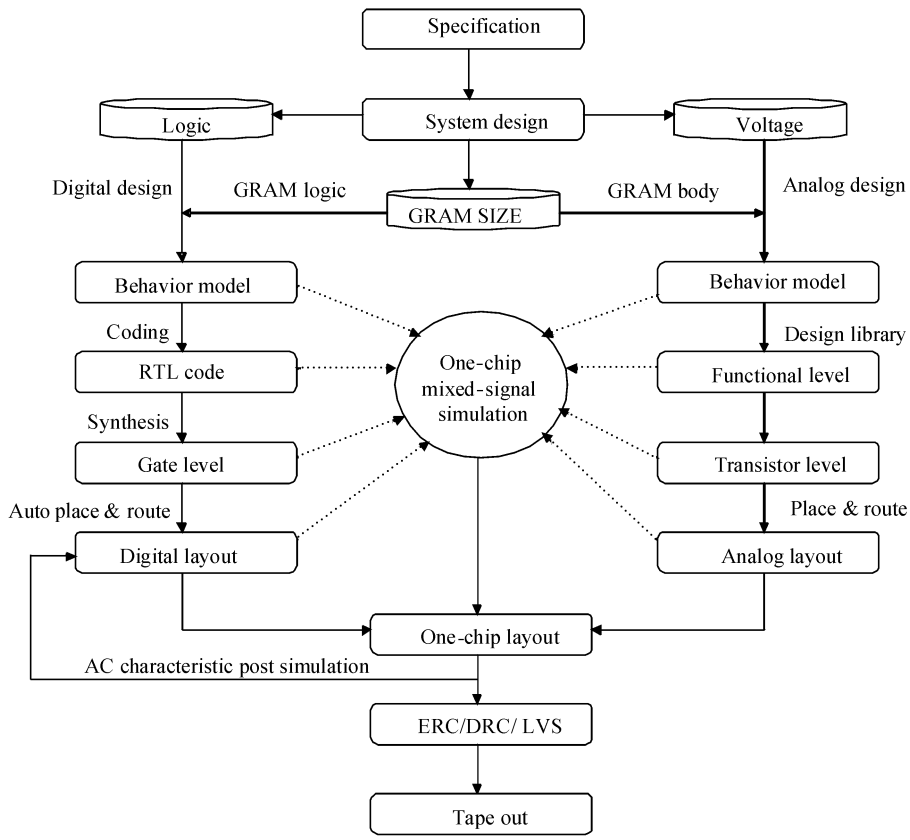

Fig. 2　Top-down design flow for TFT-LCD one-chip driver IC

consists of a system interface with MPU, OSC, timing controller, GRAM, gamma (γ) correction circuit, DC/DC converters, gate driver, source driver, Vcom & Vgoff driver, LDOs, etc.

The system interface receives digital image data from an external MPU and outputs to GRAM. GRAM is used for the storage of one-frame digital display data. The entire line data in GRAM is output to the source driver at one time. The timing controller generates controlling signals and timing clocks for the whole driver IC. The gamma (γ) correction circuit generates grayscale voltages corresponding to input digital display data. DC-DC converters generate the operating voltages of all blocks and driving voltages for the TFT-LCD panel. The gate driver and source driver generate the line driving voltages and column driving voltages, respectively. OSC generates the clock signal for the whole driver IC.

3　Top-down design methodology of one-chip driver IC

3.1　Top-down design flow

Figure 2 shows the top-down design flow of a TFT-LCD one-chip driver IC. At the system design level, the whole chip is divided into several blocks according to the chip specification, such as digital block, analog block, and GRAM. These blocks can be described by their behavior models using a hardware description language such as Verilog-AMS or Spectre-HDL. At this level, full chip functional verifications can be completed by simulations of behavior models using a system verification platform, as shown in section 3.3. As a result, the design faults in the system design can be identified, and furthermore, the system properties can be optimized by modifying the behavior models of the blocks if needed. The behavior models of each block can be used as its specification in the lower level design.

The digital functional blocks are translated into lower level representation and analyzed. The RTL level model of all blocks was written by Verilog-AMS and verified by EDA tools. The gate level circuits were generated by logic synthesis while the functions are correct, and then the layout of the digital part is finished by automatic place and route.

Analog blocks and their interconnection are designed in the same way as digital blocks. In this case, standard analog libraries are prepared. The transistor level circuits are simulated by SPICE. The layout of analog blocks is generated from place and route by hand, while the simulation results of the transistor level are satisfied with design requirements.

GRAM design is divided into two facets. GRAM bodies are designed in the same way as analog circuits. The logic circuits, including the address process and controlling cell, are designed by digital circuit design methodology.

One-chip layout is integrated after the layout of digital, analog, and GRAM are finished. AC characteristic post simulation is necessary to check the timing of the digital circuit. If the performance of some blocks is out of specification, the upper level design will be modified until the timing is correct. The chip is taped out after the verifications of ERC, DRC, and LVS.

3.2 One-chip mixed-signal simulation

Verification of TFT-LCD one-chip driver IC is a serious challenge for designer and EDA tools[1]. The reasons are as follows. First, it is a mixed-signal VLSI including logic, analog, and GRAM. Second, the one-chip circuit scale is very large, with more than 3 million transistors. Third, the p-p voltage of the power supply ranges up to 32V, requiring many high voltage circuits and DC-DC converters. Last, the timing is complex and involves more than 100 controlling signals. In other words, verifications using traditional methods will occupy many resources, including computer space and simulation time. These issues directly influence the design period and the time-to-market. A simplified verification model, which includes representative blocks of the whole chip, is usually established to deal with these issues. However, the simulation results of a simplified model are unreliable to verify all behaviors of the full chip.

In order to solve these problems, a one-chip mixed-signal simulation is adopted. Different kinds of netlists such as Verilog-A/D, system-C model, SPICE netlist, and vector list are used for simulation at the same level or different levels. For example, behavior models of the cascade charge-pump circuits need to be inserted into verification model instead of the SPICE netlist so that the simulation speed is enhanced significantly.

3.3 System verification platform

A system verification platform is developed to verify system design and one-chip functions. For this system verification platform, the TFT-LCD panel is modeled by the C language, the analog block is modeled by Verilog-A, and the digital block and GRAM are modeled by Verilog-D. The simulation result of the display image using system verification platform is given in Fig. 3, in which source, gate, and common signals obtained by one-chip mixed-signal simulations are

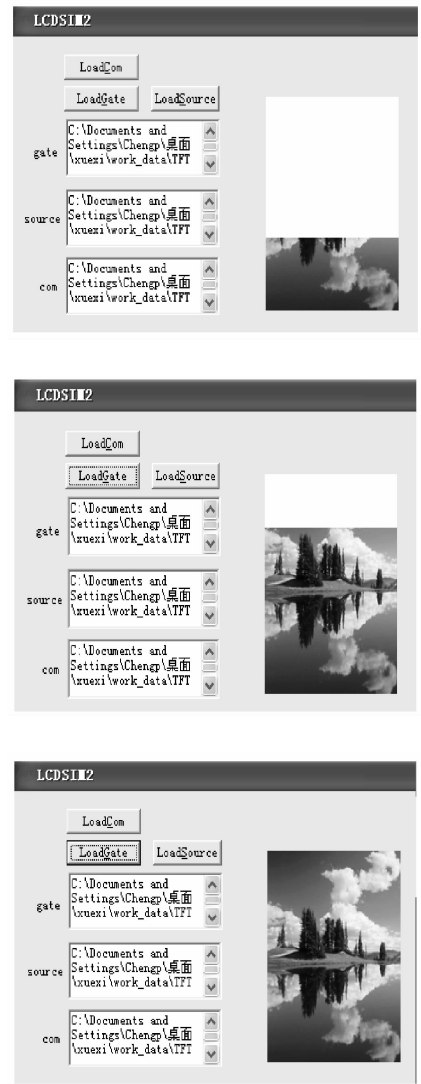

Fig. 3 Simulation result of display image by system verification platform

input to the TFT-LCD panel model to display image. This system verification platform can be used to detect system functional design faults and the Verilog-A/D model for the analog and digital block can be used as their design specification in the lower level design.

4 Key function IP blocks developments

4.1 Two-stage buffers driving architecture

For small TFT-LCD panels, the equivalent load is small and the driving circuits, including the source driver and γ-correction circuit, are different from that for large TFT-LCD panels. Driving buffers of one-chip driver ICs are usually placed to the outputs of the γ-correction circuit while the source driver block is only used as a digital-to-analog converter. The number of driving buffers is the same as the number of

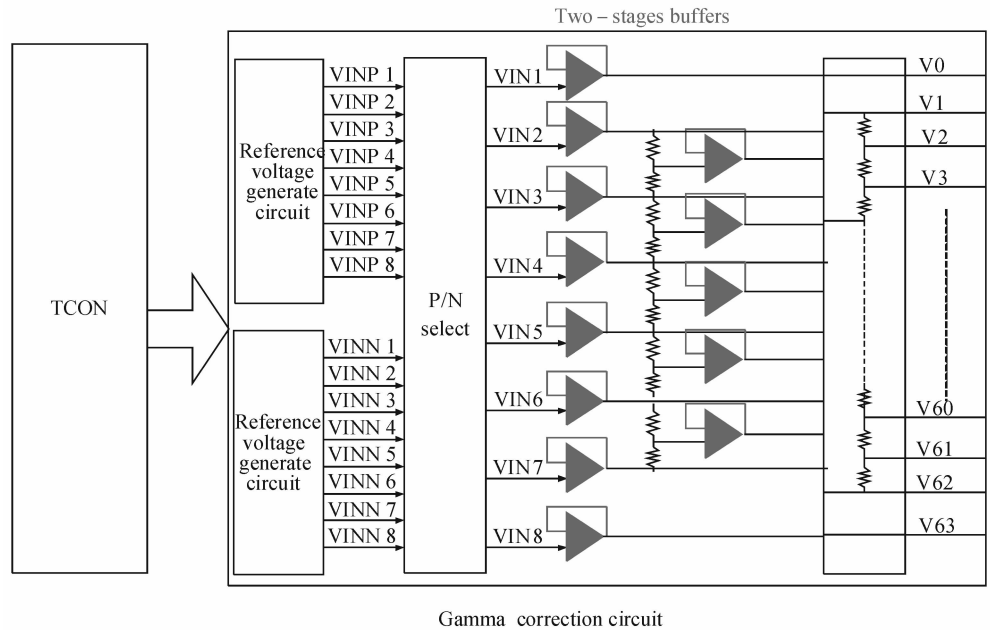

Fig. 4　Two-stage driving buffers architecture with 13 driving buffers[6]

grayscale voltages. In order to further reduce the power consumption and the die area, the traditional driving circuit can be simplified where the driving buffers are moved from the outputs of the γ-correction circuit to the outputs of the reference voltages circuit. For a 260k color TFT-LCD driver IC, the number of driving buffers can be reduced from 64 to 8.

However, the loads of driving buffers are changed. The resistance in the resistance-string of the γ-correction circuit is the new resistance load for the driving buffers, which is a main factor influencing the settling time of the output voltage of the source driver. Hence, we make a tradeoff among the settling time of the output voltage, the resistance of the γ-correction circuit, and the OPAMP buffer design. A new driving architecture is proposed as a simple solution[6], in which additional driving buffers are added as the second driving force into the γ-correction circuit at the proper place. This two-stage driving buffer architecture with 13 driving buffers is shown in Fig. 4.

4.2　Power supply circuits

The built-in power supply circuit is the most difficult part of TFT-LCD one-chip driver IC development. Its function is to generate driving voltages for the operation of the TFT-LCD panel and the power supply voltages for all circuits of the chip. The input voltages are VCC3 (2.0V to 3.3V) and VCI (2.5V to 3.3V), which are the power supply voltages of digital circuits and analog circuits, respectively. However, the specifications of the driving and power supply voltages are higher or lower than the input voltages. For example, the TFT ON voltage ranges up to 16V and the TFT OFF voltage ranges down to −16V. So, we need a DC-DC converter to generate voltages with different voltage amplitudes.

The driving voltages of the TFT gate are VGON and VGOFF, which are TFT ON and OFF voltage, respectively. VGON is the highest voltage of the chip. For the TFT structure of Cs-on-gate, VGOFF fluctuates between VGOFFH and VGOFFL for feedthough voltage reduction. Driving voltages of TFT source are grayscale voltages. VREG is the highest reference voltage for grayscale voltages. The driving voltage of the common line is VCOM, which fluctuates between VCOMH and VCOML. Power supply voltages of the analog circuit include positive voltage such as VCC, VDH, and VGH, and negative voltage such as VCL and VGL.

We design a specific block for every voltage generation. The built-in power supply diagram and the specification of voltages are shown in Fig. 5. Three LDOs are designed to generate VCC, VCI1, and VREG, and three charge pumps are adopted to generate VCL, VDH, VGH, and VGL. The functions of Vcom_drv and Vgoff_drv generate VCOM and VGOFF, respectively. Some accessorial blocks are needed for the illustrated circuits such as the bias circuit, band-gap, OSC, and non-overlap timing generating circuit. The bias circuit generates the reference bias voltage and current for the OPAMPs. The band-gap circuit generates the reference voltage of 1.2V with a low temperature coefficient. OSC is an RC oscillator to generate internal reference timing for logic operations and also for charge pumps.

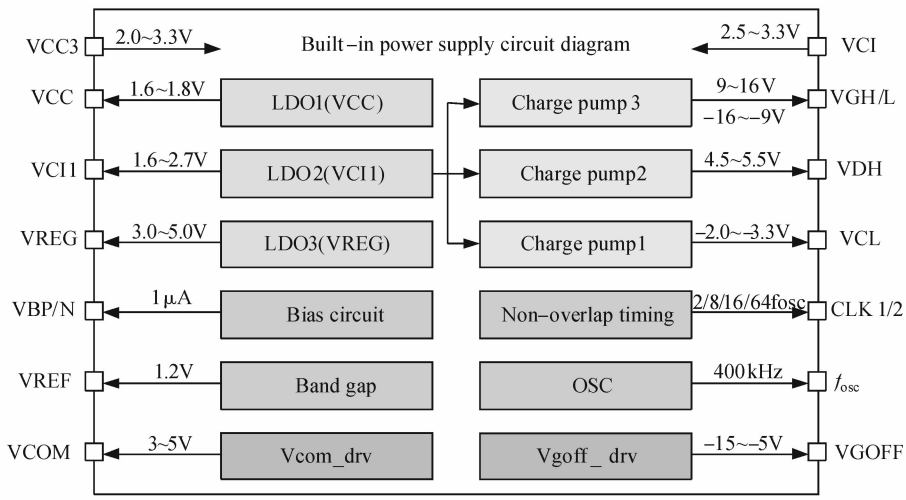

Fig. 5 Built-in power supply circuit diagram and the voltages

4.3 Other IP core development and design library

IP core reuse is a popular way to shorten design period when top-down flow is adopted. For a 260k color TFT-LCD one-chip driver IC, the specifications of source driver and gate driver change with the TFT-LCD panel resolution. However, some blocks, such as the built-in power supply circuit, GRAM, the each channel of the source drivers and gate drivers, can be reused even if the TFT-LCD panel resolution is changed. Thus, they can be made into IP cores, allowing these IP cores to be reused when a new product is developed.

The built-in power supply circuit generates the operational voltages and power supply voltages for all blocks. It is usually partitioned into four sub-blocks: LDO regulators, charge pumps, common line voltage (VCOM) driver, and TFT off voltage (VGOFF) driver. The driving ability of each voltage is considered to be optional when the circuit is made into an IP core. GRAM is used to store the digital display data for one frame image. The size of GRAM depends on the resolution of the TFT-LCD panel. However, GRAM is compatible with lower sizes so that the IP core of GRAM is widely used. The architecture of each channel for the source driver (with driving buffers moved into the gamma correction circuit) is fixed, even though the number of channels changes with different specifications. Therefore, the circuits of the source driver and gate driver are assembled by the building blocks of a single channel IP core. Other blocks such as the gamma correction circuit, timing generator, and OSC can probably be developed as IP blocks, but need configurable architectures.

5 Test and measurement

Based on top-down design methodology, a 260k color, 176RGB×220-dot TFT-LCD one-chip driver IC was successfully developed. All designed circuits are implemented by a 0.18μm HV CMOS process with a successful engineering sample at the first tape-out. The photograph of the developed chip is shown in Fig. 6 and the chip size is 20.635mm × 1.29mm. The static power dissipation is about 5mW for 262, 414-color display mode and 1.7mW for 8-color display mode. The settling time of the output grayscale voltage

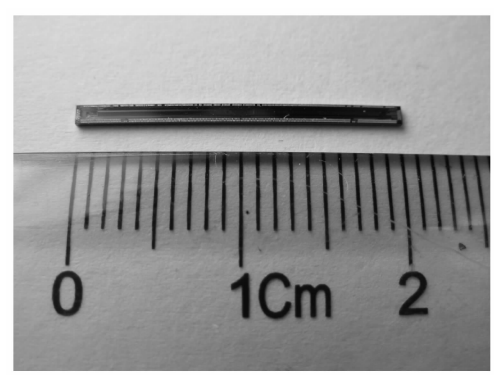

Fig. 6 Photograph of the developed chip

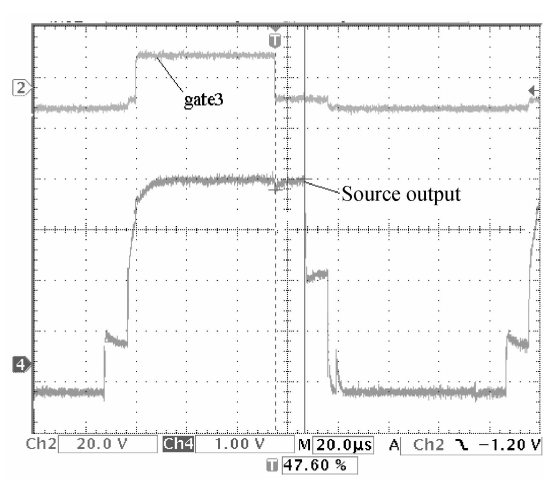

Fig. 7 Output waveforms of gate driver and source driver

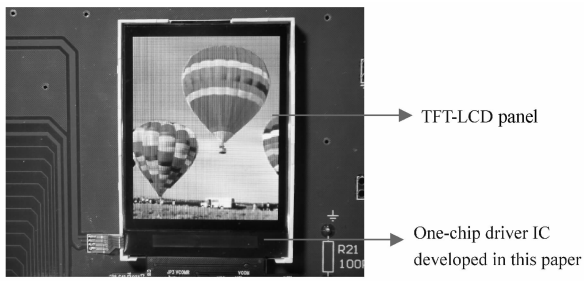

Fig. 8　Test picture of normal display in LCD module

Table 1　Main properties comparison with Hitachi HD66789

Properties	This IC	Hitachi HD66789
Power (no panel load)	5.0mW	7.5mW
Digital operating voltage	1.9V (built-in voltage regulator)	2.5～3.3V (outside supply voltage)
Minimum supply voltage	2.0V	2.5V
Output voltage deviation	＜±17mV	＜±30mV
γ-correction	4 parameter adjustable	3 parameter adjustable

within 0.2% error is less than 26μs (Fig. 7). The test picture of the normal display in LCD module using this driver IC is shown in Fig. 8.

A comparison of the main properties with a Hitachi HD66789 is listed in Table 1. Because this IC has a built-in voltage regulator (1.9V output voltage) and other low power analog circuits, such as two-stage driving buffers architecture, its power consumption and minimum supply voltage are less than that of the HD66789. Furthermore, since this IC has 4 parameter adjustable γ-correction and high precision driving buffers (less output voltage deviation), its display image quality is better than that of the HD66789. For mass production and commercial purposes, the die size and PAD arrangement of this IC are the same as that of the HD66789, namely, it is pin to pin compatible with the HD66789.

6　Conclusion

A top-down design methodology is proposed for the design of TFT-LCD one-chip driver ICs. A 260k color, 176RGB×220-dot TFT-LCD one-chip driver IC is successfully developed, which has advantages over present products, such as low power consumption, low supply voltage, and high image quality. All designed circuits are implemented by a 0.18μm HV CMOS process with a successful engineering sample at the first tape-out.

Since the TFT-LCD one-chip driver IC is a typical mixed-signal VLSI with more than 3 million transistors and implemented by a low/medium/high hybrid voltages CMOS process, the verification technology is challenging for the designer. We use a one-chip mixed-signal simulation and system verification platform to solve this problem for the top-down design flow. Development and reuse of IP cores is an effective solution for developing a TFT-LCD one-chip driver IC. The top-down design methodology and IP cores developed in this paper will be applied to product development.

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26 万色 TFT-LCD 单片集成驱动芯片的 Top-Down 设计*

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摘要：提出了应用于 TFT-LCD 单片集成驱动芯片的 Top-down 设计技术，并成功开发了一款 26 万色、176RGB×220 分辨率的 TFT-LCD 驱动芯片.该芯片是典型的混合信号超大规模集成电路芯片，采用 0.18μm HV CMOS 工艺制造.在 26 万色显示模式下，芯片的静态功耗是 5mW，输出驱动电压的建立时间(0.2%误差范围内)小于 26μs.

关键词：TFT-LCD；驱动 IC；top-down 设计；驱动电路；混合信号 VLSI

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