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OTFT with Bilayer Gate Insulator and Modificative Electrode*

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Abstract: An organic thin-film transistor (OTFT) with an OTS/SiO_2 bilayer gate insulator and a MoO_3/Al electrode configuration between gate insulator and source/drain electrodes has been investigated. A thermally grown SiO_2 layer is used as the OTFT gate dielectric and copper phthalocyanine(CuPc) is used as an active layer. This OTS/SiO_2 bilayer gate insulator configuration increases the field-effect mobility, reduces the threshold voltage, and improves the on/off ratio simultaneously. The device with a MoO_3/Al electrode has shown similar I_{ds} compared to the device with an Au electrode at the same gate voltage. Our results indicate that using a double-layer of electrodes and a double-layer of insulators is an effective way to improve OTFT performance.

Key words: organic thin film transistor; modified electrode; bilayer insulator; mobility
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1 Introduction

Organic field-effect transistors (OFETs) based on semiconductive materials have attracted increasing interest for their promising application to flexible, low cost, and large area displays, and electronic devices like smart cards due to the extraordinary electrical and mechanical properties of the small molecules[1~3]. Since the interface between the organic active material and the gate dielectric material is a critical part of the field-effect device, control over this interface is of great importance. Therefore, many methods of modifying the inorganic/organic interface have been explored to improve the growth of ordered vapor deposited films. We found that the characteristics of CuPc TFTs can be improved by using a self-organizing material like octadecyltrichlorosilane(OTS) between the SiO_2 gate dielectric and the CuPc active layer[4].

The silane coupling agent OTS is a particularly interesting material because it can bond to silicon oxide surfaces and form a Si—O—Si bond, which can influence deeply the characteristics of insulator films. In this paper, a solution technique was used to form OTS monolayers. High-quality OTS monolayers can also be spontaneously formed in solution through a simple chemical reaction. Then, we investigated the effect of OTS self-assembled monolayers(SAMs) on the characteristics of evaporated CuPc thin films[5~7], and observed that OTS SAMs not only depress the surface roughness of SiO_2 film but also decrease leakage current. Finally, we found that this method improved the organic/inorganic interface significantly and enhanced the performance of a CuPc organic thin film transistor.

Since the organic FETs are generally used for low-cost applications, the easy fabrication processes and the simplified structures are of great interest. In most of the literature, Au is used in the device as the electrode material because of its high work function, which can match that of many organic active materials. However Au is also a high price metal, which increases the cost of the device. If we can find a suitable cheaper alternative material and reduce the cost of manufacturing, then the work is of great significance. Although aluminum (Al) is a well-known contact material in integrated circuits, its low-work function precludes the application of Al to high performance OTFT for p-type semiconductors. In addition, high performance OTFTs can be achieved by inserting a transition metal oxide layer between Al electrodes and organic semiconductors. Following Chu *et al*.[8], we select MoO_3 as a modified layer of electrodes.

In this paper, we present the fabrication procedure and electrical characteristics of a FET using OTS/SiO_2 with the bilayer gate insulators modifying method and MoO_3/Al for the device modificative electrodes.

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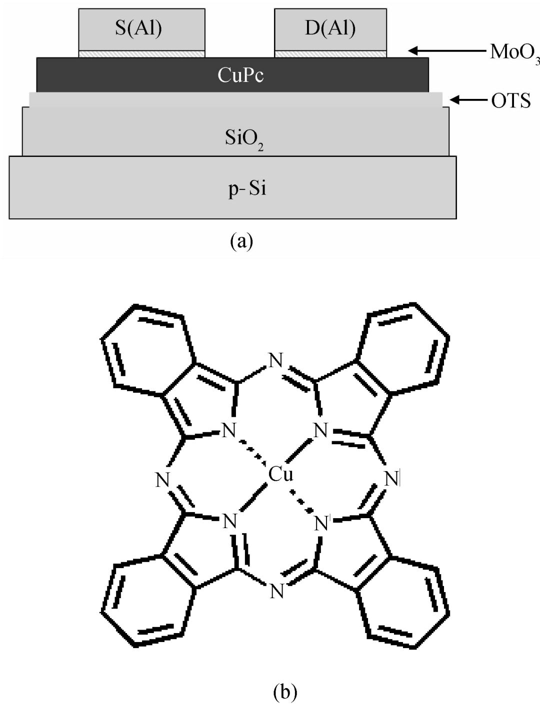

Fig. 1　(a) Schematic structure of the OTFTs; (b) Chemical structure of CuPc

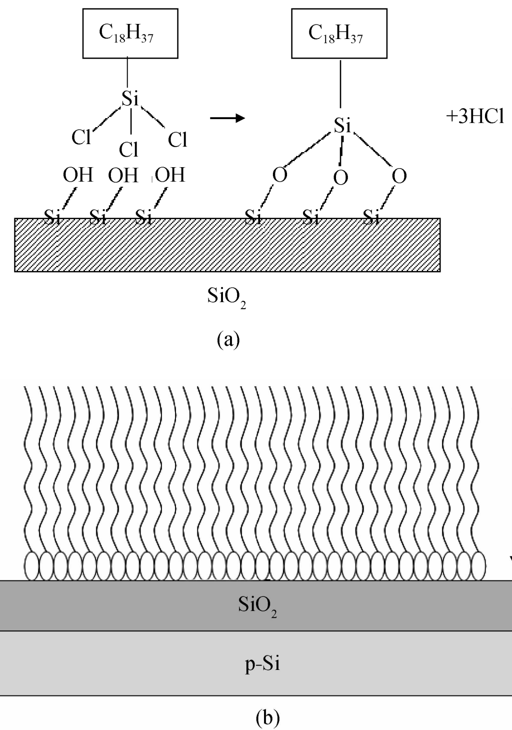

Fig. 2　(a) Chemical process between OTS and surface of SiO_2; (b) LB membrane schematic structure of OTS on surface of SiO_2

2　Experiment

The OTFT device structure used in this study is shown in Fig. 1(a). For simplicity, our devices were fabricated using a heavily doped silicon wafer as the substrate and gate electrode, with thermally grown silicon dioxide as the TFT gate dielectric. First, a 230nm thick thermal SiO_2 layer was grown as the OTFT gate dielectric (SiO_2 thickness was measured by ST2000-DLXn, Apectra Thick STD-Auto). The SiO_2 surface was ultrasonically cleaned with acetone, ethanol, and deionized water in that order, and subsequently the wafer was treated by UV for ten minutes. Then, the SiO_2 surface was treated with OTS by immersing the sample into a 0.5% solution of OTS (CH_3Cl : C_6H_{12} = 1 : 3) for 12 hours at room temperature in an anhydrous ambient. This chemical process is described in Fig. 2(a), which allows a monolayer of OTS to self-assemble on the surface of the SiO_2 and form an LB monolayer (the schematic structure is shown in Fig. 2(b)). The UV activates the Si—OH bond and makes the reaction occur more easily. A 40nm thick CuPc thin film (the chemical structure is shown in Fig. 1(b)) was then deposited by vacuum deposition at a rate of 2nm/min under a pressure of 6×10^{-4} Pa. It was purified twice using vacuum successive sublimation. Finally, the devices were completed by depositing Au or MoO_3/Al bilayer source and drain electrodes through a shadow mask (the thickness of the MoO_3 is 10nm). The electrodes were patterned to be 35μm in length and 2000μm in width.

The current-voltage characteristics of devices were measured by home-made transistor detection equipment. The measuring voltage (YJ32-2 Model) and accuracy of the micro-ammeter (HP-4140B Model) used in our experiments can reach ± 100V and 10^{-12} A, respectively. All experiments were carried out under dark conditions in ambient at room temperature.

3　Results and discussion

The *I-V* curves of OTFT have two working regions: the linear region and the saturated region. In this paper, the field-effect mobility is estimated in the saturation region using the equation:

$$I_{DS} = (W/2L)\mu C_i(V_G - V_T)^2$$

where W and L are the channel width and length, respectively, μ is the carrier mobility of the holes in the OTFT channel, C_i is the gate dielectric capacitance per unit area, and V_G, V_{DS}, V_T are the gate voltage, drain-source voltage, and threshold voltage, respectively.

Figures 3 (a) and (b) shows the *I-V* characteristics for a CuPc OTFT fabricated on untreated and OTS-treated oxidized silicon substrates held at room temperature. Clearly, a significant increase in current is observed in devices biased with the same V_G and V_{DS}. The plots in Fig. 4(a) show the characteristics of

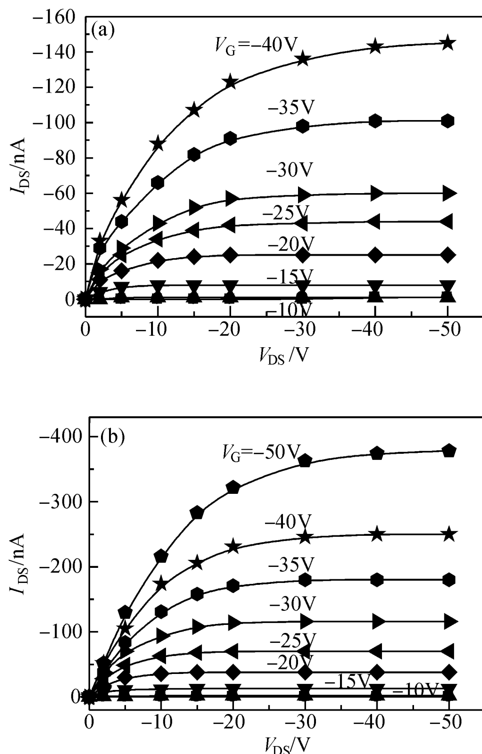

Fig.3 (a) Current-voltage characteristics of an OTFT device without an OTS layer; (b) Current-voltage characteristics of an OTFT device with an OTS layer

lgI_{DS} versus V_G at a fixed V_{DS} of −40V for the devices. Figure 4(b) shows the square root of the drain current $I_{DS}^{1/2}$ versus gate voltage V_G curve at a fixed

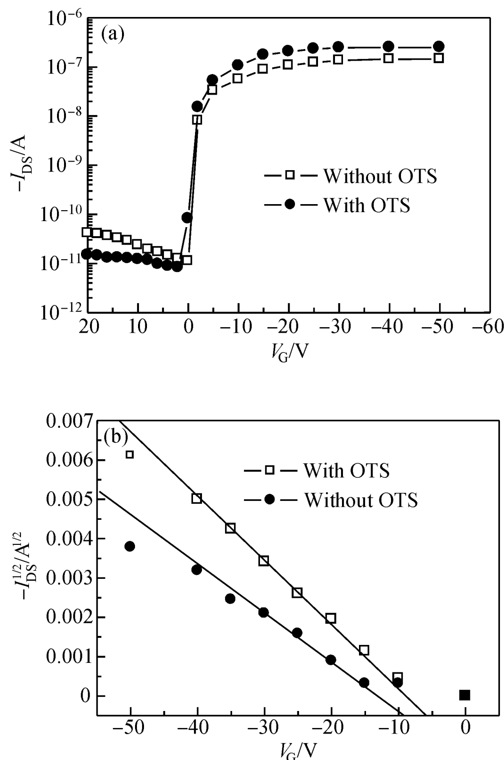

Fig.4 (a) I_{DS} versus V_G at a fixed V_{DS} of −40V for OTFT device; (b) $I_{DS}^{1/2}$ versus V_G at a fixed V_{DS} of −40V for OTFT device

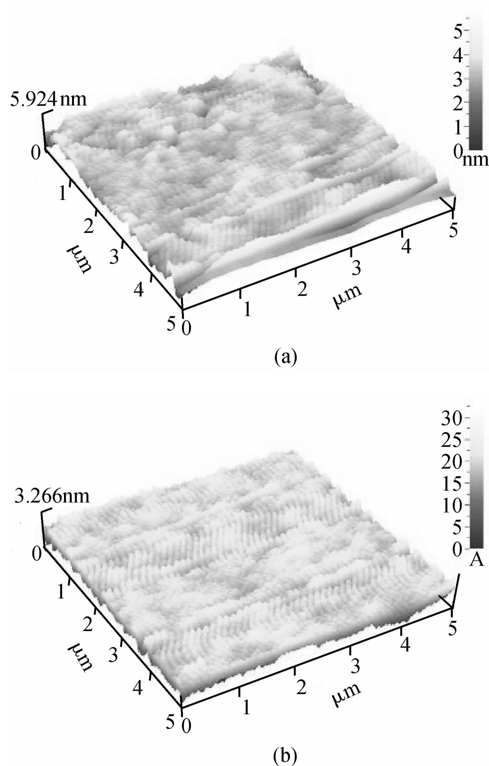

Fig.5 (a) AFM image of a 5μm square of untreated SiO_2 surface; (b) AFM image of a 5μm square of OTS-treated SiO_2 surface

drainsource voltage V_{DS} of −40V. From these four figures, we can conclude that OTFTs on untreated gate dielectrics have a field-effect mobility of 6×10^{-4} $cm^2/(V\cdot s)$, an on/off current ratio of about 10^3, and a threshold voltage of −9V. Meanwhile, OTFTs fabricated with OTS-treated gate dielectrics have a field-effect mobility as high as 1.5×10^{-3} $cm^2/(V\cdot s)$, an on/off current ratio of more than 10^4, and a threshold voltage of −6V. The above-mentioned results suggest that treating the SiO_2 surface prior to the CuPc active layer deposition with an OTS monolayer has been shown to improve noticeably the electrical characteristics of CuPc TFT.

The surface roughness of the insulator is critical to the OTFT device's performance because the regular morphology of thin film is important for the transport of carriers in the film. In our tests, the surface of the OTS-treated SiO_2 insulator was characterized with atomic force microscopy (AFM). Tapping-mode AFM was used to characterize the surface roughness and to image the surface effect, such as pinholes and defects. Figures 5(a) and (b) show that the OTS-treated SiO_2 layer is flatter than the bare SiO_2 layer and also show a considerable difference in surface roughness. Thus, the OTS shows an improved surface modified result.

For OTS-treated TFTs, another reason for the large improvement in OTFT performance using an

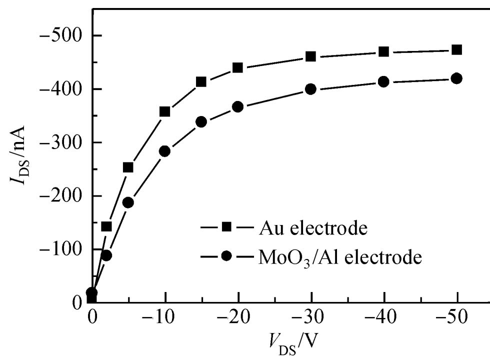

Fig. 6 Current-voltage characteristics of an OTFT device with Au and MoO_3/Al electrodes

OTS-treated SiO_2 gate dielectric is the altered film growth at the gate dielectric interface and adhesion of CuPc to the substrate. The OTS SAMs change the surface properties of the thermal oxide SiO_2 to a more hydrophobic surface with a low surface energy[9]. Secondly, the OTS SAMs perpendicular to the SiO_2 substrate would cause a preferential out-of-plane orientation of the evaporated CuPc molecules in an initial layer at the interface, which effectively improve the π-π stacking in the direction of current flow and lead to higher mobility. Therefore, the characteristics of CuPc organic TFTs can be improved with a silicon dioxide gate dielectric chemically modified with OTS monolayers. Importantly, the interface trap of organic film and inorganic insulator proved to be a limiting factor in OTFT performance. The results presented in this paper show clearly that the use of monolayers self-assembled at the interface is indeed a good method for improving the performance of the devices.

Field effect transistors require an ohmic source contact and an ohmic drain contact for ideal operation. In many real situations, the injection of charge carriers from metals into semiconductors can be an inefficient process, that is, non-ohmic, for example, Al to many of organic active materials such as CuPc, pentacene. This has an adverse impact on the performance of thin film transistors and makes the mobility of electrical measurements very poor because contact effects need to be disentangled from transistor properties. In this paper, to resolve this question, we adopt a vaporing thin MoO_3 film to modify the Al electrode layer and form double-layer electrodes. Figure 6 shows the current-voltage characteristics of OTFTs and MoO_3 covered with Al metal as the electrode. The source-drain current I_{DS} versus V_{DS} of the OTFT at the same V_G display very clear saturation currents as a function of the gate bias voltage and also show similar characteristics and performance compared to the Au electrode.

The introduction of the metal oxide MoO_3 in our OTFTs played an important role in decreasing the contact resistance. The measurement of work function based on the method of contact potential difference reported by our team showed that the work function of MoO_3 was 5.4eV, which is near that of CuPc (5.3eV). The small hole injection barrier from MoO_3 to CuPc resulted in strong hole injection. In addition, MoO_3 has a lower melting point and the ability of preventing Al metal diffusion into the organic material. These results demonstrate that the device with MoO_3/Al electrodes has a similar I_{ds} to the device with Au electrodes at the same gate voltage. Thus, using a transition metal oxide as the hole injection layer is an effective way to improve the characteristics of OTFTs.

4 Conclusion

We have fabricated bilayer gate dielectic organic TFTs with improved electrical characteristics, including a field-effect mobility as high as 1.5×10^{-3} $cm^2/(V\cdot s)$, an on/off current ratio of more than 10^4, and a threshold voltage of $-6V$. This OTS/SiO_2 bilayer gate insulator configuration increases the field-effect mobility, reduces the threshold voltage, and improves the on/off ratio at the same time. The device with MoO_3/Al electrodes has a similar I_{DS} to the device with Au electrodes at the same gate voltage. MoO_3/Al has been proven to be a superior electrode.

These results further increase the likelihood that organic thin film transistors will find use in low-cost electronic applications.

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具有双绝缘层和修饰电极的薄膜场效应晶体管*

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摘要: 研究了具有 OTS/SiO_2 双绝缘层结构及 MoO_3/Al 电极结构的有机薄膜晶体管. 器件是以热生长的 SiO_2 作为有机薄膜晶体管的栅绝缘层,酞菁铜作为有源层的. OTS/SiO_2 双绝缘层的结构提高了器件的场效应迁移率和开关电流比,降低了阈值电压. 实验表明在同样的栅极电压下,具有 MoO_3/Al 电极的器件和金电极的器件有着相似的源漏输出电流. 结果显示具有 OTS/SiO_2 双绝缘层及 MoO_3/Al 电极结构的器件能有效改进有机薄膜晶体管的性能.

关键词: 有机薄膜晶体管; 修饰电极; 双绝缘层; 迁移率
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