A 1.8V 10bit 100Msps Pipelined Analog to Digital Converter

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Abstract: A novel low-voltage, low constant-impedance switch is proposed, which not only eliminates the parasitic capacitor but also reduces the variation of switch "on" resistance. With the gain-boost technology, the operational transconductance amplifier used in this analog-to-digital converter (ADC) achieves enough DC gain and unity-gain frequency under the low voltage supply and to guarantee the performance of the sample and hold circuit (S/H) and the sub-stages. Based on these methods, a 10bit 100Msps pipelined ADC is fabricated in a 0.18μm CMOS process and operates under a 1.8V voltage supply. The ADC achieves an SNR of 54.2dB (input frequency of 6.26MHz) and an SNR of 49.8dB (input frequency of 48.96MHz) when the sampling frequency is 100MHz.

Key words: analog-to-digital converter; bootstrapped switch; gain-boosting technique
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1 Introduction

CMOS technology moves steadily towards finer geometries, which provide higher digital capacity, lower dynamic power consumption, and smaller area, resulting in integration of whole systems, or large parts of systems, on the same chip (system on chip, SoC). Speed and accuracy are two of the most important properties of analog to digital converters[1~4]. Most analog-to-digital converters employ a sample-and-hold circuit at the front end that achieves high speed, high linearity, and high precision with low-power dissipation. In a low voltage system, analog sampling becomes particularly difficult because the limited headroom severely degrades the tradeoffs among dynamic range, linearity, speed, and power dissipation. The performance of an S/H circuit is usually limited by the performance of sampling switches. Such factors as charge injection, clock feedthrough, and variation in the on-resistance of sampling switches can cause errors and introduce nonlinear distortion in the sampled voltage, resulting in a drop of sample-and-hold accuracy[5,6].

This paper presents a 10-bit 100Msample/s pipeline ADC that provides high dynamic performance for input signals. The ADC adopts an improved gate-bootstrapping technique for the SHA switches to sample input, a gain-boosting telescopic amplifier to achieve a desired and stable operation, and finally a comparator. This ADC is fabricated in SMIC 0.18μm 1P6M CMOS process, and the voltage supply is 1.8V.

2 ADC architecture

A 1.5-bit/stage architecture is adopted, which is specially designed for digital correction in the pipeline ADC. Such an architecture can adjust the offset error of the comparators so as to reduce the requirement of the comparators. Furthermore, this architecture is power efficient, and is widely used in 10bit ADCs. It requires the least closed-loop gain (equals to 2) for the OTA in each stage, which means a large feedback factor. With a relatively lower requirement for both speed and gain, the OTA can work with the lowest GBW and, thus, the lowest power consumption.

Our ADC is composed of 8 1.5-bit stages and a 2-bit flash ADC as the final stage. The main blocks include an S/H circuit, a multiplying digital-to-analog converter (MDAC), a digital correction block, a clock generator, and a bandgap reference voltage generator. The main blocks and the architecture are presented in Fig. 1.

3 Circuit implementation

In this design, we focus on the requirement of speed, resolution, noise, power consumption, the choice of the circuit architecture, and the design under a low supply voltage. The requirement of both high speed and high resolution makes it necessary for the OTA to have high DC gain and high unit-gain frequency. The adoption of the 0.18μm channel length

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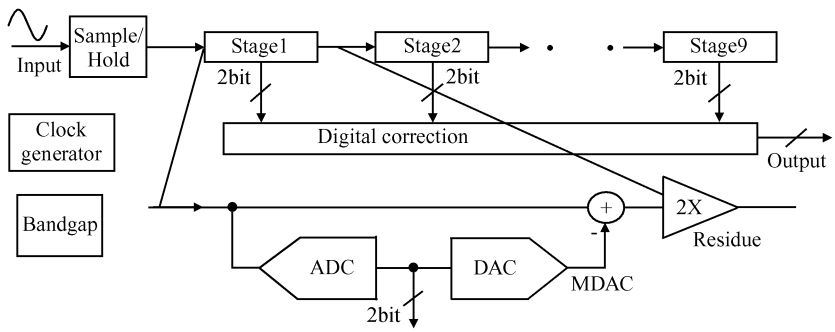

Fig. 1 Architecture of the ADC

brings about the high speed of the CMOS transistor, but makes it difficult to achieve high DC gain due to a smaller intrinsic MOS transistor gain. On the other hand, the 1.8V supply voltage helps to attain the advantage of low power consumption but at the same time provides severe output swing for the OTA.

3.1 Sample/hold circuit

The flip-around S/H circuit is used in this ADC (shown in Fig. 2), in the front of which a bootstrap switch circuit is adopted in order to improve the linearity of the sample switch. In the sample phase, the signal is sampled into the capacitors C_s. In the hold phase, C_s functions as the feedback capacitor and the signal is transferred to the output of the OTA and remains in that phase to provide to the first stage for processing.

Compared with another widely used S/H architecture, the charge-transferring S/H, this architecture has only half the number of capacitors while the feedback factor is as twice as high. Because of these two characteristics, this architecture occupies less area and provides two other advantages: lower power consumption and lower noise[7]. However, despite its advantages, there is also one drawback[7]. While in the charge-transferring S/H architecture, only the differential charge is transferred into the feedback capacitors, in the flip-around S/H both the differential charge and the common-mode charge are transferred because the input capacitor C_s in the sample phase is also used as the feedback capacitor during the hold phase. With a CMFB circuit, the common-mode voltage at the output of the OTA remains unchanged, which means that the common-mode voltage at the input of the OTA has to change according to:

$$\Delta V_{\text{in\_cm}} = V_{\text{out\_cm}} - V_{\text{sig\_cm}} \tag{1}$$

where $V_{\text{sig\_cm}}$ is the common-mode voltage of the signal and $V_{\text{out\_cm}}$ is the common-mode voltage at the output of the OTA. Such changes of the common-mode voltage at the input require the OTA to be carefully designed.

The most widely used bootstrapped switch in ADC applications[5,6] is shown in Fig. 3. This circuit eliminates the distortion source of overdrive voltage and achieves the rail-to-rail swing at low voltage supply. However, the variation in the "on" resistance of the switch dominates the distortion performance. Various techniques have been proposed to improve the linearity and "on" resistance of the switch. For example, Reference [8] uses a dual-channel bootstrapped switch to eliminate nonlinear distortion. In Ref. [7], it proposes a sampling switch circuit that enables the precise sampling of input signals greater than the chip supply voltage with no static power consumption, and without activating on-chip parasitic body diodes. However, these circuits are costly or cannot sufficiently eliminate nonlinear distortion.

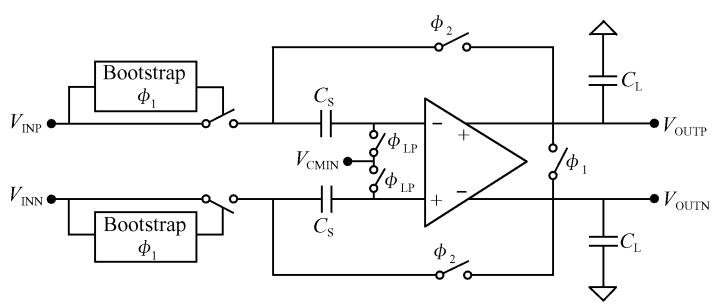

Fig. 2 Sample/hold circuit

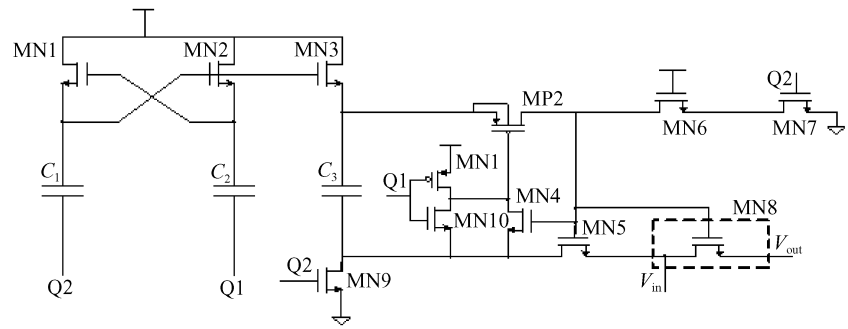

Fig. 3　Conventional nMOS bootstrapped switch

The proposed bootstrapped switch is shown in Fig. 4 and consists of two main elements: a clock booster and an nMOS-type bootstrapped switch. The clock booster is actually a charge pump. The circuit operates on a two-phase non-overlapping clock signal Q1 and Q2 that turns the sampling switch MN7 on and off. During the off state, Q1 is low and Q2 is high. Devices MN5 and MN6 discharge the gate of MN7 to ground. Meanwhile, V_{DD} is applied across capacitor C_3 by MN3 and MN8. This capacitor will act as the battery across the gate and source during the "on" phase. When Q1 goes high, MP4 pulls down the gate of MP2, allowing charge from the battery capacitor C_3 to flow onto gate G. This turns on both MN4 and MN7. MN4 enables gate G to track the input voltage V_{in} shifted by V_{DD}, keeping the gate-source voltage constant regardless of the input signal.

In fact, in the Q1 state, C_3 stores enough charge to reach the boosted voltage. In conventional switches, the voltage is significantly reduced for charge sharing by the parasitic capacitances associated with the two plates of C_3. The voltage can be simplified to:

$$V_{GS,MN7} = \frac{C_3}{C_3 + C_p} V_{DD} \tag{1}$$

In Fig. 4, there are three methods for reducing the parasitic capacitances and "on" resistance. First, the proposed bootstrapped switch replaces MN10 in Fig. 3 with C_4, which connects the drain of MP1 and the clock of Q2. This method prevents the parasitic capacitance C_p from connecting with the bottom of C_3 significantly. Second, MP4 substitutes for MN4, and the gate of MP4 is controlled by the clock Q2. This method disconnects the boosted switch MN7 and MN4 in order to decrease the parasitic capacitance that exists in the gate of MN7. It also reduces the variation of the "on" resistance. Third, the device MP3 is designed to turn off the MN6 during the "on" state and reduce the V_{gs} of the device MN5. This method can also decrease the parasitic capacitance C_p and the rise time.

In practice, fully differential circuit topologies reduce the influence of charge-injection and clock feed-through in any sample-and-hold circuit. Furthermore, a differential mode switch will reduce the total harmonic distortion, THD, as all even order harmonics are cancelled. Thus, in differential mode, Figure 5 shows the simulated waveforms of the S/H circuits based on the proposed design with a sampling speed of 100MHz and an input frequency of 48.9453MHz. The SFDR is about 84.5dB, which is sufficient for 10bit resolution. Figure 6 shows the on-resistance for the two kinds of switched discussed above. The resistance of the conventional switch is about 38Ω, while the resistance of the proposed switch is 12Ω, indicating that the proposed switch has much larger bandwidth.

3.2　Differential gain-boosting folded cascode OTA

The folded cascode OTA is employed in the S/H

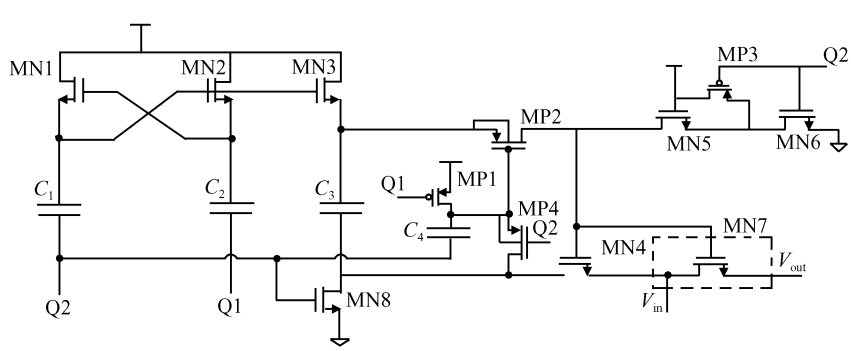

Fig. 4　Proposed bootstrapped switch

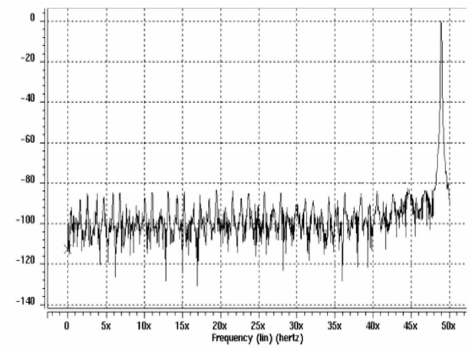

Fig. 5 FFT of the proposed bootstrapped switch

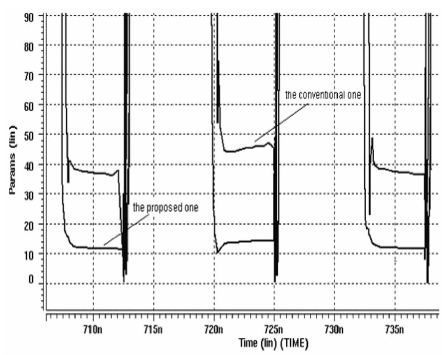

Fig. 6 On-resistance of switch

circuit and the sub-ADCs. The implementation is shown in Fig. 7 (CMFB is not shown for simplicity). Due to the requirement of a high DC gain under low voltage supply, the cascade OTA is a good choice because it provides a sufficiently high DC gain and a large output swing. A two-stage cascade OTA such as the design in Ref. [9] is widely used. However, this architecture achieves relatively low unity-gain frequency and, thus, low speed because of the frequency compensation.

Therefore, the cascode OTA is adopted to provide enough unity-gain frequency. In order to accommodate the large range of signal common mode that is required by the flip-around architecture of the T/H circuit, the folded cascode OTA is chosen. Compared with the telescopic cascode OTA, which is also often

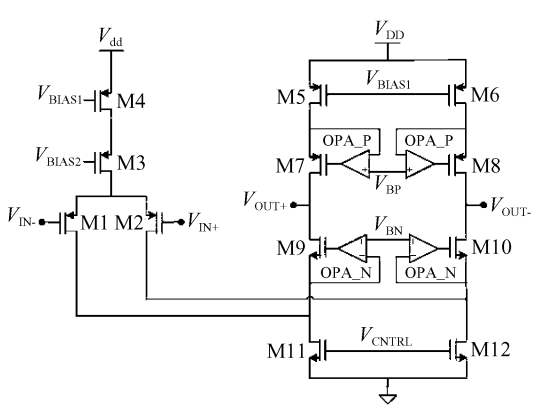

Fig. 7 Gain-boosting folded cascode OTA

used in high-gain applications, the common mode of the input can be more freely chosen. Furthermore, this architecture has a higher signal swing range, which is important under voltage supply as low as 1.8V.

However, this architecture also has its drawbacks, including higher power consumption, lower open-loop gain, and lower unity-gain frequency. These disadvantages can be overcome or alleviated with the adoption of a lower voltage supply and smaller device dimensions, thus decreasing the capacitance at the critical nodes and the gain-enhancing technology such as the gain-boost technology used in this OTA.

3.2.1 Decision of the capacitors

The decision of the capacitors is mainly considered from the requirement of the noise tolerance. The noise generated by the T/H circuit directly degrades the SNR, and should be treated as the main noise source. The noise of the T/H circuit is composed of two parts: the noise of the OTA and that from the sampling switch[10~12].

The noise of the OTA, which primarily comes from MOSFET M1, M2, M5, M6, M11 and M12, and the close-loop noise, can be expressed as:

$$\overline{V}_{\mathrm{n,opa}}^2 = N\gamma \times \frac{1}{f} \times \frac{kT}{C_{\mathrm{Leff}}} \tag{2}$$

where $N = 2(1 + g_{\mathrm{m5}}/g_{\mathrm{m1}} + g_{\mathrm{m11}}/g_{\mathrm{m1}})$, f is the feedback factor, γ is the thermal noise factor, C_{Leff} is the effective load capacitance, and the value is:

$$C_{\mathrm{Leff}} = (1-f)C_{\mathrm{s}} + 2C_{\mathrm{s\text{-}next}} + C_{\mathrm{CMFB}} + C_{\mathrm{out}} \tag{3}$$

where C_{s} is the sampling capacitor of the T/H circuit, $C_{\mathrm{s\text{-}next}}$ is the sampling capacitor of the first stage, C_{CMFB} is the capacitance of the CMFB, and C_{out} is the capacitance of the output, including the parasitic capacitance and the capacitor of the comparator.

For the S/H circuit, the total noise can be expressed as

$$\overline{V}_{\mathrm{n,S/H}}^2 = 2\frac{kT}{C_{\mathrm{s}}} + N\gamma \times \frac{1}{f} \times \frac{kT}{C_{\mathrm{Leff}}} \tag{4}$$

where $2kT/C_{\mathrm{s}}$ is the noise of the sampling switch. The noise of the T/H circuit should be less than the quantify noise, $(\mathrm{FS}/(2^B-1))^2/12$, where FS is the range of the input signal.

In this design, $g_{\mathrm{m5}}/g_{\mathrm{m1}} \approx 1/3$, $g_{\mathrm{m11}}/g_{\mathrm{m1}} = 2/3$, γ is assumed to be 3 in the 0.18μm CMOS process, $C_{\mathrm{CMFB}} = 0.2\mathrm{pF}$, $C_{\mathrm{out,p}} = 0.2\mathrm{pF}$, $C_{\mathrm{com}} = 0.1\mathrm{pF}$, FS = 1V, $B = 10$, and C_{s} is:

$$C_{\mathrm{S}} > 0.46\mathrm{pF} \tag{5}$$

Because of the critical contribution of the S/H to the total noise, C_{s} is set larger, and the value is 1.2pF. Based on the value we choose for the capacitors, we calculate the value of the effective load capacitor C_{Leff} to be 1.85pF.

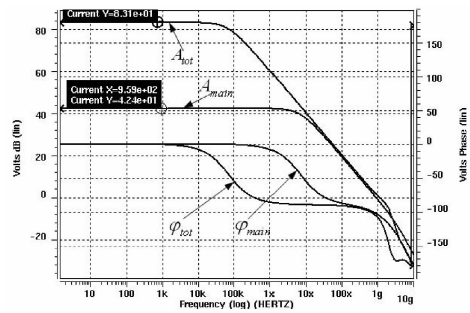

Fig. 8　Simulated frequency response for the whole OTA

In the case of the sampling capacitor of the MDAC, the calculation is similar. Because the contribution of the noise is relatively small, the capacitance is chosen as 0.5pF.

3.2.2　Simulated result of the whole OTA

Figure 8 shows the frequency response of the entire OTA with a load capacitance of 1.85pF. The DC gain is 83.1dB, the unity-gain frequency is 1.2GHz, and the phase margin is 70°. Figure 8 compares the frequency response of the OTA with and without the adoption of the gain-boosting technology. The whole OTA has nearly the same unity-gain frequency and the same phase margin as that without the gain-boosting OTA, but the DC gain is greatly increased.

3.3　Comparator

The current-mirror comparator with dynamic latch is adopted and shown in Fig. 9[13]. When CK is low, the comparator begins to work. It compares the input signal V_{IN1} and V_{IN2}, and transfers them into the current signal I_1 and I_2, which are then mirrored as current through M5 and M6. As shown in the figure, the size of M5 and M6 is twice as large as M4 and M7, and thus $I_3 = 2I_1$, $I_4 = 2I_2$. The current used to charge the input capacitance of the latch is doubled, increasing the speed of the comparator.

When CK is high, M8 is switched on, and VO = NVO. Because M9 is off, the latch is inactive, and the process of restoration is fast.

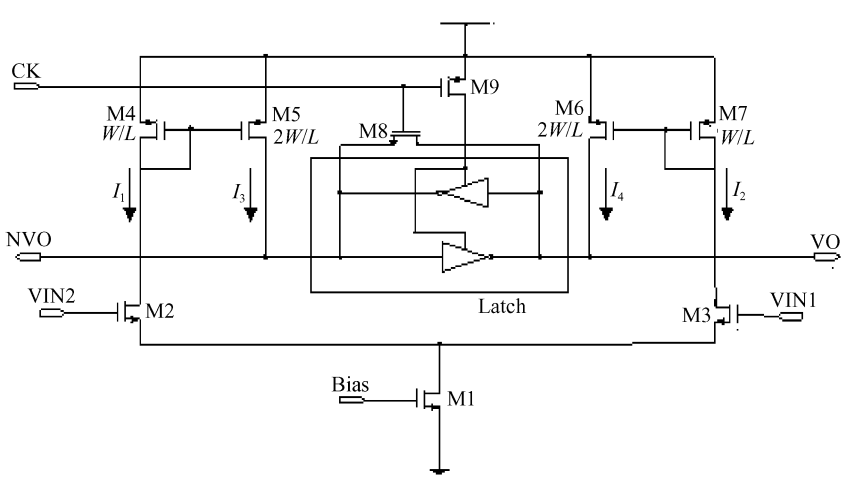

Fig. 9　Comparator

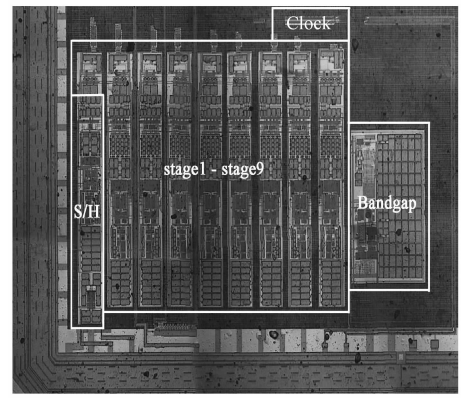

Fig. 10　Micrograph of the ADC

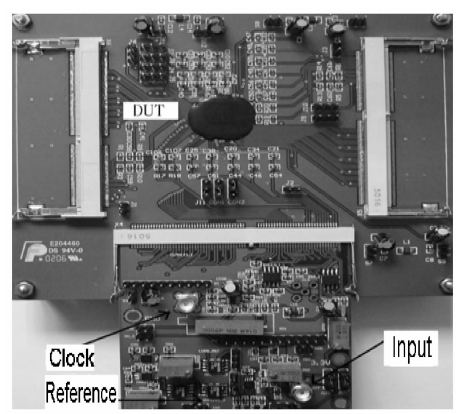

Fig. 11　Test board of the ADC

4　Experimental results

The pipelined ADC was fabricated in a SMIC 0.18μm 1P6M CMOS process, and the voltage supply is 1.8V. The micrograph of the ADC is shown in Fig. 10. The core without the I/O pad occupies an area of 2.98mm^2. Figure 11 is the test board of the proposed ADC.

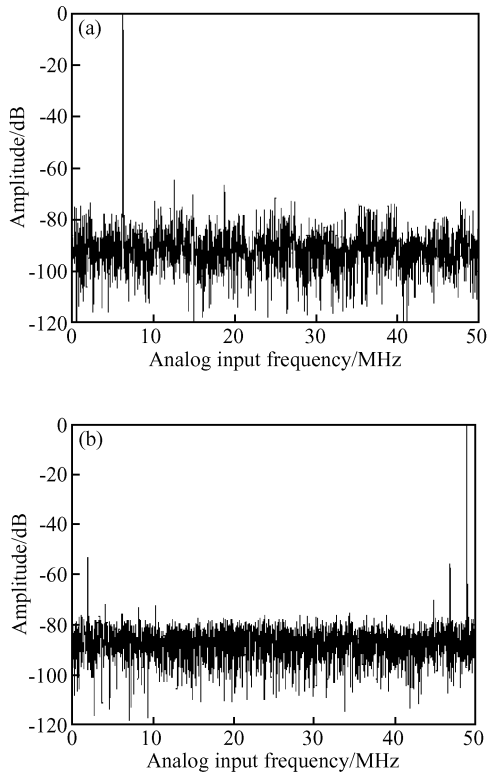

Fig. 12 Tested output spectrum (a) f_{in} = 6.26MHz; (b) f_{in} = 48.96MHz

Figure 12 shows the tested output spectrum at the input frequency of 6.26MHz and 48.96MHz with the sampling frequency of 100MHz. The results show that the ADC can achieve an SNR of 54.2dB at the input frequency of 6.26MHz and an SNR of 49.8dB at the input frequency of 48.96MHz. Table 1 summarizes the performance of the pipelined ADC. Table 2 shows that this work has good dynamic performance in comparison with AD9040 and AD9050.

Table 1 Measured results of the ADC

Parameter	Typical
Supply voltage	1.8V
Resolution	10Bit
Power consumption	92mW
Sample rate	100MHz
Technology	0.18μm 1P6M CMOS process
SINAD @6.26MHz @48.96MHz	54.2dB 49.8dB
SFDR @6.26MHz @48.96MHz	64.5767dB 60.07dB
Core area	2.98mm^2

Table 2 Comparison with previous work

	Resolution /bit	Conversion rate/MHz	Power /mW	SNR /dB	Supply voltage /V
This work	10	100	92	54.2	1.8
AD9040	10	40	940	53	5
AD9050	10	60	345	53	5

5 Conclusion

This paper describes the implementation of a pipeline analog-to-digital converter in 180 nm technology operating under a 1.8V supply voltage. For the ADC to achieve high-performance, advanced technology should be adopted and the circuits should be carefully designed. A novel low-voltage low constant-impedance switch is proposed in this paper, which not only eliminates the parasitic capacitor but also reduces the variation of the switch "on" resistance. With the gain-boost technology, the operational amplifier used in this analog-to-digital converter (ADC) achieves enough DC gain and unity-gain frequency under the low voltage supply and thus guarantees the performance of the sample and hold circuit (S/H). This ADC is useful for wideband visual and communication systems.

References

[1] Le B, Rondeau T W, Reed J H, et al. Analog-to-digital converters. IEEE Signal Processing Magazine, 2005, 22(6): 69
[2] Le B, Rondeau T W, Reed J H, et al. Analog-to-digital converters. IEEE Signal Processing Magazine, 2005: 69
[3] Hirotomo I, Ken T, Tetsuya I. A 1.0V 40mW 10b 100MS/s pipeline ADC in 90nm CMOS. IEEE 2005 Custom Integrated Circuits Conference, 2005: 388
[4] Bjornar H, Atle B, Terje N A, et al. A 1.2V 220MS/s 10b pipeline ADC implemented in 0.13μm digital CMOS. IEEE Solid-State Circuits Conference, 2004: 256
[5] Abo A M, Gray P R. A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J Solid-State Circuits, 1999, 34: 599
[6] Abo A M. Design for reliability of low-voltage, switched-capacitor circuits. PhD Dissertation, University of California, Berkeley, CA, 1999
[7] Yang C Y, Hung C C. A low-voltage low-distortion MOS sampling switch. IEEE Proc Int Symp Circuits and Systems, Kobe, Japan, 2005, 5: 3131
[8] Wang L, Yin W J, Xu J, et al. Dual-channel bootstrapped switch for high-speed high-resolution sampling. Electron Lett, 2006, 42(22): 1275
[9] Yang W, Kelly D, Mehr I, et al. A 3-V 340mW 14-b 75Msample/s CMOS ADC with 85-dB SFDR at Nyquist input. IEEE J Solid-State Circuits, 2001, 36: 1931
[10] Aksin D, Al-Shyoukh M, Maloberti F. Switch bootstrapping for precise sampling beyond supply voltage. IEEE J Solid-State Circuits, 2006, 41: 1938
[11] Liu M H, Ou W Y, Su T Y, et al. A 1.5V 12-bit 16MSPS CMOS pipelined ADC with 68dB dynamic range. Analog Integrated Circuits and Signal Processing, 2004, 41: 269
[12] Bult K, Geelen G J G M. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. IEEE J Solid-State Circuits, 1990, 25: 1379
[13] Yoo S M, Park J B, Lee S H, et al. A 2.5-V 10-b 120-MSample/s CMOS pipelined ADC based on merged-capacitor switching. IEEE Trans Circuits Syst II, 2004, 51(5): 269

一种 1.8V 10 位 100Ms/s 流水线模数转换器设计

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摘要：针对自举开关中的寄生效应和导通电阻的非线性问题提出了一种新的低压低电阻的自举开关.同时利用增益增强技术设计高直流增益和高单位增益带宽的运放，从而保证采样保持电路和子级电路的性能.基于以上技术，设计了一个 10 位 100Ms/s 流水线模数转换器，该模数转换器用 0.18μm CMOS 工艺流片验证.经测试，该模数转换器可以在采样率为 100MHz，输入频率分别为在 6.26 和 48.96MHz 的情况下分别获得 54.2 和 49.8dB 的信噪比.

关键词：模数转换器；自举开关；增益提升电路

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