# A CMOS Voltage Reference Based on $V_{GS}$ and $\Delta V_{GS}$ in the Weak Inversion Region

Xia Xiaojuan†, Xie Liang, and Sun Weifeng

(*National ASIC System Engineering Research Center, Southeast University, Nanjing* 210096, *China*)

**Abstract**: A CMOS voltage reference, which is based on $V_{GS}$ and $\Delta V_{GS}$ in the weak inversion region, has been designed and implemented in standard 0.6$\mu$m CMOS technology. No diodes and parasitic bipolar junction transistors (BJTs) are used. The proposed voltage reference uses a current-mode topology by summing a PTAT current and a CTAT current into a resistor to generate the required reference voltage. It can also provide more than one reference voltage output, which is quite suitable for systems requiring many different reference voltages simultaneously. The occupied chip area is 0.023mm$^2$. The operation supply voltage is from 2.5 to 6V, and the maximum supply current is 8.25$\mu$A. The designed three different outputs are respectively about 203mV, 1.0V, and 2.05V at room temperature when the supply voltage is 4V. The circuit achieves a temperature coefficient of 31ppm/℃ in the temperature range of 0 to 100℃ and an average line regulation of ±0.203%/V. The voltage reference has been successfully applied in a white LED backlight driver chip.

**Key words**: CMOS voltage reference; CTAT current; PTAT current; temperature coefficient; weak inversion region
**EEACC**: 1265B; 2570D
**CLC number**: TN791 **Document code**: A **Article ID**: 0253-4177(2008)08-1523-06

## Nomenclature

| | |
|---|---|
| $C_D$ | Depletion capacitance |
| $\mu$ | Mobility |
| $W$ | Transistor channel width |
| $L$ | Transistor channel length |
| $S$ | $W/L$, transistor width and length ratio |
| $V_t$ | Thermal voltage, $kT/q$ |
| $A$ | Subthreshold current parameter |
| $V_{DS}$ | Drain-source voltage |
| $V_{GS}$ | Gate-source voltage |
| $I_D$ | Drain current |
| $V_{TH}$ | Threshold voltage |
| $V_{THN}$ | Threshold voltage of nMOS transistor |
| $V_{THP}$ | Threshold voltage of pMOS transistor |
| $\phi_F$ | Fermi potential |
| $\phi_S$ | Surface potential relative to the source |
| $V_S$ | Source to substrate voltage |
| $V_D$ | Drain to substrate voltage |

## 1 Introduction

Voltage references with low sensitivity to the temperature and supply are commonly required both in analog and digital circuits such as A/D, D/A, flash memories, and so on. Since the first bandgap reference was proposed by Pease in 1971[1], several bandgap voltage references have been reported for use in a wide range of applications. In these designs, an output voltage with low sensitivity to temperature is obtained as the sum of a voltage of a forward-biased diode having a negative temperature coefficient and a voltage proportional to absolute temperature (PTAT), which is realized by amplifying the voltage difference of two forward-biased base-emitter junctions[2,3].

In CMOS technology, a parasitic vertical bipolar junction transistor (BJT) formed in a p- or n-well is commonly used to implement a bandgap reference. However, BJTs present several problems in the implementation of bandgap references. For example, the parasitic BJT in a CMOS process is usually not very well characterized, the output voltage of the bandgap voltage reference is always fixed since the base of the parasitic transistor is grounded, and most bandgap structures only offer a single output voltage. In Ref. [4], a low temperature drift reference voltage obtained by mutually compensating the temperature drifts of threshold voltage and mobility was presented. Although it was implemented without BJTs and the output voltage was different from 1.25V, the temperature dependence was governed by a linear term and a nonlinear term. In Ref. [5], a current mode voltage reference was developed in which two currents with different temperature coefficients were summed into a resistor to create a voltage reference. The output voltage can be easily changed as the resis-

† Corresponding author. Email: xiaxj@seu.edu.cn
Received 15 October 2007, revised manuscript received 8 April 2008

tor changes. References [6,7] also reported a sub-1V bandgap voltage reference rather than 1.25V. But in Refs. [5～7], BJTs were used. The work reported in Ref. [8] developed a voltage reference based on subthreshold MOSFETs without any BJTs. The average output voltage was about 295mV. However, the circuit structure can only offer a single output with a good temperature coefficient because it uses a voltage summing mode topology.

In this paper, a new architecture for a precision voltage reference in standard CMOS technology based on $V_{GS}$ and $\Delta V_{GS}$ in the weak inversion region is presented to overcome the problems described above. The voltage reference does not use any BJTs or diodes. It uses a current-mode topology and derives its temperature independent characteristic from two temperature dependent currents that are summed together into a resistor to generate the reference voltage. Two linear currents are combined to generate a reference voltage that is stable with temperature. One is proportional to absolute temperature (PTAT) associated with $\Delta V_{GS}$ in the weak inversion region, while the other is conversely proportional to the absolute temperature (CTAT) associated with $V_{GS}$ in the same work region. The reference circuit has been realized in a standard 0.6$\mu$m double poly double metal (DPDM) n-well CMOS process. The detailed circuit principle, structure, and the experimental results are presented in the following sections.

## 2 CMOS voltage reference

The MOS transistor has two primary regions of operation in which current flows from the source to the drain: one is the weak inversion region and the other is the strong inversion region. The weak inversion region occurs when the gate-source voltage $V_{GS}$ is less than the threshold voltage. In the weak inversion region, there are two important temperature dependent parameters: $V_{GS}$ and the difference gate-source voltage between two MOSFETs, $\Delta V_{GS}$.

Considering these two temperature factors in the weak inversion region, we introduce a novel CMOS voltage reference with a new circuit structure based on $V_{GS}$ and $\Delta V_{GS}$. The proposed voltage reference uses a current-mode topology by summing a PTAT current and a CTAT current into a resistor to generate the reference voltage. The temperature coefficients are cancelled and the resulting voltage can also be adjusted to the desired output reference voltage by changing the circuit parameters.

The complete schematic of the proposed CMOS voltage reference is shown in Fig. 1. It is composed of four sub-circuits: the startup circuit, PTAT current generator, CTAT current generator, and reference voltage generator.

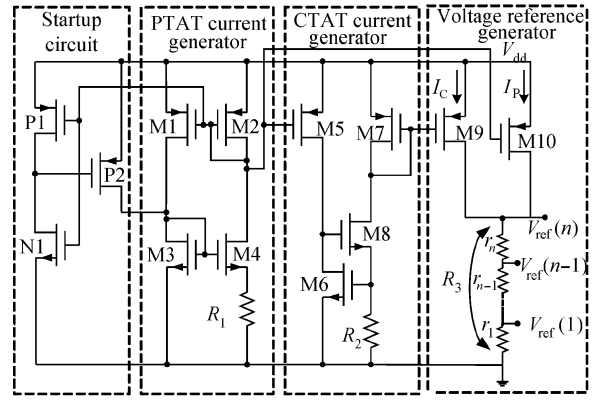


Fig. 1 Complete schematic of the proposed CMOS voltage reference

### 2.1 Startup circuit

A startup circuit is designed to ensure the circuit works properly, as shown in Fig. 1. It is formed by two pMOS transistors P1, P2 and one nMOS transistor N1. When the circuit operates in the zero-current state, the gate voltages of M1, M2, and P1 are close to the supply voltage $V_{dd}$. P1 and N1 function as an inverter. The drain voltage of N1 is pulled low, and this turns on P2 to inject a small current to the PTAT generator. Thus the startup circuit enables the entire circuit. Furthermore, as the gate voltage of M1 decreases, P1 will be turned on and then P2 is turned off. Thus, the startup circuit is disabled after the reference works properly. The design of nMOS transistor N1 is very critical. In order to cut off the transistor P2 completely after startup, the $W/L$ ratio of N1 must be chosen to be much less than 1.

### 2.2 PTAT current generator

The PTAT current generator in this paper is made up of transistors M1～M4 and resistor $R_1$. M3 and M4 operate in the weak inversion region. Assuming the channel length is sufficiently long and $V_{DS} > 4V_t$, the channel length modulation effects are negligible and $\exp\left(-\frac{V_{DS}}{V_t}\right) \approx 0$. As illustrated in Refs. [9, 10], the weak inversion currents of M3 and M4 versus the gate-source voltage are

$$I_{D3} = \mu S_3 C_D V_t^2 \exp\frac{A(V_{GS3} - V_{TH})}{V_t} \tag{1}$$

and

$$I_{D4} = \mu S_4 C_D V_t^2 \exp\frac{A(V_{GS4} - V_{TH})}{V_t} \tag{2}$$

where

$$\frac{I_{D3}}{I_{D4}} = \frac{I_{D1}}{I_{D2}} = \frac{S_1}{S_2}. \tag{3}$$

Solving Eqs. (1), (2), and (3) for the difference in

gate-source voltage between M3 and M4 $\Delta V_{GS34}(T)$ gives

$$\Delta V_{GS34}(T) = V_{GS3}(T) - V_{GS4}(T) = \Delta V_{GS34}(T_0)\frac{T}{T_0} \tag{4}$$

where $\Delta V_{GS34}(T_0) = \dfrac{kT_0}{Aq}\ln\dfrac{S_1 S_4}{S_2 S_3}$. (5)

For a typical value of $\Delta V_{GS34}(T_0)$, $\Delta V_{GS34}$ linearly increases with the temperature and is a PTAT voltage.

The difference in gate-source voltage between M3 and M4, which is a PTAT voltage as described above, flows through $R_1$ and generates a PTAT current.

$$I_{D2} = \frac{\Delta V_{GS34}(T_0)}{R_1} \times \frac{T}{T_0} \tag{6}$$

### 2.3 CTAT current generator

Transistors M5 ~ M8 and resistor $R_2$ form a CTAT current generator. M6 operates in the weak inversion region. M5 is used to copy current from M2 and provides a fixed current to M6. Two equivalent representations for the drain current of M6 are described in Ref.[8], as

$$I_{D6} = \mu S_6 C_D V_t^2 \exp\frac{A(V_{GS6} - V_{TH})}{V_t} \tag{7}$$

and $I_{D6} = \mu S_6 C_D V_t^2 \exp\dfrac{\phi_S - 2\phi_F}{V_t}$. (8)

Comparing Eq.(7) and Eq.(8) results in

$$A(V_{GS6} - V_{TH}) = \phi_S - 2\phi_F \tag{9}$$

When the operating temperature is $T_0$, Equation (9) changes to

$$\phi_S(T_0) - 2\phi_F(T_0) = A(T_0)[V_{GS6}(T_0) - V_{TH}(T_0)] \tag{10}$$

The expression $\phi_S - 2\phi_F$ with respect to temperature $T$ can be found in Ref.[7]:

$$\phi_S(T) - 2\phi_F(T) = [\phi_S(T_0) - 2\phi_F(T_0)]\frac{T}{T_0} \tag{11}$$

Hence, combining Eqs.(9), (10), and (11) yields

$$A(T)[V_{GS6}(T) - V_{TH}(T)] = A(T_0)[V_{GS6}(T_0) - V_{TH}(T_0)]\frac{T}{T_0} \tag{12}$$

The threshold voltage is a linear function of temperature as modeled in Ref.[11]:

$$V_{TH} = V_{TH}(T_0) + K_T\left(\frac{T}{T_0} - 1\right) \tag{13}$$

where $K_T$ is the temperature coefficient of the threshold voltage and $K_T < 0$. Assuming that $A(T)$ has small variations with temperature, that is, $A(T) \approx A(T_0)$, we get

$$V_{GS6}(T) = V_{GS6}(T_0) + [V_{GS6}(T_0) - V_{TH}(T_0) + K_T]\left(\frac{T}{T_0} - 1\right) \tag{14}$$

Thus, $V_{GS6}(T_0) - V_{TH}(T_0)$ and $K_T$ are negative quantities, so

$$V_{GS6}(T_0) - V_{TH}(T_0) + K_T < 0 \tag{15}$$

That is, a voltage $V_{GS6}$ that decreases with temperature linearly for any fixed drain current $I_D$. $V_{GS6}$ in the weak inversion region is a CTAT voltage.

So the current through $R_2$ is a CTAT current.

$$I_{D7} = \frac{V_{GS6}(T)}{R_2} \tag{16}$$

### 2.4 Voltage reference generator

The voltage reference generator is made up of transistors M9, M10 and resistor $R_3$, which is used to generate a low-temperature-drift reference voltage. M9 and M10 are used to copy currents from CTAT and PTAT current generators in order to obtain two currents with different temperature coefficients. The currents through M9 and M10, $I_C$ and $I_P$, are given by the following equations.

$$I_C = \frac{V_{GS6}(T)}{R_2} \times \frac{S_9}{S_7} \tag{17}$$

and $I_P = \dfrac{S_{10}}{S_2} \times \dfrac{\Delta V_{GS34}(T)}{R_1}$. (18)

These two temperature dependent currents $I_C$ and $I_P$ are summed together into resistor $R_3$, thus the low-temperature-drift reference voltage $V_{ref}$ is generated.

$$V_{ref} = (I_C + I_P)R_3 = \left[\frac{V_{GS6}(T)}{R_2} \times \frac{S_9}{S_7} + \frac{S_{10}}{S_2} \times \frac{\Delta V_{GS34}(T)}{R_1}\right]R_3 \tag{19}$$

The temperature coefficient of resistors is cancelled if the resistors are formed with the same resistive layer. As shown in Eq.(19), the temperature dependence of the proposed voltage reference is governed by two linear terms. It can be obtained by differentiating Eq.(19) with respect to temperature and is given by

$$\frac{\partial V_{ref}}{\partial T} = \frac{S_9}{R_2 S_7} \times \frac{\partial V_{GS6}(T)}{\partial T} + \frac{S_{10}}{S_2 R_1} \times \frac{\partial \Delta V_{GS34}(T)}{\partial T} = \frac{S_9}{R_2 S_7} \times \frac{V_{GS6}(T_0) - V_{TH}(T_0) + K_T}{T_0} + \frac{S_{10}}{S_2 R_1} \times \frac{\Delta V_{GS34}(T_0)}{T_0} \tag{20}$$

To demonstrate that the voltage reference is insensitive to temperature, we make $\dfrac{\partial V_{ref}}{\partial T} = 0$ and obtain the following equation:

$$\frac{S_9 S_2 R_1}{S_7 S_{10} R_2} = -\frac{\Delta V_{GS34}(T_0)}{V_{GS6}(T_0) - V_{TH}(T_0) + K_T} \tag{21}$$

Equation (21) shows that the temperature coefficient can be optimized by circuit parameters. Freedom on optimization can be done on the circuit design level and on-chip trimming.

As shown in Fig. 1, the resistor $R_3$ can be divided

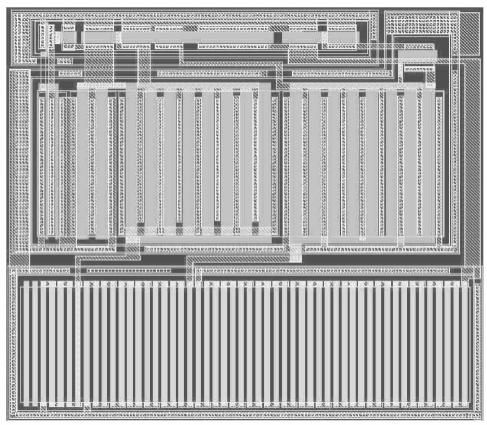

Fig. 2 Layout of the proposed circuit

into many parts, as $r_1, r_2, \cdots, r_n$, to get more than one reference voltage output, such as $V_{\mathrm{ref}}(1), V_{\mathrm{ref}}(2), \cdots, V_{\mathrm{ref}}(n)$. This structure is quite suitable for the systems requiring many different reference voltages simultaneously. According to the summing current and required reference voltages, the value of each resistor can be calculated. For example, if the system requires two reference voltages, two proper resistors are connected in series as resistor $R_3$. The high voltage nodes of both the resistors are reference outputs. As mentioned above, the temperature coefficient of resistors is cancelled in this circuit structure, so each reference voltage output has a low temperature coefficient. Another characteristic of the proposed voltage reference is that the power dissipation of the whole circuit can be easily controlled by increasing or decreasing the PTAT and CTAT currents proportionally.

## 3 Experimental results

The proposed voltage reference shown in Fig. 1 has been successfully designed and implemented in standard 0.6$\mu$m DPDM n-well CMOS technology and the main process parameters are $V_{\mathrm{THN}} = 0.728\mathrm{V}$ and $V_{\mathrm{THP}} = -1.02\mathrm{V}$. The circuit is designed to provide three reference voltage outputs (200mV, 1V, and 2V) for a white LED backlight driver chip, so resistor $R_3$ is made up of three parts $r_1$, $r_2$, and $r_3$. The sizes of the MOSFETs and resistors chosen are tabulated in Table 1. The proposed voltage reference has been simulated and the results show that the output voltages are about 199.6mV, 0.998V, and 1.997V at room temperature when the supply voltage is 4V. The temperature coefficient is about 10.5ppm/℃ and the voltages change about 0.21, 1.05, and 2.1mV when the temperature increases from 0 to 100℃.

Since the circuit is for a white LED backlight driver, the layout of the voltage reference is designed with other parts. In this paper, only the layout of the

Table 1 Sizes of the proposed circuit components

| MOSFET | $(W/L)/(\mu\mathrm{m}/\mu\mathrm{m})$ | MOSFET | $(W/L)/(\mu\mathrm{m}/\mu\mathrm{m})$ |
|---|---|---|---|
| P1 | 8/1 | M5 | 10/4 |
| P2 | 4/4 | M6 | 400/4 |
| N1 | 1/100 | M7 | 10/4 |
| M1 | 10/4 | M8 | 10/4 |
| M2 | 10/4 | M9 | 8/4 |
| M3 | 100/4 | M10 | 25/4 |
| M4 | 400/4 | | |

| Resistor | Value/kΩ | Resistor | | Value /kΩ |
|---|---|---|---|---|
| $R_1$ | 100 | $R_3$ | $r_1$ | 65 |
| $R_2$ | 260 | | $r_2$ | 255 |
| | | | $r_3$ | 335 |

reference circuit is shown in Fig. 2. A high-resistive poly resistor (about 1kΩ/□) is used to reduce the chip area. The occupied circuit area is about 0.023mm$^2$, which is much smaller than the bandgap reference.

The chip is encapsulated with a dual in-line package (DIP) type. There are five bonding pads for the test, which are $V_{\mathrm{dd}}$, Gnd, $V_{\mathrm{ref}}(1)$, $V_{\mathrm{ref}}(2)$, and $V_{\mathrm{ref}}(3)$. $V_{\mathrm{dd}}$ and Gnd are input pins, and the other three are output pins. Four items are tested: supply current, temperature coefficient, line regulation, and power supply rejection ratio. Throughout the test, three external operational Amplifiers are used to follow the three output voltages respectively for the lack of load capacity. Each amplifier is designed as a voltage follower. Thus, the output of the amplifiers is tested in order to avoid the distortion of the output load.

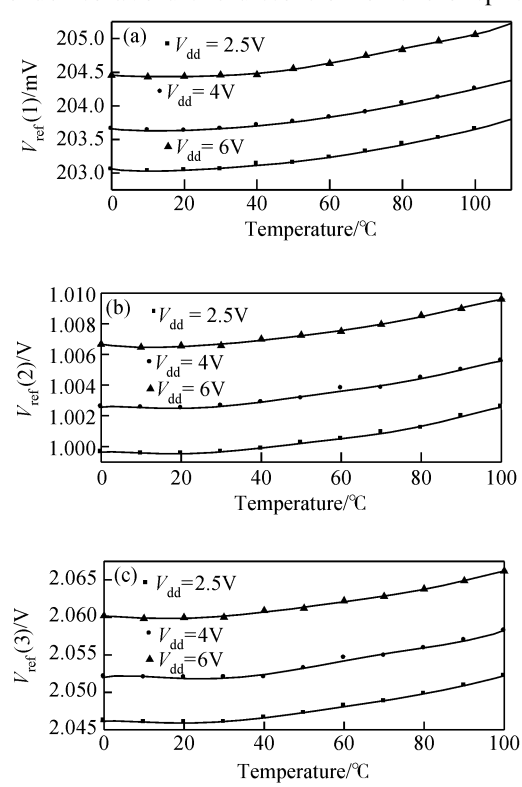


Fig. 3 Measured results of (a) $V_{\mathrm{ref}}(1)$, (b) $V_{\mathrm{ref}}(2)$, (c) $V_{\mathrm{ref}}(3)$ on temperature effect with different supply voltages

Table 2　Comparison with published voltage reference circuits with a standard CMOS process

| | This work | Leung *et al*.[4] | Leung *et al*.[6] | Wang *et al*.[12] | Qin *et al*.[13] |
|---|---|---|---|---|---|
| Technology | 0.6$\mu$m CMOS | 0.6$\mu$m CMOS | 0.6$\mu$m CMOS | 0.18$\mu$m CMOS | 0.35$\mu$m CMOS |
| Threshold voltages | $V_{THN}$ = 0.728V, $V_{THP}$ = −1.02V | $V_{THN}$ = 0.9V, $V_{THP}$ = −0.9V | $V_{THN}$ = 0.9V, $V_{THP}$ = −0.9V | —— | —— |
| Supply voltage $V_{dd}$/V | 2.5 to 6 | 1.4 to 3 | 0.98 to 1.5 | 0.6 to 1.5 | 1 to 1.4 |
| Supply current (max)/$\mu$A | 8.25 | 9.7 | 18 | 4.8 | 160 |
| Reference voltage/V | 0.203,1 and 2.05 | 0.3091 | 0.603 | 0.399 | 0.352 |
| Temperature coefficient /(ppm/℃) | 31 | 36.9 | 15 | 80 | 16.7 |
| Line regulation/(%/V) | 0.203 | 0.08 | 0.73 | 0.5 | 0.1 |
| Chip area /mm$^2$ | 0.023 | 0.055 | 0.24 | 0.045 | 0.18 |

When testing the supply current of this chip, a galvanometer was connected the supply voltage and $V_{dd}$ pin. A different current result is obtained directly from the galvanometer when the test conditions, such as temperature and supply voltage, are changed. An oven is used to provide different temperatures during the temperature coefficient test. The encapsulated chip is put in the oven and the output pins are measured with a voltmeter to get the output voltages under different fixed temperatures. With these test data from the voltmeter, a temperature coefficient curve is obtained with data processing software. The supply voltage can also be changed to produce different output curves with temperature. After testing the output voltage with different supply voltages, the line regulation is easily calculated to be $\frac{\Delta V_{ref}}{\Delta V_{dd} V_{ref}} \times 100\%$. A waveform generator is needed in the power supply rejection ratio test. A sine wave with a DC voltage such as 3V and an amplitude voltage such as 0.1V in a certain frequency is used as the supply voltage. The output node is measured with an oscillograph and the peak-to-peak value is measured. The power supply rejection ratio is $20\log_{10} \frac{\Delta V_{ref\_pp}}{\Delta V_{dd\_pp}}$, where $\Delta V_{ref\_pp}$ is the peak-to-peak value of $V_{ref}$ and $\Delta V_{dd\_pp}$ is the peak-to-peak value of $V_{dd}$.

The chip was tested adopting the method described above. The measurement results show that the three typical mean reference voltages are about 203mV, 1.0V, and 2.05V at room temperature when the supply voltage is 4V. The maximum supply current is 8.25$\mu$A, which occurs at the maximum supply voltage (6V) and the maximum operational temperature (100℃). Lower supply current can be achieved through decreasing the PTAT and CTAT currents proportionally, that is, decreasing the $W/L$ ratios of M9 and M10.

Figure 3 shows the test result of a sample with a temperature coefficient of about 31ppm/℃ at 2.5, 4, and 6V supply voltages over the whole measurement range. When the operation temperature changes from 0 to 20℃, these three reference voltage outputs show themselves as CTAT voltages, while the outputs increase as PTAT voltages when the temperature increases from 20 to 100℃. As shown in Fig. 3, over the whole operating temperature range, the three voltage outputs, $V_{ref}(1)$, $V_{ref}(2)$, and $V_{ref}(3)$ change about 0.62, 3.09, and 6.32mV, respectively. The average line regulation is ±0.203%/V. At the supply voltage of 2.5V, the measured power supply rejection ratio of $V_{ref}(2)$ at 100kHz is −26dB. A filtering capacitor to the output is necessary to improve the power supply rejection ratio of the high-frequency region. The test results are similar to, but not as good as, the simulation results. The reason for the difference is the ideality of the simulation model and inevitable parasitics of the transistors.

A comparison with published voltage reference circuits fabricated with a standard CMOS process is shown in Table 2. All of the results listed in the table are chip test results. The structure in this work has a good performance with respect to temperature coefficient and line regulation. Since no BJTs are used in this work, it has the smallest chip area. The supply voltage range is also the largest. Furthermore, only the proposed voltage reference provides more than one reference voltage output, which is the main advantage of this structure. It is quite suitable for systems requiring many different reference voltages synchronously.

Since the designed voltage reference is for a white LED backlight driver chip whose supply voltage range is about 2.5～6V, the voltage reference structure cannot operate at a very low supply voltage such as 1V. This will be solved in a future study.

## 4　Conclusion

A CMOS voltage reference based on $V_{GS}$ and

$\Delta V_{GS}$ in the weak inversion region is described in this paper. Unlike conventional voltage reference designs, the proposed structure which has no BJTs, overcomes the problem of a fixed reference voltage. It also provides a convenient method for obtaining many reference outputs synchronously.

A test chip has been fabricated using a standard 0.6$\mu$m CMOS process and experimental results are presented to verify the theoretical analysis. The small chip area, low-temperature coefficient, and low power dissipation are well suited for on-chip voltage reference generation in both analog and digital systems. The proposed circuit is reproducible in any CMOS technology. It has been successfully applied in a white LED backlight driver chip.

## References


[1] Pease R A. The design of bandgap reference circuits: trials and tribulations. IEEE Bipolar Circuits and Technology Meeting, 1990:214

[2] Strik S. Bandgap voltage reference: errors and techniques for their minimization. International Baltic Electronics Conference, 2006:1

[3] Mao Jingwen, Chen Tingqian, Chen Cheng, et al. CMOS 1.5V bandgap voltage reference. 6th International Conference on ASIC, 2005:469

[4] Leung K N, Mok P K T. A CMOS voltage reference based on weighted $\Delta V_{GS}$ for CMOS low-dropout linear regulators. IEEE J Solid-State Circuits, 2003, 38:146

[5] Harrison W T, Connelly J A, Stair R. An improved current-mode CMOS voltage reference. Proc Southwest Symposium, SSMSD, 2001, 1:24

[6] Leung K N, Mok P K. A sub-1-V 15-ppm/℃ CMOS bandgap voltage reference without requiring low threshold device. IEEE J Solid-State Circuits, 2002, 37:526

[7] Malcovati P, Maloberti F, Fiocchi C, et al. Curvature-Compensated BICMOS bandgap with 1-V supply voltage. IEEE J Solid-State Circuits, 2001, 36:1076

[8] Giustolisi G, Palumbo G, Criscione M, et al. A low-voltage low-power voltage reference based on subthreshold MOSFETs. IEEE J Solid-State Circuits, 2003, 38:151

[9] Vittoz E, Fellrath J. CMOS analog integrated circuits based on weak inversion operation. IEEE J Solid-State Circuits, 1977, 12: 224

[10] Grotjohn T, Hoefflinger B. A parametric short-channel MOS transistor model for subthreshold and strong inversion current. IEEE Trans Electron Devices, 1984, 31(2):234.

[11] Liu W. MOSFET models for spice simulation. New York: John Wiley & Sons, Inc, 2001

[12] Wang Han, Ye Qing. Design and stability analysis of a 0.6V supply CMOS voltage reference. Chinese Journal of Semiconductors, 2006, 27:1508 (in Chinese)[王晗, 叶青. 0.6V 电源电压的 CMOS 基准源设计及稳定性分析. 半导体学报, 2006, 27(8):1508]

[13] Qin Bo, Jia Chen, Chen Zhiliang, et al. A 1V MNC bandgap reference with high temperature stability. Chinese Journal of Semiconductors, 2006, 27(11):2035 (in Chinese)[秦波, 贾晨, 陈志良, 等. 1V 电源非线性补偿的高温度稳定性电压带隙基准源. 半导体学报, 2006, 27(11):2035]


# 一种基于亚阈区 $V_{GS}$ 和 $\Delta V_{GS}$ 的 CMOS 基准电压源电路


夏晓娟† 谢 亮 孙伟锋

(东南大学国家专用集成电路系统工程技术研究中心, 南京 210096)



**摘要**: 介绍了一种基于亚阈区 $V_{GS}$ 和 $\Delta V_{GS}$ 的 CMOS 基准电压源电路, 电路不采用二极管和三极管. 电路采用正负温度系数电流叠加的原理, 可以产生多个基准电压值的输出, 适用于同时需要多个基准的电路系统中. 所设计的电路在 0.6$\mu$m CMOS 工艺线上流水验证, 芯片面积为 0.023mm$^2$. 测试结果表明, 电源电压为 2.5～6V 时, 最大的电流为 8.25$\mu$A; 电源电压为 4V 时, 常温下所获得的三个基准电压值为 203mV, 1.0V 及 2.05V. 温度由 0℃ 变化到 100℃ 时, 芯片的温度系数为 31ppm/℃, 平均的线性度为 ±0.203%/V. 此电路结构已经成功应用于背光 LED 驱动电路中.



**关键词**: CMOS 基准电压源; CTAT 电流; PTAT 电流; 温度系数; 亚阈值区

**EEACC**: 1265B; 2570D

**中图分类号**: TN791 **文献标识码**: A **文章编号**: 0253-4177(2008)08-1523-06



† 通信作者. Email: xiaxj@seu.edu.cn



2007-10-15 收到, 2008-04-08 定稿