Effect of High-Gate-Voltage Stress on the Reverse Gated-Diode Current in LDD nMOSFET's*

Chen Haifeng†, Hao Yue, and Ma Xiaohua

(*School of Microelectronics, Xidian University, Xi'an 710071, China*)

Abstract: The reverse generation current under high-gate-voltage stress condition in LDD nMOSFET's is studied. We find that the generation current peak decreases as the stress time increases. We ascribe this finding to the dominating oxide trapped electrons that reduce the effective drain bias, lowering the maximal generation rate. The density of the effective trapped electrons affecting the effective drain bias is calculated with our model.

Key words: generation current; high gate voltage stress; trapped electron
EEACC: 2530; 2560R
CLC number: TN386.1 **Document code**: A **Article ID**: 0253-4177(2008)05-0875-04

1 Introduction

The gated-diode (GD) current I_{GD} or gate-induced drain leakage (GIDL) current I_{GIDL} under a very low field is composed of the generation-recombination current[1]. Since the interface states act as the generation-recombination centers and increase the additional generation-recombination current, the variation of this current reveals the condition of the interface states. Therefore, the GD technique or very low field GIDL measurement is used widely to detect the interface states. Compared with the charge pumping method, the GD technique is a direct-current measurement and simple[2].

In Refs. [3,4], the generation current under the reverse GD mode is applied to investigate the oxide damage in nMOSFET's. However, they mainly studied the damage under the middle gate voltage ($V_G = V_D/2$) stress. In this case, the interface states dominate the damage. Commonly, the density of interface states N_{it} is the focus in using the GD technique, while the role of oxide charges is ignored. Yih *et al*. studied high-gate-voltage ($V_G = V_D$) stress-induced damage in nMOSFETs using the forward GD mode technique[5]. They used injected holes neutralizing the trapped electrons to separate N_{it} and the density of oxide charges N_{ox}. However, they use the recombination current in their work.

In this paper, we present results obtained from the generation current I_D measurements under the high-gate-voltage (HGV) stress condition, showing the effect of oxide trapped electrons. A correlation is reported between the generation current peak $I_{D,peak}$ and the corresponding density of trapped charges.

2 Experimental devices and theory

We used two LDD nMOSFETs with the same geometry in this study. The oxide thickness is 4nm. The gate has a length of $L = 0.35\mu$m and a width of $W = 3\mu$m. In order to reduce the leakage of the drain pn junction, a small voltage of 0.1V is applied to the drain. Thus, the reverse current comes mainly from the interface states. For measurements, the substrate is grounded ($V_B = 0$V) and the source is floating. The gate voltage V_G is swept from -0.6V to 0.8V.

At the depletion region surrounding the drain pn junction, Shockley-Read-Hall (SRH) statistics point to the midgap traps as the maximum effective generation centers under the small reverse bias ($V_D < 0.3$V). The generation current comes from the midgap traps in the narrow zone Δx between the electron quasi-Fermi level φ_e and hole quasi-Fermi level φ_h. As the gate is swept from the inversion threshold through depletion into the strong accumulation, the effective generation zone moves like a pointer of decreasing width along the interface towards the drain[6]. This zone separates from the interface completely when the gate voltage approaches a small positive value. In Ref. [4], the value is 0.5V at $V_D = 0.1$V. After that, the generation current drops sharply.

The recombination rate U is given by Ref. [7]:

$$U = \frac{N_{it}\sigma_p\sigma_n v_{th}(np - n_i^2)}{\sigma_n\left(n + p + 2n_i\exp\left(\frac{E_t - E_i}{kT}\right)\right) + \sigma_p\left(n + p + 2n_i\exp\left(\frac{E_i - E_t}{kT}\right)\right)} \quad (1)$$

* Project supported by the National Natural Science Foundation of China (No. 60376024)
† Corresponding author. Email: heellor@163.com
Received 31 October 2007, revised manuscript received 5 December 2007

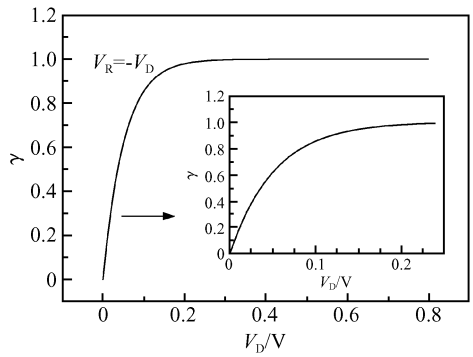

Fig. 1 γ as a function of drain bias V_D

where v_{th} is the carrier thermal velocity, σ_p and σ_n are the hole and electron capture cross section, respectively, and E_t is the trap energy level. Other parameters have their common meanings. When the pn junction is the reverse biased $V_R<0$ ($V_R=-V_D$, $V_D>0$V), $np=n_i^2\exp(qV_R/kT)\ll n_i^2$. U is negative and delegates the generation rate G. Assuming $E_t=E_i$, $\sigma_p=\sigma_n=\sigma$, G approaches its maximum G_{max} when $n=p=n_i\exp(qV_R/2kT)$. Thus, Equation (1) becomes:

$$G_{max}=\frac{1}{2}N_{it}\sigma v_{th}n_i[1-\exp(qV_R/2kT)]=\frac{1}{2}N_{it}\sigma v_{th}n_i\gamma \quad (2)$$

$$\gamma=1-\exp(qV_R/2kT)=1-\exp(-qV_D/2kT) \quad (3)$$

where γ is defined as the maximum G factor.

Figure 1 describes the relationship between γ and V_D. When $V_D>0.2$V, γ approaches 1. When $V_D<0.2$V, γ decreases quickly as V_D increases.

The maximal generation current is then:

$$I_{D,peak}=qW\Delta xG_{max}=\frac{1}{2}qW\Delta xn_iN_{it}\sigma v_{th}\gamma \quad (4)$$

Thus, the generation current depends on the generation zone Δx, interface state N_{it}, and γ. After stress, the additional N_{it} and the oxide trapped charges Q_{ox} are created. The additional N_{it} enhances the generation current. The Q_{ox} locating in the oxide decreases or increases the effective gate voltage, shifting the location of Δx. However, it cannot change the value of Δx as $I_{D,peak}$ appears. Meanwhile, if the Q_{ox} locates in the oxide above the drain region or overlap region, these trapped charges could change the effective V_D, thus changing γ. We define the effective trapped charge $Q_{ox,eff}$, which denotes the effective influence of the trapped charge Q_{ox} on V_D. For a certain gate voltage on the reverse GD mode, the effective V_D decreases when the trapped charge is electron ($Q_{ox,eff}<0$), and the effective V_D increases when the trapped charge is hole ($Q_{ox,eff}>0$). Then, the effective γ is:

$$\gamma_{eff}=1-\exp\left[q\left(-V_D-\frac{Q_{ox,eff}}{C_{ox}}\right)/2kT\right] \quad (5)$$

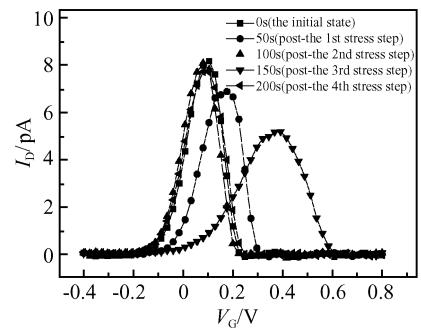

Fig. 2 Generation current I_D as a function of V_G during alternating stress conditions The hot electron injection stress at $V_D=V_G=3.5$V and the hot hole injection at $V_D=3.0$V and $V_G=-3.0$V. The first stress step is the electron injection, followed by a hole injection, an electron injection, and again a hole injection condition. Each stress step continues for 50s. The total stress time is 200s.

Considering N_{it} and the influences of oxide charges on Δx, γ, Equation (4) is deduced to:

$$I_{D,peak}(post)=\frac{1}{2}q\times W\times\Delta x\left(V_G+\frac{Q_{ox}}{C_{ox}}\right)\times n_i\times(N_{it}+\Delta N_{it})\times\sigma\times v_{th}\times\gamma_{eff} \quad (6)$$

3 Results and discussion

Figure 2 shows that $I_{D,peak}$ decreases as the gate voltage shifts positive in the first step. This results from the trapped electron, as has been mentioned above. According to Eq. (6), the oxide trapped electrons decrease the effective gate voltage, so V_G shifts to a more positive value when $I_{D,peak}$ appears. Meanwhile, because $V_D=V_G$ stress will introduce trapped electrons in the oxide above the drain-gate overlap region in LDD nMOSFETs[8]. So, the oxide trapped electrons decrease γ_{eff} and lower $I_{D,peak}$. After the second stress step, the off state stress ($V_D=3.0$V and $V_G=-3.0$V) injects the holes into the oxide at this overlap region. After a few seconds, the holes neutralize the trapped electrons completely, which shifts V_G left to its initial value, shifts γ_{eff} back to its initial value, and $I_{D,peak}$ rises to its initial position. Thus, the curve almost returns to its initial state. This result proves that few interface states are created during the HGV stress in the first step. If there are many interface states in the oxide, after the holes have neutralized the trapped electrons completely in Fig. 2 (the curve recovers completely), $I_{D,peak}$ should be enhanced according to Eq. (4). However, after the second stress step there is no increase, which implies that very few interface states are created in the first stress step. In others words, the role of interface states can be ignored. After the third step, the curve appears like after the first stress step, with $I_{D,peak}$ shifting rightwards

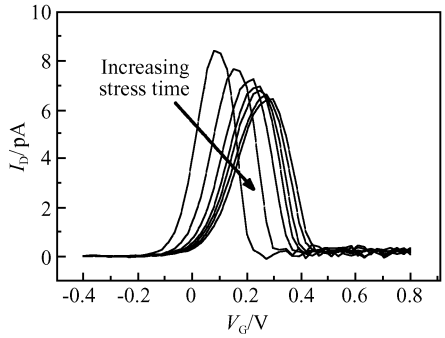

Fig. 3　Generation current I_D (measured with $V_D = 0.1$V) as a function of gate voltage before and after stress at $V_D = V_G = 3.5$V　The stress time is varied from 0 to 300s (i.e. 0, 50, 100, 150, 200, 250, 300s).

and downwards.

However, the shifts become stronger, as can be seen in Fig. 2. According to $\Delta N_{ox} = \frac{\Delta V_g C_{ox}}{q}$ [9], where $C_{ox} = 9.6 \times 10^{-7}$ F/cm^2 measured, the density of the trapped electron is 4.38×10^{11} cm^{-2} for the first step and 1.73×10^{12} cm^{-2} for the third step. Although the same stress conditions are applied to the device during the first and third step, the density of ΔN_{ox} created during the third step is much greater than during the first step. Since hole injection can create the neutral electron traps in the oxide[10], a lot of neutral electron traps are created by the hole injection during the second step. The hot electrons of the third step fill not only the neutralized electron traps created in the first step, but also the neutral electron traps created during the second step. In this way, the density of trapped electrons after the third stress step is much larger than after the first. So the larger density of trapped electrons reduces γ_{eff} more than in the first step. Consequently, $I_{D,peak}$ decreases and shifts to positive gate voltage much more than the initial $I_{D,peak}$. We can roughly calculate the density of the neutral electron traps created during the second step, which equals the difference of the densities of the trapped electrons during the first and second stress step and is 1.35×10^{12} cm^{-2}.

During the fourth stress step, holes are injected to neutralize the trapped electrons again. Because the trapped electrons in the oxide lower the barrier that the hole must surmount, the 50s holes injection during the fourth step still neutralize the trapped electron almost completely despite more trapped electrons in the oxide than after the first stress step. After the fourth step, the current curve almost recovers its initial state, as can be seen in Fig. 2. Like the discussion on ΔN_{it} after the second step, the result after the fourth step further proves that the trapped electrons make the dominating effect on the generation current and

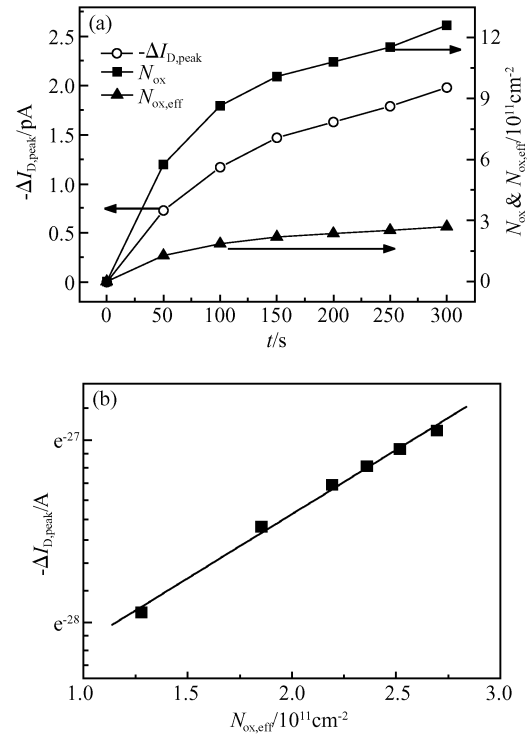

Fig. 4　(a) $N_{ox,eff}$, N_{ox}, $-\Delta I_{dpeak}$ versus the stress time; (b) Relationship of $-\Delta I_{dpeak}$ with $N_{ox,eff}$ in half-ln

the role of interface states can be ignored after the HGV stress.

Based on the results and analysis, we further investigate the influence of oxide trapped electrons on the generation current. Figure 3 shows the changes of the generation current before and after the HGV stress. After stress, the peak current is shifted to positive gate voltage and is lowered, indicating that the electrons are trapped in the oxide. According to Eq. (5), the trapped electrons reduce γ_{eff}, and thus increase the generation current peak $I_{D,peak}$. Because there are few interface states and they can be ignored above, according to Eqs. (4)～(6):

$$\frac{I_D(\text{post})}{I_D(\text{pre})} = \frac{\gamma_{eff}}{\gamma} = \frac{1 - \exp\left[q\left(-V_D - \frac{Q_{ox,eff}}{C_{ox}}\right)/2kT\right]}{1 - \exp(-qV_D/2kT)} \tag{7}$$

$Q_{ox,eff}$ can be obtained ($N_{ox,eff}$ is the density of $Q_{ox,eff}$):

$$Q_{ox,eff} = -qN_{ox,eff} = C_{ox}\left\{-V_D - \frac{2kT}{q} \times \ln\left[1 - \frac{I_D(\text{post})}{I_D(\text{pre})}\left(1 - \exp\left(\frac{-qV_D}{2kT}\right)\right)\right]\right\} \tag{8}$$

$$N_{ox,eff} = \frac{C_{ox}}{q}\left\{V_D + \frac{2kT}{q} \times \ln\left[1 - \frac{I_D(\text{post})}{I_D(\text{pre})}\left(1 - \exp\frac{-qV_D}{2kT}\right)\right]\right\} \tag{9}$$

$N_{ox,eff}$ can be calculated by Eq. (9). Figure 4 (a) shows the changes of $N_{ox,eff}$, $-\Delta I_{D,peak}$, and N_{ox} with

stress time, which is extracted from Fig. 3. They have the same trend of change. The rate of enhancement is fast at the start and becomes slower later.

Equation (9) is deduced on the basis of Eq. (6), so we should clarify the validity of Eq. (6) in order to confirm Eq. (9). According Eq. (6):

$$-\Delta I_{\mathrm{D,peak}} = I_{\mathrm{D}}(\mathrm{pre}) - I_{\mathrm{D}}(\mathrm{post}) \propto \gamma - \gamma_{\mathrm{eff}}$$
$$= \exp\left[q\left(-V_{\mathrm{D}} - \frac{Q_{\mathrm{ox,eff}}}{C_{\mathrm{ox}}}\right)/2kT\right] - \exp(-qV_{\mathrm{D}}/2kT) \propto$$
$$\exp\left(-\frac{qQ_{\mathrm{ox,eff}}}{C_{\mathrm{ox}}}\right) \propto \exp(N_{\mathrm{ox,eff}}) \qquad (10)$$

Given Eq. (6), $-\Delta I_{\mathrm{D,peak}}$ will vary exponentially with $N_{\mathrm{ox,eff}}$. Figure 4(b) shows $-\Delta I_{\mathrm{D,peak}}$ is linear with $N_{\mathrm{ox,eff}}$ in the half-natural logarithm coordinate, which extracted from Fig. 4. (a). This result clarifies the validity of Eq. (6). Furthermore, it supports the validity of calculating $N_{\mathrm{ox,eff}}$ with Eq. (9).

4 Conclusion

The effect of the HGV stress on the generation current in LDD nMOSFET's has been studied. The trapped electrons reduce the effective factor influencing the maximal generation rate and decrease the current. We using our model to calculate the density of effective trapped electrons created in the HGV stress. Although this mode only suits the case when interface states can be ignored, it should still be helpful to understand the features of detecting the damage in the oxide using the reverse GD method.

References

[1] Okhonin S, Hessier T, Dutoit M. Spatial distribution of interface traps after hot-carrier stress from forward GIDL measurements. Microelectron Eng, 1995, 28: 261

[2] Cheng S M, Yih C M, Yeh J C, et al. A unified approach to profiling the lateral distributions of both oxide charge and interface states in n-MOSFET's under various bias stress conditions. IEEE Trans Electron Devices, 1997, 44(11): 1908

[3] Giebel T, Goser K. Hot-carrier degradation of n-channel MOSFET's characteristized by a gated-diode measurement technique. IEEE Electron Device Lett, 1989, 10(2): 76

[4] Speckbacher P, Asenov A, Bollu M, et al. Hot-carrier-induced deep-level defectes from gated-diode measurements on MOSFET's. IEEE Electron Device Lett, 1990, 11(2): 95

[5] Yih C M, Cheng S M, Chung S S. A new approach to simu n-MOSFET gate current degradation by including hot-electron induced oxide damage. IEEE Trans Electron Devices, 1998, 45(11): 2343

[6] Speckbacher P, Berger J, Asenov A, et al. The 'gated-diode' configuration in MOSFET's, a sensitive tool for characterizing hot carrier degradation. IEEE Trans Electron Devices, 1995, 42(7): 1287

[7] Grove A S. Physics and technology of semiconductor devices. New York: Wiley, 1967

[8] Chen H F, Hao Y, Ma X H, et al. Comparison of hot-hole injections in ultrathin oxide under an alternating stress. Chinese Physics, 2007, 16(10): 3114

[9] Minson E, Sanchez I, Barnaby H J, et al. Assessment of gated sweep technique for total dose and dose rate analysis in bipolar oxides. IEEE Trans Nucl Sci, 2004, 51(6): 3723

[10] Doyle B S, Bourcerie M, Bergonzoni C, et al. The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n-MOS transistors. IEEE Trans Electron Devices, 1990, 37(8): 1869

高栅压电子注入损伤对产生电流的影响*

陈海峰† 郝 跃 马晓华

(西安电子科技大学微电子学院, 西安 710071)

摘要: 用反向 GD 法研究了高栅压应力下的 LDD nMOSFET 中的损伤情况. 发现这种应力下产生电流峰值随着应力时间的增大变小, 峰值变小和氧化层中负陷阱电荷增大的趋势一致. 峰值变小是由于应力中氧化层陷阱电子起主导作用, 从而减小了漏电压的有效作用, 使得产生率最大值变小. 应用这种新模型定量得出了影响漏电压的等效电荷密度.

关键词: 产生电流; 高栅压应力; 陷落电子

EEACC: 2530; 2560R

中图分类号: TN386.1 **文献标识码**: A **文章编号**: 0253-4177(2008)05-0875-04

* 国家自然科学基金资助项目(批准号: 60376024)

† 通信作者. Email: heellor@163.com

2007-10-31 收到, 2007-12-05 定稿