Implementation of a DC-10Mb/s 0.5μm CMOS Laser Diode Driver

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Abstract: A DC-10Mb/s laser diode driver, compatible with TTL and CMOS levels, is presented. The optical power corresponding to '1' and '0' can be set independently with resistors off-chip and stabilized with a closed loop. A novel peak-to-peak optical power monitor and stabilization mechanism is introduced. The circuit, fabricated in a CSMC 0.5μm mixed signal CMOS process, can provide 120mA maximum drive current and 0.6dB extinction ration fluctuation over $-20\sim+80$℃, which is independent of input pattern.

Key words: laser diode driver; CMOS; extinction ratio; temperature compensation
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1 Introduction

Laser diode drivers (LDD) are one of the most critical components in optic fiber transmission systems[1] and can convert input level to drive current. Traditional LDDs consist of three parts: modulator, automatic power control (APC), and automatic temperature compensation (ATC). These can meet the needs of traditional optical communication system perfectly. Optical line coding is necessary for this kind of LDD. But for ultra-low speed communications, the pre-processing of input data is difficult. For example, low speed burst mode RS232 or RS485 data must be converted to higher speed continuous line coding before being sent to the LDD.

This paper will demonstrate a DC to 10Mb/s LDD that has certain advantages over conventional LDDs for ultra-low speed optical communication. It can provide high temperature stability without ATC, APC, and line coding.

2 Circuit description

2.1 Circuit structure

The circuit structure of a traditional LDD is shown in Fig. 1. The modulator is a multi-stage amplifier to generate LD drive current. APC ensures that the system keeps stable average power over temperature and LD aging by adjusting bias current ($I_{\rm bias}$). ATC guarantees enough optical amplitude by adjusting the modulated current ($I_{\rm mod}$) as temperature fluctuates. The characteristic of the LD *P-I* curve for different temperatures is shown in Fig. 2. The LDD maintains stable average power and optical amplitude over a broad temperature effectively with the cooperation of these three circuit modules.

Traditional LDDs require line coding for input

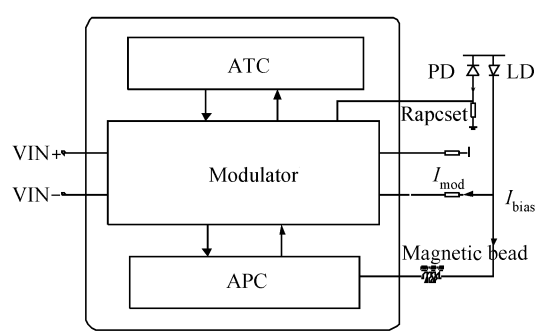

Fig. 1 Architecture of traditional LDD

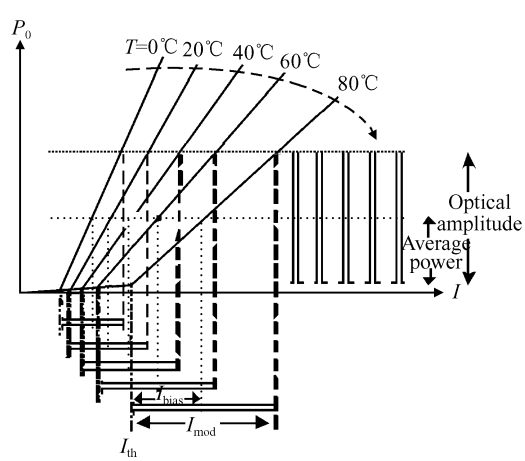

Fig. 2 LD *P-I* curve

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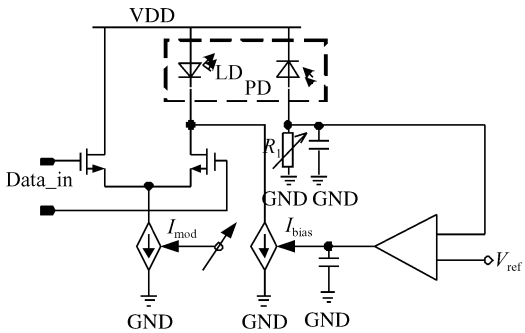

Fig. 3 Representative architecture of APC

signals in advance (e. g., 4B5B, 8B10B)[2,3], which will result in symmetrical '0' and '1' distribution and DC balance. An APC keeps average optical power stable in this condition. The typical architecture of an APC is shown in Fig. 3.

As shown in Fig. 3, the PD (photo diode) is the back-facet photodiode of the LD and the current from the PD is proportional to the LD optical intensity. After a low pass filter, the PD current is converted to a low frequency monitor voltage. This voltage is compared with an internal reference (V_{ref}) and the result is used to adjust the I_{bias} to achieve stable average optical power. The optical power can be changed by adjusting R_1.

The bandwidth of the APC loop is very low to prevent I_{bias} from high frequency noise, so the APC cannot work well when the input data rate is closed to DC. To solve this problem, this paper presents an LDD architecture aimed at low speed applications, which is called APPC (automatic peak-peak control, Fig. 4). The APPC can hold the peak-to-peak optical power ($P_{P\text{-}P}$) and extinction ratio (Er) stable without line coding.

2.2 Operation theory

As shown in Fig. 4, I_{set1} is the expected PD monitor current when LDD drives '1' and I_{set0} is the expected PD monitor current when LDD drives '0', both of which can be adjusted independently by resistors off-chip and are independent of temperature.

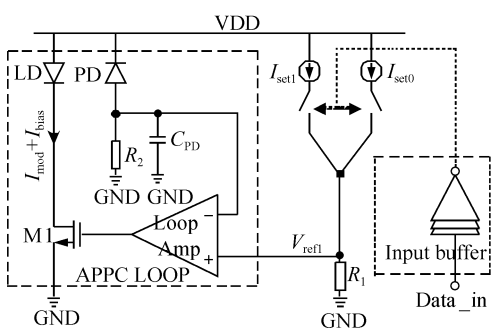

Fig. 4 Architecture of APPC

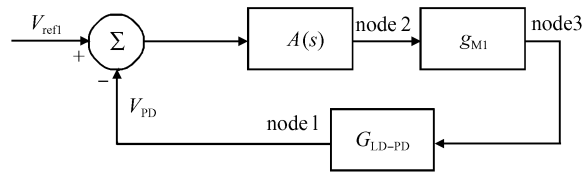

Fig. 5 Linear model of APPC loop

Reshaped by the input buffer, the input signal (Data_in) is used to switch the current source (I_{set1} or I_{set0}) that the APPC loop will track (see Fig. 4). P_1 here denotes the peak optical power of '1' and P_0 denotes the peak optical power of '0'. When Data_in is '1', the track target of the APPC loop is P_1, set by an external resistor. When Data_in is '0', the track target of APPC loop is P_0 set by another external resistor. The definition of Er is:

$$\mathrm{Er} = 10\lg(P_1/P_0) \tag{1}$$

If P_1 and P_0 overcome the influence from the variety of LD *P-I* curves over a broad temperature to preserve stabilization, then a stable Er can be achieved.

Contrary to traditional APC loops, the bandwidth of the APPC is so broad that the loop can setup and achieve stabilization in a short time after a switch between I_{set1} and I_{set0}. Line coding is not needed here because APPC can keep $P_{P\text{-}P}$ and Er stable, and average power may not be stable. In general, the operation data rate of this LDD primarily depends on the loop stability.

3 Analysis of key circuit parameters

The APPC loop is a typical negative feedback loop and its key parameters include the magnitudes of the setting currents, gain between the LD drive current and the PD current, values of PD filter components, and the dominant pole of the loop amplifier. These parameters determine the loop performance such as stability, phase margin, bandwidth, and gain.

3.1 Analysis of loop stability

Figure 5 is the linear model of the APPC loop (see Fig. 4). In Fig. 5, V_{ref1} is the reference voltage associated with I_{set1} and I_{set0}, V_{PD} is the PD anode voltage, $A(s)$ is the gain of the loop amplifier, g_{M1} is the transconductance of M1, and $G_{LD\text{-}PD}$ is the electrical gain between the LD drive current and the PD current. This model treats the loop amplifier as a single pole system. The transfer functions in Fig. 5 are given as follows:

$$A(s) = \frac{A_{dI}}{1 + SR_{O1}C_{O1}} \tag{2}$$

where R_{O1} is the output impedance and C_{O1} is the out-

put capacitance of the amplifier.

$$g_{M1} = \sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L_{M1}} (I_{mod} + I_{bias})} \tag{3}$$

where $I_{mod} + I_{bias}$ is the sum of the modulated current and bias current through LD.

$$G_{LD\text{-}PD} = \frac{\rho(T)\eta R_2}{(1 + sr_{LD}C_{O2})(1 + sR_2 C_{PD})} \tag{4}$$

where $\rho(T)$ is the LD slope efficiency, which is relative to temperature, η is the PD monitor efficiency, r_{LD} is LD AC impedance, and C_{O2} is parasitic capacitance at LD cathode.

According to these equations, the system transfer function is:

$$\begin{aligned} H(s) &= \frac{\partial V_{PD}}{\partial V_{ref1}} = A(s) \times g_{M1} \times G_{LD\text{-}PD} \\ &= \frac{A_{dI}\sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L_{M1}} (I_{mod} + I_{bias})}\rho(T)\eta R_2}{(1 + sR_{O1}C_{O1})(1 + sr_{LD}C_{O2})(1 + sR_2 C_{PD})} \Bigg/ \\ &\left(1 + \frac{A_{dI}\sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L_{M1}} (I_{mod} + I_{bias})}\rho(T)\eta R_2}{(1 + sR_{O1}C_{O1})(1 + sr_{LD}C_{O2})(1 + sR_2 C_{PD})}\right) \\ &= \frac{G(s)}{1 + G(s)} \end{aligned} \tag{5}$$

where $G(s)$ is the open-loop transfer function. At a certain temperature, $\rho(T)$ is represented by a constant ρ, so $G(s)$ is given by Eq. (6).

The loop stability is determined mostly by ω_1 and ω_2. ω_1 is the dominant pole of $G(s)$ and ω_2 is the second-most-dominant pole of $G(s)$. The loop is apt to be stable if ω_1 is smaller than ω_2. Reducing ω_1 or lowering loop gain will increase the loop phase-margin and improve the loop stability, while the loop bandwidth will be reduced at the same time. Given the guaranteed loop bandwidth, the loop stability can be improved by reducing the output impedance of the second-most-dominant pole and the parasitic capacitance.

$$G(s) = \frac{A_{dI}\sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L_{M1}} (I_{mod} + I_{bias})}\rho\eta R_2}{(1 + sR_{O1}C_{O1})(1 + sr_{LD}C_{O2})(1 + sR_2 C_{PD})} \tag{6}$$

3.2 Optimization of phase-margin

A sufficient phase-margin is crucial to loop stability. According to Eq. (5) and the APPC linear model shown in Fig. 5, the dominant pole is placed on node 1 and determined mainly by adjustable filter capacitor C_{PD} and PD junction capacitance, which is difficult to evaluate. If the dominant pole is placed on node 2 or node 3, unexpected noise will be amplified by the loop amplifier and influence the LD drive current. With the given specification, according to Eq. (6), the numerator of $G(s)$ can be treated as a constant, and when $R_{O1}C_{O1} < R_2 C_{PD}$ and $r_{LD}C_{O2} < R_2 C_{PD}$ are satisfied, the dominant pole will be $\omega_p = 1/R_2 C_{PD}$.

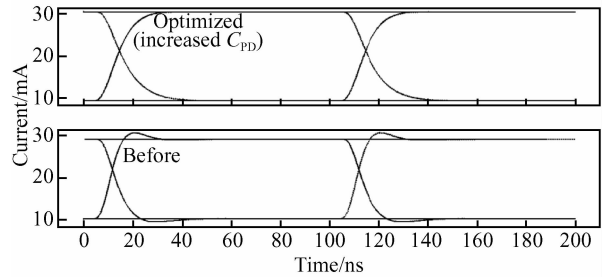

Fig. 6　Eye-diagram by improved stability

The consistency of the LD and PD parameters should be considered during optimization. For certain LD and PD, with 65dB loop gain and a 10Mbps data rate, simulation results show that a 100 to 200pF C_{PD} can meet the phase margin requirement. As shown in Fig. 6, when changing C_{PD} from 100 to 200pF, the waveform of the simulated LD drive current ($I_{bias} + I_{mod}$) is improved because of the increased phase margin (reach 71.5°). The associated gain and phase characteristic is shown in Fig. 7.

3.3 Guarantee of the cross point

Figure 6 illustrates that the cross point of the eye diagram was close to the center. This is very important for small PWD (pulse width distortion) and is guaranteed by the output of the input buffer shown in Fig. 4. The input buffer is used to judge and reshape the input data. As a low-speed TTL or CMOS input signal, its rise time and fall time can change dramatically. The input buffer's output will be used to select I_{set1} or I_{set0} and its eye diagram cross point will determine the eventual output waveform quality. The input buffer can adjust the judgment threshold according to the input signal to keep the ideal output cross point by its symmetrical output. The architecture of the input buffer is shown in Fig. 8. M1-M8 constructs a comparator. The threshold adjuster samples the high level of DIN and latches it. Its medium value (V_{th}) is used as the judgment threshold.

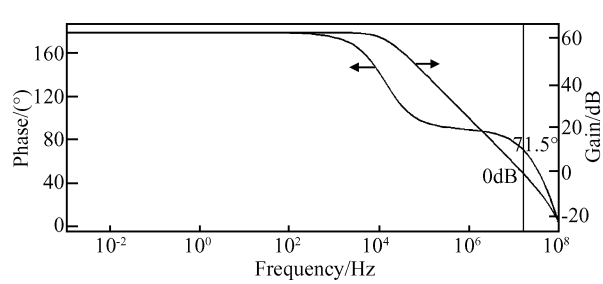

Fig. 7　Stability analysis of loop

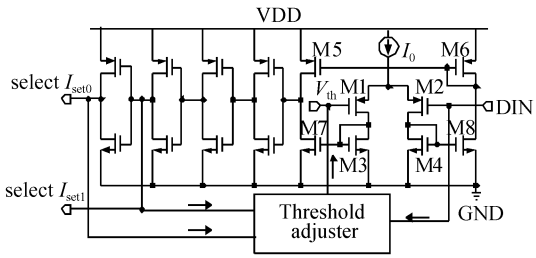

Fig. 8 Input buffer

4 Implementation and measurement

4.1 Implementation

Based on the theoretical analysis, the key circuit parameters in Section 3 are chosen to hold the APPC loop stable under all process corners. The chip was implemented in CSMC 0.5μm mixed signal CMOS technology with a 1.5mm × 1.9mm die area and the micrograph of the chip is shown in Fig. 9. As a single end mixed signal driver, it must be arranged and routed carefully to minimize the crosstalk. A guard-ring is placed around different blocks. The power supply and ground are divided into digital and analog sections to prevent unexpected coupling. Furthermore, the transistors with large areas are realized in a multi-finger structure, which will reduce the parasitic capacitance greatly[4].

4.2 Measurement

With 5V supply, the LDD is coupled with LD directly. The main testing instruments consist of a SMP04 signal generator, a regulated DC power supply PMR18-1.37R, and an Agilent 86100A optical oscilloscope.

Test results indicate that the circuit can maintain stable $P_{P\text{-}P}$ with a PRBS (pseudorandom bit sequence) and fixed pattern input, and Er is almost invariable. The variations of P_1 and P_0 over temperature are shown in Fig. 10 and are independent of input pattern. P_0 changed only about 0.4dB over $-20\sim+80$℃

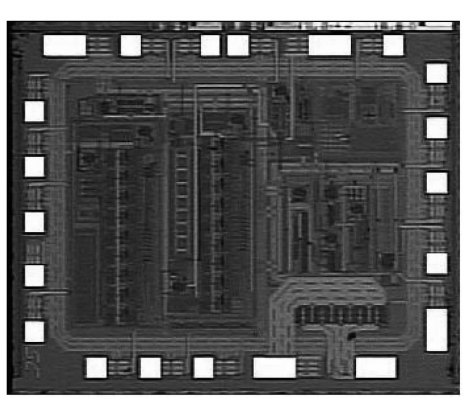

Fig. 9 Micrograph of LDD chip

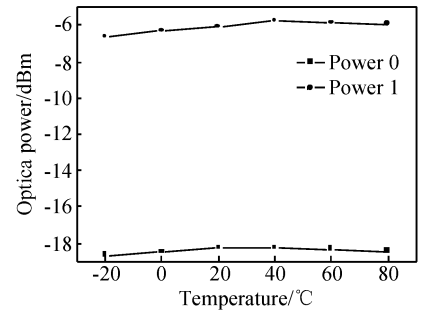

Fig. 10 P_1 and P_0 over temperature

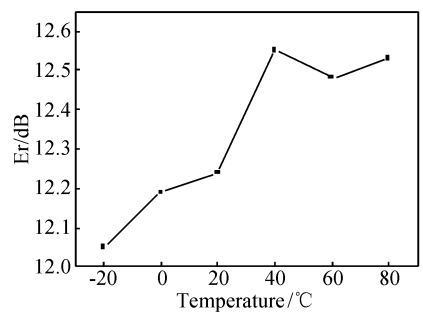

Fig. 11 Er over temperature

and P_1 changed only about 0.9dB over $-20\sim+80$℃. Er over temperature is shown in Fig. 11 and it changed less than 0.6dB over $-20\sim+80$℃, for a variation of about 2.6%. The output optical pattern with the '1000000000' periodical sequence is shown in Fig. 12; the bit rate is 10Mb/s. I_{set1} is 1.03mA (P_1 is

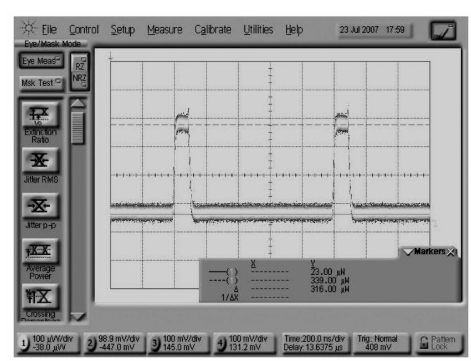

Fig. 12 Operation at 10Mb/s

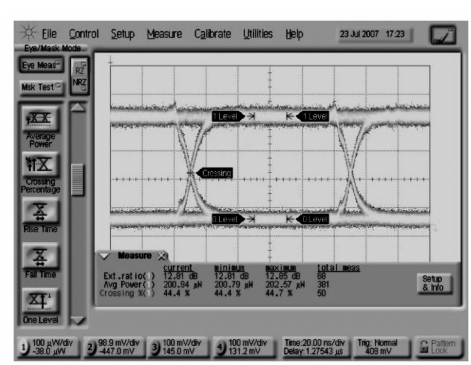

Fig. 13 Eye diagram at 10Mb/s

Table 1　Summary of optical test results (@10Mb/s, I_{set1} = 1.03mA, I_{set0} = 95μA)

Parameter	Average power/μW	Extinction ratio/dB	Rise time (10%～90%) /ns	Fall time (10%～90%) /ns	P-P jitter/ns	RMS jitter /ps
MIN	191.77	11.63	15.56	16.89	–	–
Typical	200.94	12.81	15.89	17.11 3	416	
MAX	202.57	12.85	25.8	24.4	–	–

339μW) and I_{set0} is 95μA (P_0 is 23μW). Figure 12 indicates that LDD works well without line coding. Figure 13 is the eye diagram with $2^{15}-1$ PRBS input, and the RMS jitter is 416ps and the peak to peak jitter is 3ns. It has a 200pF CPD for APPC loop stability. This proves that the loop has enough phase-margin and no overshoot on drive current, which coincides with the simulation results (Fig. 6) perfectly. The test results in Fig. 13 are summarized in Table 1.

5　Conclusion

The design of a DC-10Mb/s LDD with a novel structure is presented. Without traditional APC and ATC, the APPC loop structure used here can keep $P_{P\text{-}P}$ and Er stable over a broad temperature range without line coding. Tested with PRBS and fixed patterns, the variation of P_1 and P_0 is 1.8% and 0.8% over −20～+80℃, respectively, with a variation of Er less than 2.6%. The maximum drive current is 120mA and the typical power dissipation is 100mW without considering the drive current.

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DC-10Mb/s 0.5μm CMOS 激光器驱动电路的实现

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摘要： 设计并实现了一种适用于 DC-10Mb/s 速率、兼容 TTL 和 CMOS 输入电平的激光器驱动电路. 该电路通过片外电阻可以独立地设置激光器发送光脉冲的'1'功率和'0'功率，并以闭环方式实现稳定的'1'，'0'发送光功率. 介绍了一种新颖的峰-峰值光功率检测的工作机制，并能得到稳定的峰-峰值光功率. 整个电路采用 CSMC 0.5μm 混合信号 CMOS 工艺实现，芯片最大输出驱动电流为 120mA，在不要求输入码型的情况下，发送光脉冲的消光比波动在 −20～+80℃ 范围内小于 0.6dB.

关键词： 激光器驱动电路；CMOS；消光比；温度补偿
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