An Improved Charge-Averaging Charge Pump for a Fractional-*N* Frequency Synthesizer*

Zhang Jian†, Huang Shuilong, Li Zhiqiang, Chen Pufeng, and Zhang Haiying

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: An improved charge-averaging charge pump and the corresponding circuit implementation are presented. The charge-averaging charge pump proposed by Koo is analyzed and a new scheme is proposed. This new scheme decreases power by 1/3 and eliminates the practical defects in the original. Spectre Verilog behavioral simulation results show that the proposed scheme can strongly reduce the energy of spurs. Circuit implementation of this new charge pump for a frequency synthesizer with a fractional division ratio of 1/3 is then presented and multi-level simulation is performed to validate its feasibility at the circuit level. The simulation results show this new scheme outputs a flat voltage curve in a locked state and can thus effectively suppress fraction spurs.

Key words: charge-averaging; charge pump; spur
EEACC: 1280
CLC number: TN43 **Document code**: A **Article ID**: 0253-4177(2008)05-0913-04

1 Introduction

A fractional frequency synthesizer can achieve both high frequency resolution and fast settling by decoupling the frequency resolution from the reference frequency. One major disadvantage of fractional-*N* PLL is the generation of fractional spurs located at multiples of the channel spacing. There are a variety of techniques reported in the literature to solve this problem. Such techniques can be divided into two categories: the classical technique and delta-sigma modulation techniques. The classical technique employs dithering and phase interpolation to reduce the spurs, but the main performance limitation is the lack of precise analog components. The delta-sigma modulation approach is used to randomize the division ratio, such that the quantization noise of the fractional divider is transferred to higher frequencies. The problem with this architecture is that the quantization noise leads to the degradation of spectral purity. Furthermore, it poses a very stringent requirement on the linearity of the phase/frequency detector and charge pump.

A charge-averaging charge pump was proposed by Koo[1]. This technique offers a new perspective for the suppression of fractional spurs. Novel in nature, the original scheme still suffers from defects, as will be shown in section 2. A new charge-averaging charge pump is proposed in section 3. System simulation with Spectre Verilog validates its role in fractional spur suppression for a fractional-*N* frequency synthesizer. The circuit implementation of the proposed improved charge pump is given in section 4. Multi-level simulation verifies the feasibility of this new scheme.

2 Koo's original scheme

The conventional charge-averaging charge pump proposed by Koo is shown in Fig. 1. It consists of four current sources with current of 1/3 the total current and four charge-collecting capacitors. This scheme applies to frequency synthesizers with a fractional division ratio of 1/3. To realize such a frequency synthe-

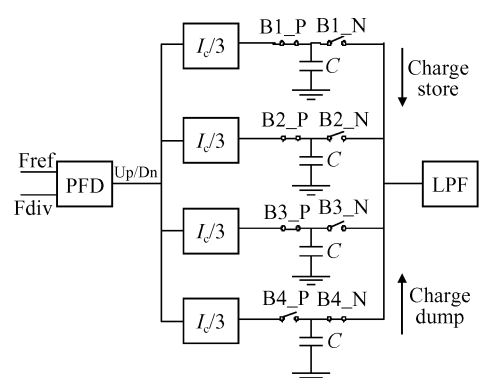

Fig. 1 Conventional charge-averaging charge pump

* Project supported by the National Natural Science Foundation of China (No. 60276021) and the State Key Development Program for Basic Research of China (No. G2002CB311901)
† Corresponding author. Email: zhangjian@ime.ac.cn
Received 7 November 2007, revised manuscript received 30 November 2007

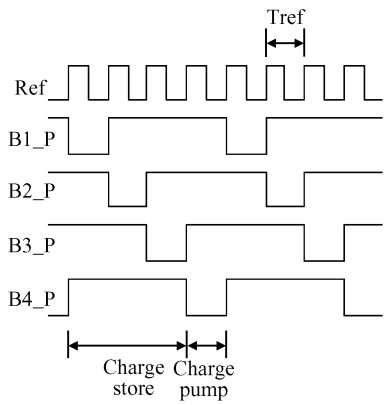

Fig. 2 Charge-averaging operation

sizer, the prescaler division factor is $M+1$ in one cycle and M in the other two cycles in every successive three cycles. This produces periodic voltage ripples in the control signal of the VCO and, therefore, a fractional spur occurs. However, the sum of phase errors during any three successive clock cycles is zero in the locked state. By realizing this, three of the four capacitors are used to collect charges when the left capacitor is dumping the charges it collected in the previous three cycles, as shown in Fig. 2. Because of the zero phase error of three cycles, the voltage at Vctrl is held constant and no voltage ripple is produced. With a few modifications, this scheme applies to any fractional frequency synthesizers.

However, there are still defects in this scheme. The first arises from the four current sources, which are difficult to match in practice. The paths from the PFD output to these four current sources make it difficult to equalize the delays. These non-idealities lead to spurs at the output spectrum. Another drawback is the increased power consumption. Since four current sources with an output current of $I_c/3$ are used, the total current consumption is $4I_c/3$.

3 Proposed charge-averaging scheme

The proposed charge-averaging scheme is shown in Fig. 3. The basic theory is the same as the conventional theory, except that the current is now provided by only one current source with an output current of I_c, which leads to a current saving of $I_c/3$. Charges are first collected by capacitor C1 and then distributed to three identical switching capacitors. Compared to the conventional scheme, only one charge pump is needed, so the circuit design is greatly simplified and there is no current mismatch problem. The PFD output signals are now fed to only one current source, so the delay difference is eliminated. An additional capacitor C_{add} provides an alternate path for charges from the charge pump and helps to eliminate the potential risk of saturating current sources.

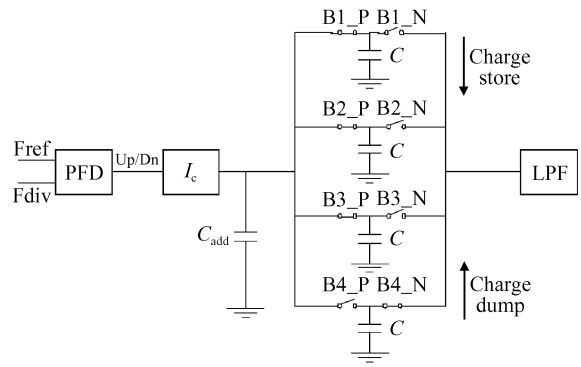

Fig. 3 Improved charge-averaging charge pump

To verify the scheme's effect on the spectral purity, a simple PLL based frequency synthesizer employing the proposed charge-averaging charge pump is described with Verilog/VerilogA. The system topology is illustrated in Fig. 4. The reference frequency is 0.9MHz and the charge pump current is 0.8mA. The VCO has a 1.77～1.83GHz frequency tuning range. A third-order low pass filter is employed as the loop filter. To speed the settling, one branch in the charge averaging scheme is connected directly to the loop filter, while the other three branches are left open in the acquisition mode.

The simulated spectral purity of the scheme with/without charge-averaging is shown in Fig. 5. For the charge pump without charge-averaging, the spur level is about −80dBc. However, the fractional spur in Fig. 5 (b) is suppressed to nearly −100dBc. This indicates the effects of the charge-averaging scheme on spur suppression.

4 Circuit implementation of the proposed charge pump

A high performance charge pump with perfect current matching characteristics is designed to validate the proposed scheme at the circuit level. The charge pump is implemented with TSMC 0.18μm

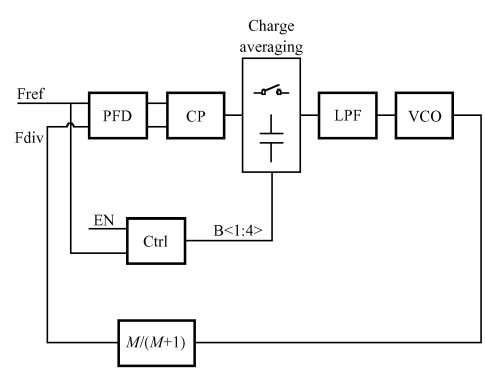

Fig. 4 PLL system used in simulation

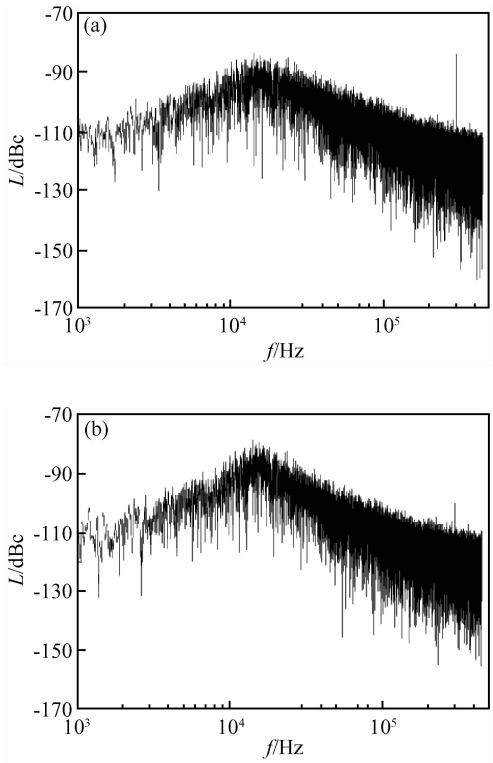

Fig. 5　Spectral purity of the loop without (a) and with (b) charge-averaging

1P6M CMOS technology. The topology is shown in Fig. 6. Operational amplifier OP1 is holds the voltage of node A equal to node B. M4 and M7 are dummy transistors. The size ratio of M4 to M5 and M7 to M8 are the same as M2 to M3 and M10 to M11. Figure 7 shows the static characteristic of the up and down current source with output voltage ranges from 0 to 1.8V. Figure 7 shows that with this configuration, the two current sources can be perfectly matched from 0.2 to 1.6V output range. Operational amplifier OP2 addresses the charge sharing issue associated with the gate-switching type charge pump[2]. A 10pF capacitor serves as the additional capacitor C_{add}, which should be accounted for when designing the loop filter.

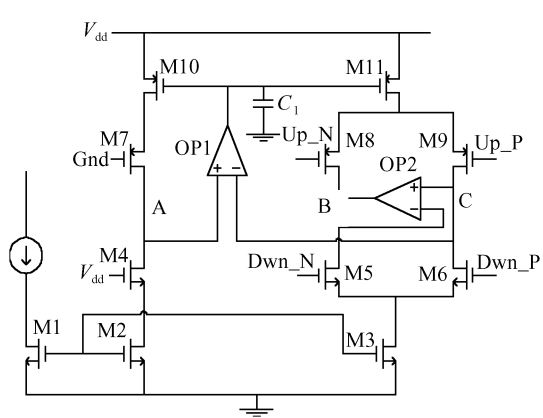

Fig. 6　Charge pump topology

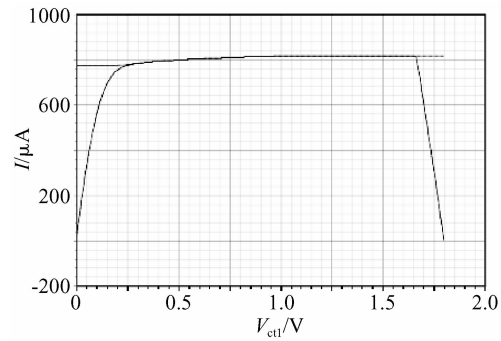

Fig. 7　Up and down current of charge pump

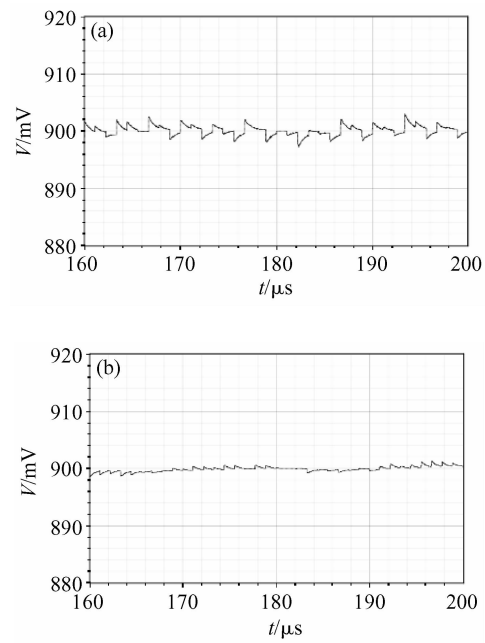

Fig. 8　Control voltage in locked state without (a) and with (b) charge-averaging

Multi-level simulations with and without the improved charge-averaging charge pump scheme are then performed by replacing the charge pump behavioral model in the previous simulation with this circuit implementation. The improved charge-averaging charge pump works well during the entire acquisition and holding processes, and no saturation occurs. The simulated control voltage in the locked state with and without charge-averaging is shown in Fig. 8. The ripple without charge-averaging is much more significant than that with charge averaging, which demonstrates the role of this improved charge-averaging charge pump on spur suppression.

5　Conclusion

A new charge-averaging charge pump scheme is proposed based on the work of Koo. This new scheme is more robust and more power-efficient. Both behavioral and circuit level simulations validate its

feasibility for spur reduction in a fractional frequency synthesizer.

References

[1] Koo Y, Huh H. A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and Celluar-CDMA wireless systems. IEEE J Solid-State Circuits, 2002, 37: 536

[2] Rhee W. Design of high performance CMOS charge pumps for phase-locked loops. Proc IEEE International Symposium on Circuits and Systems (ISCAS), May, 1999: 545

用于分数频率综合器的改进型电荷平均电荷泵*

张 健† 黄水龙 李志强 陈普峰 张海英

(中国科学院微电子研究所，北京 100029)

摘要：介绍了一种改进型的电荷平均电荷泵以及相应的电路实现.文章在对 Yido Koo 首先提出的电荷平均电荷泵结构分析的基础上提出了改进型的实现方式.相比于原结构，这种新型电路能够节省 1/3 的功耗并且消除了原先结构在实际实现中的一些问题.Spectre Verilog 行为级仿真结果证明该结构能够有效降低杂散能量.本文同时设计了一个针对分数分频比为 1/3 的小数频率综合器的改进型电荷共享电荷泵，并通过多层次仿真的方式来验证其可行性.从仿真结果可以看出，这种新结构输出电压稳定，从而能够有效消除频率综合器中的分数杂散.

关键词：电荷平均；电荷泵；杂散

EEACC：1280

中图分类号：TN43 **文献标识码**：A **文章编号**：0253-4177(2008)05-0913-04

* 国家自然科学基金(批准号：60276021)和国家重点基础研究发展规划(批准号：G2002CB311901)资助项目

† 通信作者. Email：zhangjian@ime.ac.cn

2007-11-07 收到，2007-11-30 定稿