An Analytical Model of Drain Current for Ultra-Thin Body and Double-Gate Schottky Source/Drain MOSFETs Accounting for Quantum Effects*

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Abstract: A compact drain current including the variation of barrier heights and carrier quantization in ultrathin-body and double-gate Schottky barrier MOSFETs (UTBDG SBFETs) is developed. In this model, Schrödinger's equation is solved using the triangular potential well approximation. The carrier density thus obtained is included in the space charge density to obtain quantum carrier confinement effects in the modeling of thin-body devices. Due to the quantum effects, the first subband is higher than the conduction band edge, which is equivalent to the band gap widening. Thus, the barrier heights at the source and drain increase and the carrier concentration decreases as the drain current decreases. The drawback of the existing models, which cannot present an accurate prediction of the drain current because they mainly consider the effects of Schottky barrier lowering (SBL) due to image forces, is eliminated. Our research results suggest that for small nonnegative Schottky barrier (SB) heights, even for zero barrier height, the tunneling current also plays a role in the total on-state currents. Verification of the present model was carried out by the device numerical simulator-Silvaco and showed good agreement.

Key words: Schottky barrier; quantum effects; the effective mass; electron density
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1 Introduction

The Schottky barrier MOSFET has a similar device structure to the conventional MOSFET, but the source/drain regions are made of silicide or metal rather than heavily doped semiconductor[1,2]. The device offers several potential advantages over a conventional MOSFET at nanometer scale. Therefore, scaling beyond the limit of the conventional MOSFET is being explored. By using metal source/drain, SBFETs would essentially eliminate the parasitic resistance, and thus could deliver more on current than the conventional MOSFETs[3,4]. As modern VLSI devices scale down, the gate oxide is getting thinner. Consequently, the strong transverse electric field and deep potential well near the Si/SiO_2 interface lead to the quantization of mobile carrier energy, i.e., quantum mechanical effects (QME's).

QME's have significant influence on MOSFET behavior such as threshold voltage shift[5], maximum gate capacitance scaling, and low voltage application[6]. Theoretical studies of SBFETs have focused on assessing device operation at nanometer scale, treating the tunneling through Schottky barriers and fitting the experimental data[7~9]. For thin body devices, quantum confinement raises the electron energy levels in the silicon and the effective barrier height. In this paper, the solution of the Schrödinger equation under the triangular potential well approximation is coupled with the numerical solution of the Poisson equation. An iteration procedure is employed to find the self-consistent results of carrier distribution and potential profile in the inversion and accumulation layer in the MOS structure. An effective electric field is defined by combining the mobile carrier sheet density and depletion charge sheet density. Then, a closed form of drain current for UTBDG SBFET is presented fully, including QM effects. Model verification is carried out using the 2-dimensional device simulator Silvaco[10].

2 Drain current modeling

2.1 Energy band model and quantum charge

The structure of the UTBDG SBFET is depicted in Fig. 1. Determining the carrier distribution and potential profile in the quantized inversion and accumulation layer in UTBDG SBFET structure requires solving coupled Schrödinger's and Poisson equations.

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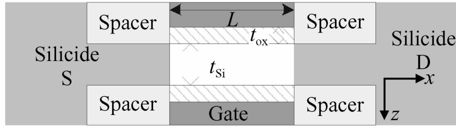

Fig. 1 Illustration of UTBDG SBFET with silicide/metal source and drain

The one-dimensional (1-D) Poisson equation is given as:

$$\frac{d^2\phi(z)}{dz^2} = -\frac{q}{\varepsilon_{Si}}(p - n + N_{sub}) \quad (1)$$

where $\phi(z)$ is electric potential; p and n are hole and electron concentration, respectively; and N_{sub} is the channel doping concentration. In the vertical direction (the z-direction in Fig. 1), the Schrödinger's equation was solved for each x-position independently to generate eigen-energy of the ith subband and jth valley E_{ij} and the corresponding wave function Ψ_{ij}

$$-\frac{\hbar^2}{2m_{zj}^*} \times \frac{d^2\Psi_{ij}}{dz^2} - q\phi(z)\Psi_{ij} = E_{ij}\Psi_{ij} \quad (2)$$

where m_{zj}^* is the effective mass along the z-direction of the jth valley with $m_{z1}^* = 0.916m_0$ ($m_0 = 9.1 \times 10^{-31}$kg) and $m_{z2}^* = 0.910m_0$ (subscript 1 referring to the unprimed valley and 2 referring to the primed valley for a silicon with ⟨100⟩ crystal orientation, $\hbar$ is the reduced Planck's constant, and m_0 the free electron mass).

In earlier works, the solutions to energy levels for MOS structure using parabolic profile are reasonable both in the subthreshold region and in the strong inversion region. However, an analytical solution can not be obtained on the basis of parabolic potential. The theory of quantum mechanics shows that the lower energy levels rest on the potential distribution at the bottom of the potential well. Thus, we assume a triangular well in the channel and infinitely high potential barriers at the silicon/oxide interfaces along the z-direction. Then, the solution of Schrödinger's equation in triangular potential well is,

$$E_{ij} = \left(\frac{\hbar^2}{2m_{zj}^*}\right)^{1/3} \times \left[\frac{3}{2}\pi qF_s\left(i + \frac{3}{4}\right)\right]^{2/3} \quad (3)$$

To define F_s in Eq. (3), an effective electric field in inversion layer is adopted:

$$F_s = q(\eta N_e + N_d)/\varepsilon_{Si} \quad (4)$$

where N_e and N_d are inversion carrier density and depletion charge density, respectively; and η is a fit parameter. In the accumulation layer, N_d is zero and N_e is the accumulation carrier density. In Refs. [11,12], η is taken as 0.5. Although the value of 0.5 is often used in the modeling of the universality of the mobility of inversion layer carriers (for electrons only), it is not reasonable that the value should remain unchanged when applied in the calculation of carrier density. In this work, it is taken as an adjustable parameter.

Due to the confinement of electron motion normal to the interface, the conduction band within the transistor channel is split into several subbands, each of which is associated with the corresponding eigenenergy. Hence, the electron density in the channel may be expressed as

$$N_e = \sum_i \sum_j N_{ij} = \sum_i \sum_j D_j k_B T \ln\left[1 + \exp\left(\frac{E_{Fn} - E_{ij}}{k_B T}\right)\right] \quad (5)$$

where $D_j = (g_j m_{dj}^* k_B T/\pi\hbar^2)$ is the density of states in the jth valley and m_{dj}^* is the density of states of effective mass per valley ($m_{d1}^* = 0.190m_0$, $m_{d2}^* = 0.417m_0$). $g_1 = 2$, $g_2 = 4$ are the degeneracy of the valleys of the set. E_{Fn} is the quasi-Fermi level. The device current flows only along the channel so that the quasi-Fermi level is constant across the silicon-film direction (z-direction). k_B is the Boltzmann constant and T is the absolute temperature. The expression of Y_e (the average distance of all electrons from the surface) formulated assuming the triangular potential well (TPW) approximation is

$$Y_e = \frac{\sum_j \sum_i N_{ij} Y_{ij}}{N_e} = \frac{\sum_j \sum_i N_{ij} Y_{ij}}{\sum_j \sum_i N_{ij}} \quad (6)$$

where $Y_{ij} = 2E_{ij}/3F_s$ is the average separation of carriers in the ith subband and jth valley.

2.2 Drain current modeling

For calculating the drain current in a UTBDG device with metal S/D, two major transport mechanisms through the Schottky contacts are considered: thermionic emission and barrier tunneling. At a given bias, the net current density flowing through a metal-semiconductor contact is[4]

$$J = J_{therm} + J_{tun} \quad (7)$$

$$J_{therm} = \sum_i \sum_j \frac{A^* T}{k_B} \int_{q(\phi_{b0} - \Delta\phi_b - V_a)}^{\infty} [f_s(E_{ij}) - f_m(E_{ij})] dE_{ij} \quad (8)$$

$$J_{tun} = \sum_i \sum_j \frac{A^* T}{k_B} \int_0^{q(\phi_{b0} - \Delta\phi_b - V_a)} T_t(E_{ij})[f_s(E_{ij}) - f_m(E_{ij})] dE_{ij} \quad (9)$$

$$f_s(E_{ij}) = \frac{1}{1 + \exp\left(\frac{E_{ij} - E_{fs}}{k_B T}\right)} \quad (10)$$

$$f_m(E_{ij}) = \frac{1}{1 + \exp\left(\frac{E_{ij} - (E_{fs} - qV_a)}{k_B T}\right)} \quad (11)$$

Assume the conduction band edge inside the silicon as the reference point. $f_s(E)$ and $f_m(E)$ are the Fermi-Dirac (F-D) distributions at semiconductor and metal, respectively. $T_t(E)$ is the transmission coeffi-

cient. V_a is the forward bias across the Schottky contact. The effective Richardson's coefficient A^* is

$$A^* = \frac{4\pi q k_B^2 m_{dj}^*}{h^3} \tag{12}$$

As a factor affecting the electrical transport, Schottky barrier lowering (SBL) due to the image force effect and the interfacial layer is also considered in our study, and is

$$\Delta\phi_b = \sqrt{\frac{q\alpha F_{sm}}{4\pi\varepsilon_{Si}}} + \gamma F_{sm} \tag{13}$$

Here, F_{sm} is the maximum lateral field at the Schottky contact. The first term in Eq. (13) describes the SBL due to the image force; the second term is generated by the interfacial film. α is a fitting parameter. Classical theory sets it to one[13]. However, fitting this model to empirical data suggests that this value varies and depends on V_{ds} and L. The value of γ is usually set to 1.5~3nm and is set to 1.5nm here.

To perform the model's caculations, rather than performing an integral over an energy range for Eqs. (8) and (9), a Riemann sum over a fine energy grid (ΔE = 0.001 to 0.01eV) was used. Also, instead of using ∞ as the final energy in Eq. (8), a finite value between one and three (depending on V_{ds}) is equally useful, as the tail of the F-D distribution becomes very small very quickly. Furthermore, V_{ds} must also be included to account for the difference in F-D distribution between the source and drain at a given energy.

A nonlocal tunneling model is employed based on the Fermi-Dirac distribution function in our model and the tunneling probability based on the WKB approximation is

$$T_t(E_{ij}) = \exp\left\{\frac{2}{\hbar\, q}\sqrt{\frac{m_{dj}^*\varepsilon_{Si}}{N_e}} \times \left[E_{ij}\ln\left(\frac{\sqrt{E_b}+\sqrt{E_b - E_{ij}}}{\sqrt{E_{ij}}}\right) - \sqrt{E_b}\sqrt{E_b - E_{ij}}\right]\right\} \tag{14}$$

where $E_b = q(\phi_{b0} - \Delta\phi_b - V_a)$. The effective mass in the above equation is anisotropic for electrons, which brings anisotropy to the tunneling current of electrons. Tunneling current is sensitive to the effective masses in Eq. (14). An accurate determination of the tunneling effective masses from experiments is thus important. Unfortunately, reliable experimental data of carrier tunneling effective masses for nanoscale contacts with a wide range of barrier heights are not available. The tunneling current is calculated based on the following assumptions. The tunneling current through a Schottky barrier is dominated by electrons with light masses because their tunneling probabilities are much larger, as expected from Eq. (14).

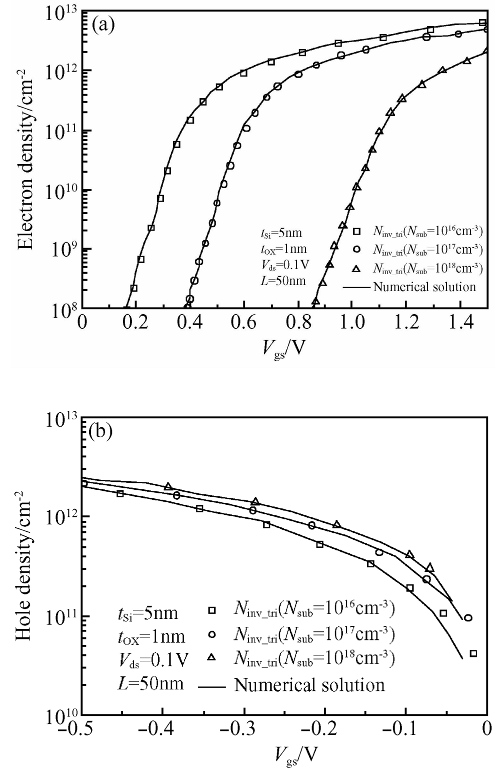

Fig. 2　Inversion layer carrier density (a) and accumulation layer carrier density (b) by analytical solution under the triangular potential well approximation (symbols) and by numerical simulation (line)

3　Results and discussion

The model was validated by an extensive comparison with a quantum numerical simulation using the 2D device simulator Silvaco. Figures 2 and 3 show the electron density in the inversion layer and the hole density in accumulation layer, respectively. When η is taken as 0.75 for the inversion layer and 0.80 for the accumulation layer, the carrier density coincides with the fully numerical calculation. The difference of η for electrons and for holes may lie in the different subband structure of the two kinds of layers. In the

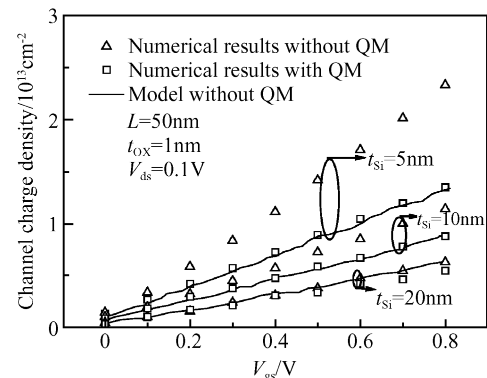

Fig. 3　Analytical charge densities are depicted against gate voltage with different t_{Si}

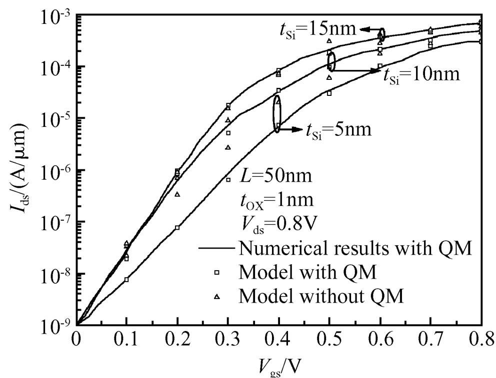

Fig. 4 Impact of silicon film thickness on the drain current for UTBDG SBFET

calculation, the coefficient in equation (4) is 0.75 for the inversion layer (electron) and 0.8 for the accumulation layer (hole).

In Fig. 3, the analytical charge densities are depicted against gate voltage with different thicknesses of silicon films (t_{Si}), agreeing with the numerical simulation results. The figure shows that the electron density increases as t_{Si} scales down. The results of our model agree with numerical results and the error becomes larger as t_{Si} decreases between the results considering QM effects or not. Figure 4 shows further calculation of drain current with and without QM effects for the S/D Schottky barriers (the gate work function for this device was selected to produce an off-current of 1nA/μm). The QM model perfectly reproduces two essential phenomena: the impact of quantum effects on drain current is increasingly significant when t_{Si} is scaled down; and the drain current depends on t_{Si} in the subthreshold region, but above the threshold, the drain current depends much less on t_{Si}.

The validation procedure was continued by an in-depth investigation of the model's capability to account for carrier quantization effects. For this purpose, the inversion charge density N_e (in both the classical and quantum cases) with two different channel lengths is compared to numerical results and very good agreement is found in Fig. 5. Figure 6 shows the first subband profile of these SBFETs under on-state conditions beyond a certain gate voltage. Somewhat surprisingly, a tunneling barrier still exists for $\phi_{b0}=0$. The current of the SBFETs with zero effective barrier heights is limited by the tunneling barrier at the source rather than the thermic barrier in the channel. For this thin body device, quantum confinement raises the electron energy levels in the silicon and the effective barrier height.

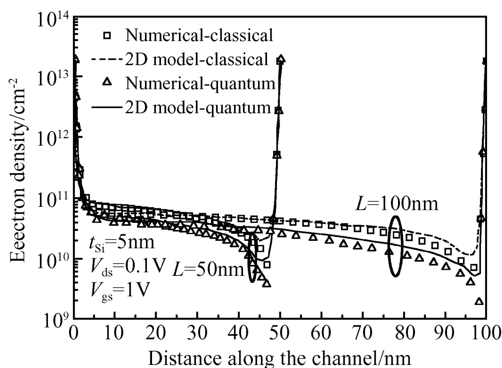

Fig. 5 Variation of the inversion charge density N_e in classical and quantum mechanical cases

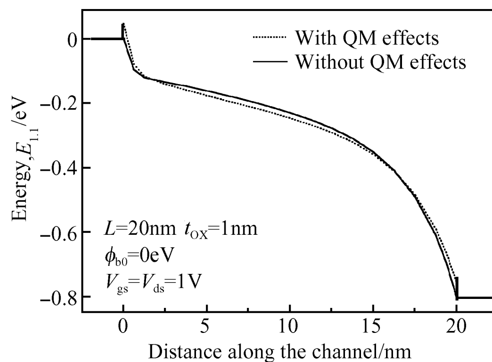

Fig. 6 Energy band diagrams of the 20nm UTBDG SBFET with Schottky barrier height zero

Figure 7 shows the energy band of SBFETs in on and off states with a SBH of $\phi_{b0}=0.56$eV comprising QM effects. When the device is in the off-state, the energy band resembles that of a conventional MOSFET with a large energy barrier between source and drain, and the current is limited by thermic emission over the barrier at the source. At the drain side, the Schottky barrier for holes is thin, which allows holes to tunnel from the drain terminal into the channel and causes extra leakage current. Thus, the off-state current is composed of either thermionic or tunneling components, depending on the gate work function and bias. Under higher gate bias, a conduction band spike appears at the source. The SB of electrons on the source side is thin, which allows electrons to

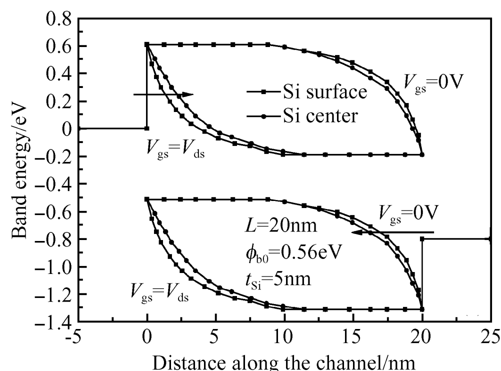

Fig. 7 Conduction and valence band from source to drain for UTBDG SBFETs

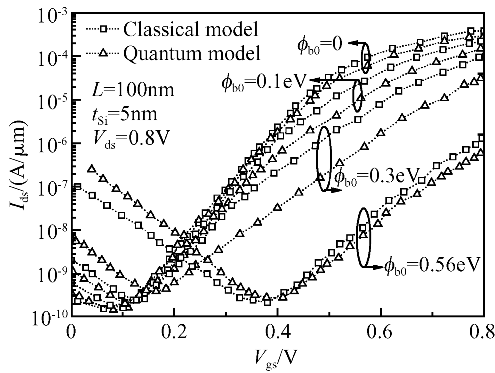

Fig. 8　I_{ds}-V_{gs} curves for UTBDG SBFETs with different Schottky barrier heights for electrons

tunnel from the source terminal into the channel.

Furthermore, the barriers are thicker in the center of the channel. The SBL (not shown in Fig. 7) is also smaller in the center of the channel. Thus, the favorable path for the tunneling current is near the surface rather than through the center of the channel. The lower the SB is for electrons, the higher the SB is for holes. As a result, the tunneling current of holes decreases, which explains the reduced holes for lower electron SB in Fig. 8. The minimum leakage current is insensitive to the SBHs and is the consequence of a tradeoff between electron and hole current. The minimum leakage currents of the zero barrier and the mid gap SBFETs are similar. The reason for this is that the gate oxide (t_{ox} = 1nm) in our model is very thin, and the SB is also very thin and essentially transparent for carriers. The current is, therefore, limited by thermic emission over a barrier with the height of the barrier determined by the conduction/valence band in the interior of the channel. Tunneling through the metal/semiconductor barrier varies with the barrier height and the bias, which plays a minor role (because the barrier is so transparent) compared to the barrier in the silicon body. Above the threshold, the situation is different. The tunneling resistance limits the on-state

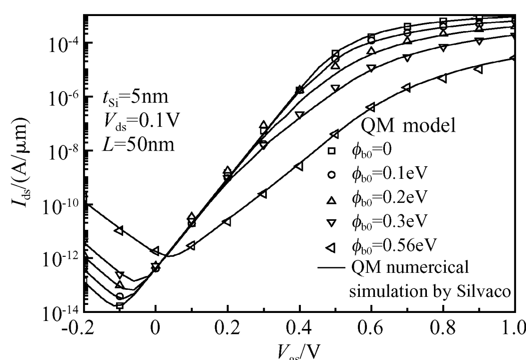

Fig. 9　I_{ds}-V_{gs} with different SBH at source/drain calculated by the QM model and validated

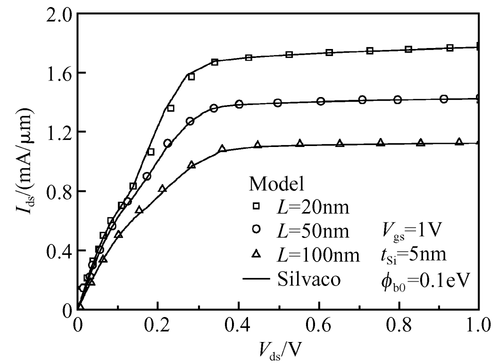

Fig. 10　Drain current with different channel lengths calculated by the QM model and validated

current and the zero barrier delivers more on-current. Moreover, as Figure 9 shows, the analytical solutions fully comprising QM effects with the triangular potential well approximation are in agreement with the numerical results. The model with only SBL overestimates the value of the drain current, as shown in Fig. 8.

The drain current with different channel lengths is shown in Fig. 10. Due to the existence of a Schottky barrier at the source/drain, the effect of drain bias on the channel is screened. Thus, the short channel effect (SCE) is eliminated. The model is in agreement with the numerical simulation.

The height of the Schottky barrier (SBH) at the source plays a significant role in drain current, as

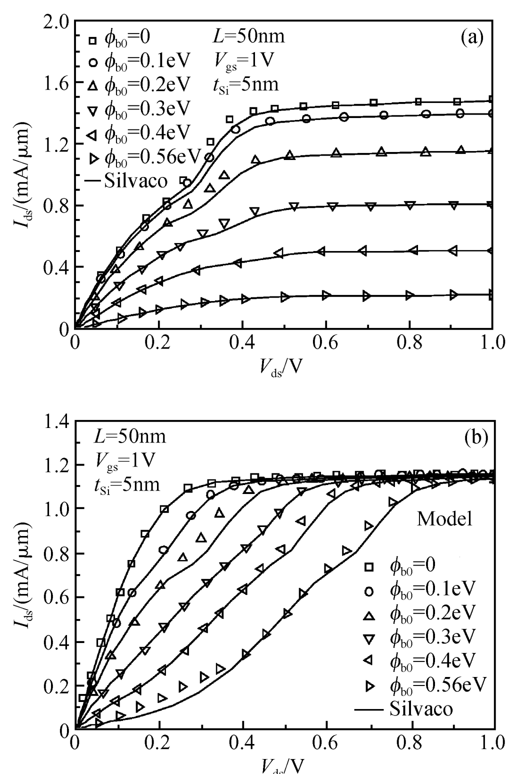

Fig. 11　Output characteristics of UTBDG SBFET with various barrier heights　(a) At the source; (b) At the drain

shown in Fig. 11 (a). However, the SBH at the drain has little influence on the device performance in Fig. 11 (b). The saturation current increases as the barrier height decreases, which implies increased tunneling current due to the low Schottky barrier height. As the barrier height increases, the drain current raises slowly with the drain voltage because the higher field is needed to tunnel the higher and thicker Schottky barrier. Moreover, Figure 11 shows that the drain current at low drain bias deviates from linearity. The exponential behavior of the I_{ds}-V_{ds} plot for the nMOS device at low drain bias demonstrates the presence of the Schottky barrier. The model agrees very well with the numerical simulation.

4 Conclusion

A short channel quantum compact model for drain current in thin-body double-gate SBFETs has been developed. For thin body devices, quantum confinement raises the electron levels in silicon and the effective barrier height. Previous works merely included the SBL in their models, either ignoring QM effects or making too coarse assumptions of the quantum potential well, which overestimated the drain current. The development of our model considering the analytical solutions to energy levels with the triangular potential well approximation was the starting point. According to our model, the current of the SBFETs with zero effective barrier heights involves the tunneling current due to quantum confinement. Regardless of barrier height the minimum leakage current is similar due to the thin gate oxide. Beyond the threshold, the lower Schottky barrier height delivers more on-current. The numerical results validate the proposed model.

References

[1] Kedzierski J, Xuan P, Anderson E H, et al. Complementary silicide source-drain thin-body MOSFETs for 20nm gate length regime. IEDM Tech Dig, 2000: 57

[2] Tao M, Agarwal S, Udeshi D, et al. Low Schottky barriers on n-type silicon (001). Appl Phys Lett, 2003, 83(13): 2593

[3] Pellegrini B. Properties of silicon-metal contacts versus metal workfunction, silicon impurity concentration and bias voltage. J Phys D: Appl Phys, 1976, 9: 55

[4] Xiong S, King T J, Bokor J. A comparison study of symmetric ultrathin-body double-gate devices with metal source/drain and doped source/drain. IEEE Trans Electron Devices, 2005, 52(8): 1859.

[5] Van Dort M J, Woerlee P H, Walker A J, et al. Influence of high substrate doping levels on the threshold voltage and the mobility of deep-submicrometer MOSFETs. IEEE Trans Electron Devices, 1992, 39(4): 932

[6] Takagi S, Takayanagi-Takagi M. Accurate characterization of electron and hole inversion-layer capacitance and its impact on low voltage operation of scaled MOSFETs. IEDM Tech Dig, 1998: 619

[7] Ieong M, Solomon P M, Laux S E, et al. Comparison of raised and Schottky source-drain MOSFETs using a novel tunneling contact model. IEDM Tech Dig, 1998: 733

[8] Huang C K, Zhang W E, Yang C H. Two-dimensional numerical simulation of Schottky barrier MOSFET with channel length to 10nm. IEEE Trans Electron Devices, 1998, 45(4): 842

[9] Winstead B, Ravaioli U. Simulation of Schottky barrier MOSFETs with a coupled quantum injection/Monte Carlo technique. IEEE Trans Electron Devices, 2000, 47(6): 1241

[10] http://www.silvaco.com/silvalo manuals

[11] Mueller H H, Schulz M J. Simplified method to calculate the band bending and the subband energies in MOS capacitors. IEEE Trans Electron Devices, 1997, 44(9): 1539

[12] Janik T, Majkusiak B. Analysis of the MOS transistor based on the self-consistent solution to the Schrödinger and Poisson equations and on the local mobility model. IEEE Trans Electron Devices, 1998, 45(6): 1263

[13] Pierret R F. Semiconductor device fundamentals. Reading, MA: Addison-Wesley, 1996: 492

考虑量子效应的超薄体双栅肖特基源漏 MOSFET 电流解析模型*

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摘要：推导了超薄体双栅肖特基势垒 MOSFET 器件的漏电流模型，模型中考虑了势垒高度变化和载流子束缚效应.利用三角势垒近似求解薛定谔方程，得到的载流子密度和空间电荷密度一起用来得到量子束缚效应.由于量子束缚效应的存在，第一个子带高于导带底，这等效于禁带变宽.因此源漏端的势垒高度提高，载流子密度降低，漏电流降低.以前的模型仅考虑由于镜像力导致的肖特基势垒降低，因而不能准确表示漏电流.包含量子束缚效应的漏电流模型克服了这些缺陷.结果表明，较小的非负肖特基势垒，甚至零势垒高度，也存在隧穿电流.二维器件模拟器 Silvaco 得到的结果和模型结果吻合得很好.

关键词：肖特基势垒；量子效应；有效质量；电子密度

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