Analysis and Design of a Quadrature Down-Conversion Mixer for UHF RFID Readers*

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Abstract: A quadrature mixer with a shared transconductor stage is analyzed, including voltage conversion gain, linearity, noise figure, and image rejection. The analysis indicates it has better performance than a conventional Gilbert mixer pair in commutating mode. A quadrature down-conversion mixer based on this topology is designed and optimized for an ultra high frequency RFID reader. Operating in the 915MHz ISM band, the presented quadrature mixer measures a conversion gain of 12.5dB, an IIP3 of 10dBm, an IIP2 of 58dBm, and an SSB noise figure of 17.6dB. The chip was fabricated in a 0.18μm 1P6M RF CMOS process and consumes only 3mA of current from a 1.8V power supply.

Key words: quadrature mixer; shared transconductor stage; RFID reader; CMOS; low power; high linearity
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1 Introduction

As part of the general identification procedure, radio frequency identification (RFID) systems are becoming indispensable in manufacturing, purchasing, transportation, etc. However, almost all the RFID readers on the market today are composed of discrete devices, which lead to bad portability and high cost and, thus, are a primary obstacle to popularization. Fortunately, the remarkable development of the CMOS process enables the integration of a wireless transceiver on a single chip, which greatly reduces the volume, cost, and power consumption. In fact, the single chip reader is now a promising and hot research topic in both industry and universities.

A direct-conversion receiver for an ultra high frequency (UHF) single-chip reader based on EPCglobal Class-1 Gen-2 protocol[1] is illustrated in Fig. 1. The direct-conversion architecture is a viable solution due to its low complexity and good performance. As a key block in the receiver, the performance of the quadrature down-conversion mixer dominates the dynamic range of the whole receiver. On one hand, the linearity of the receiver front-end is limited by that of the down-conversion mixer[2], and, in the presence of adjacent channel interference from other readers, both the second-order and third-order inter-modulation of the mixer should be suppressed. On the other hand, the direct-conversion architecture requires the down-conversion mixer to be almost free of flicker noise, which is also problematic. Furthermore, power consumption and chip area are expected to be small in view of low cost.

In this paper, a quadrature down-conversion mixer with a shared transconductor stage for the UHF RFID reader application is analyzed, designed, and fabricated.

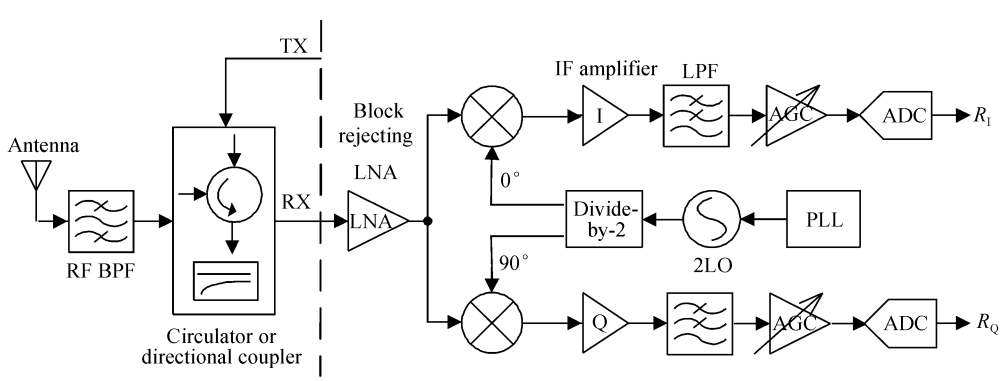

Fig. 1 A direct-conversion receiver architecture for UHF RFID reader

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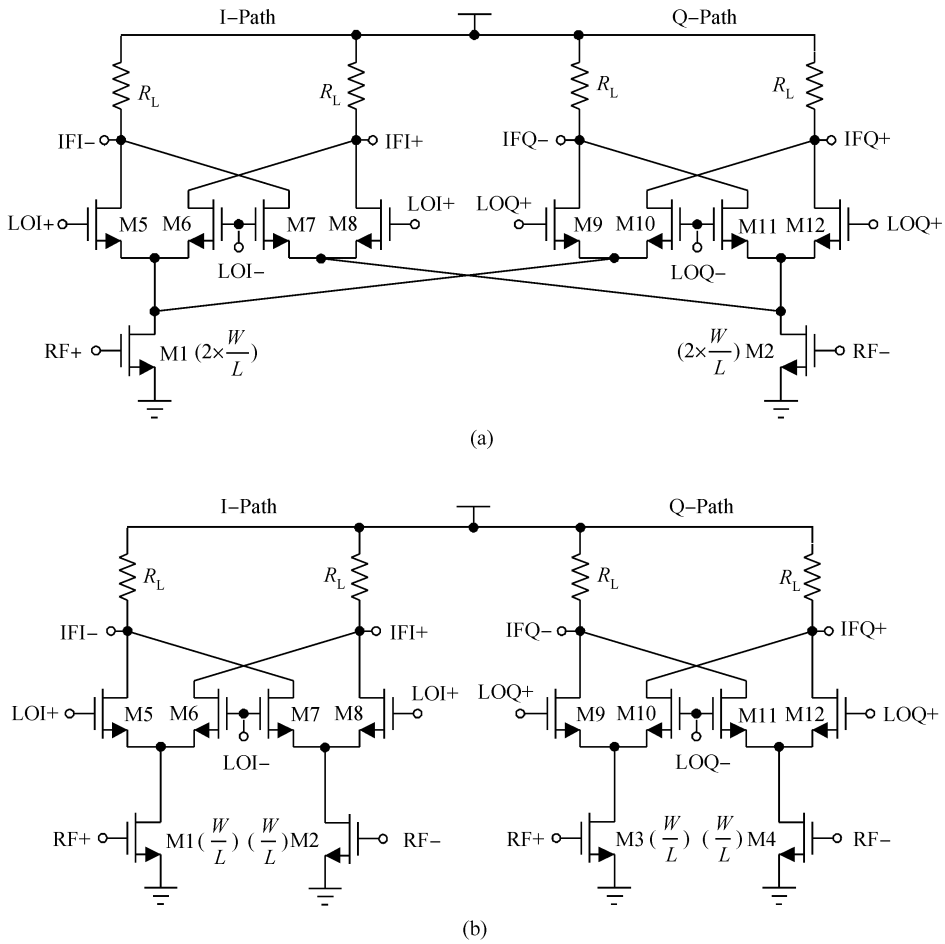

Fig. 2　Two topologies of quadrature down-conversion　(a) Quadrature mixer with shared transconductor stage; (b) Gilbert mixer pair

2　Analysis of a quadrature mixer with shared transconductor stage

Quadrature down-conversion can be realized through two topologies, as shown in Fig. 2[3], the quadrature mixer with shared transconductor stage (Q-mixer) and the conventional Gilbert mixer pair (G-mixer). To give a normalized performance analysis, the two topologies are designed to have equal power dissipation under the same bias condition. This is achieved by making the gate width of the transconductor transistors in the Q-mixer twice of that in the G-mixer, and making other parameters in switching stage and load stage identical. In addition, the mixers are assumed to operate in the commutating mode driven by a large sinusoidal local oscillator (LO) signal. This is reasonable because the LO signal offered by LC VCO is generally a large sinusoidal wave through buffering or frequency-division.

2.1　Voltage conversion gain analysis

The voltage conversion gain (CG) of a G-mixer in commutating mode is

$$\mathrm{CG_G} = g_{\mathrm{m,G}} G_{\mathrm{SW,G}} R_{\mathrm{L}} \tag{1}$$

where $g_{\mathrm{m,G}}$ and $G_{\mathrm{SW,G}}$ represent the transconductance of the transconductor transistor and the transfer gain of the switching pair in the G-mixer, respectively. The CG to each output path in a Q-mixer is

$$\mathrm{CG_Q} = g_{\mathrm{m,Q}} G_{\mathrm{SW,Q}} R_{\mathrm{L}} \tag{2}$$

where $g_{\mathrm{m,Q}}$ and $G_{\mathrm{SW,Q}}$ represent the transconductance of the transconductor transistor and the transfer gain of the switching pair in the Q-mixer, respectively. According to the biasing and size of the transconductor stage,

$$g_{\mathrm{m,Q}} = 2g_{\mathrm{m,G}} \tag{3}$$

The values of $G_{\mathrm{SW,G}}$ and $G_{\mathrm{SW,Q}}$ can be calculated from the ideal transfer waveform of the switching pair illustrated in Fig. 3. In a G-mixer, the input current available at the drain of a transconductor transistor is switched through each of the two switching transistors for half of the LO period. Therefore, the input current is multiplied by a square wave, whose Fourier series expansion is

$$f_{\mathrm{G}}(t) = \sum_{k=-\infty}^{\infty} \frac{\sin(k\pi/2)}{k\pi/2} \times \mathrm{e}^{\mathrm{j}k\omega_{\mathrm{LO}}t} \tag{4}$$

In a Q-mixer, the input current available at the drain of a transconductor transistor is switched

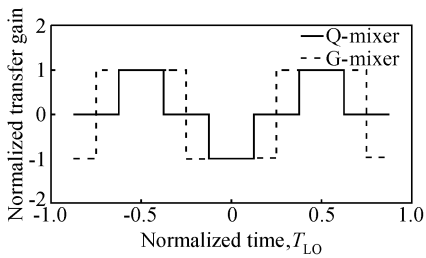

Fig. 3 Ideal transfer waveform of switching pair

through each of the four switching transistors for one quarter of the LO period. The corresponding transfer waveform has the Fourier series expansion

$$f_{\mathrm{Q}}(t) = \frac{1}{4}\sum_{k=-\infty}^{\infty}\frac{\sin(k\pi/4)}{k\pi/4}\times(1-\mathrm{e}^{-\mathrm{j}k\pi})\times\mathrm{e}^{\mathrm{j}k\omega_{\mathrm{LO}}t} \tag{5}$$

The transfer gain of switching pair equals the Fourier coefficient of the fundamental LO frequency, which means

$$G_{\mathrm{SW,G}} = 2/\pi \tag{6}$$

$$G_{\mathrm{SW,Q}} = \sqrt{2}/\pi \tag{7}$$

$$G_{\mathrm{SW,Q}} = G_{\mathrm{SW,G}}/\sqrt{2} \tag{8}$$

Combining Eqs. (1), (2), (3), and (8), we conclude that

$$\mathrm{CG_Q} = \sqrt{2}\mathrm{CG_G} \tag{9}$$

Thus, in commutating mode, the Q-mixer has a 3dB improvement in CG over the G-mixer. Figure 4 plots the simulated CG of these two topologies versus LO amplitude. In non-commutating mode, the two topologies have similar CG, but when the LO amplitude is high and the mixers are operating in the commutating mode, the CG of the Q-mixer is approximately 2.8dB greater than the G-mixer. The slight discrepancy between 2.8 and 3dB is due to the larger parasitic capacitance at the drain of the transconductor transistors.

2.2 Linearity analysis

In commutating mixers, the linearity is limited by the transconductor stage[4]. To compare the transconductor nonlinearity of the Q-mixer and G-mixer, we first analyze the nonlinearity of the common source short-channel MOSFET, whose I-V relation is[5]

$$I = K\frac{V_{\mathrm{GST}}^2}{1+\theta V_{\mathrm{GST}}} \tag{10}$$

where I is the drain current and $V_{\mathrm{GST}} = V_{\mathrm{GS}} - V_{\mathrm{T}}$ is the gate overdrive voltage. Parameter K depends on the technology and the size of the device, and is proportional to the channel width. Parameter θ models to a first order the source series resistance, the mobility degradation due to the vertical field, and the velocity saturation due to the lateral field in the short-channel. θ depends on the channel length and is independent of the body effect. The third-order input-intercept point of this MOSFET can be derived as

$$\mathrm{IIP3} = \frac{4V_{\mathrm{GST}}(2+\theta V_{\mathrm{GST}})(1+\theta V_{GST})^2}{3\theta} \tag{11}$$

According to Eq. (11), IIP3 is a monotonically increasing function of V_{GST}. The transconductor transistors of the Q-mixer and G-mixer have the same channel length and gate overdrive voltage, and therefore exhibit similar linearity.

In fact, as the Q-mixer has a larger parasitic capacitance at the drain of a transconductor transistor than the G-mixer, the nonlinearity caused by the switching pair is somewhat larger. This is because when the LO amplitude is high, higher current is injected by the parasitic capacitances, which attenuates the high-frequency phenomena and alters the periodic operating point of the devices[5]. However, because this switching pair is a minor nonlinearity contributor in commutating mixers, this linearity loss is negligible.

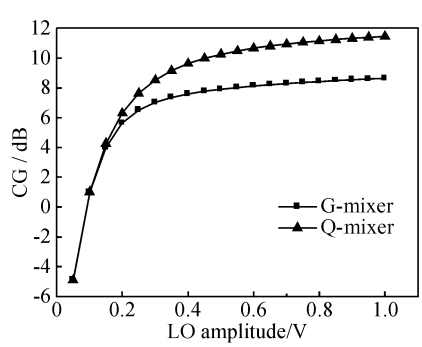

Fig. 4 Simulated CG of Q-mixer and G-mixer versus LO amplitude

2.3 Noise analysis

Output noise of the mixer derives from the load stage, switching stage, and transconductor stage, in different proportions and from different frequencies.

The loads of the mixer contribute noise in the intermediate frequency (IF). Since the loads of the Q-mixer and G-mixer are identical, the output noise due to the load stage is also the same, with power spectral density (PSD)

$$\overline{V_{\mathrm{n,Load}}^2} = 4kTR_{\mathrm{L}} \tag{12}$$

As far as the mixer is concerned, noise originating in the transconductor stage is indistinguishable from the RF input signal, so the noise at frequencies $f_{\mathrm{LO}} \pm f_{\mathrm{IF}}$, $3f_{\mathrm{LO}} \pm f_{\mathrm{IF}}$, $5f_{\mathrm{LO}} \pm f_{\mathrm{IF}}\cdots$ is down-converted to IF at output, in the same way as the input signal[6]. Thus, the transconductor stage contributes only white noise to the output noise if the switching transistors

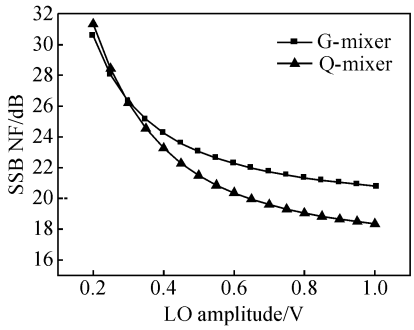

Fig. 5　Simulated SSB NF of Q-Mixer and G-Mixer versus LO amplitude

are well matched or the LO amplitude is large enough to perform ideal switching. The PSD of output noise due to the transconductor stage can be expressed as

$$\overline{V_{\mathrm{n,Transconductor}}^2} = 4kT\gamma g_{\mathrm{m}} G_{\mathrm{SW}}^2 R_{\mathrm{L}}^2 \qquad (13)$$

Equations (3), (8), and (13) indicate that the output noise due to transconductor stage is the same in the Q-mixer and G-mixer. However, because the CG of the Q-mixer is 3dB higher, the NF due to the transconductor stage and load stage is 3dB lower than that of the G-mixer.

In the switching pair, the noise at frequencies f_{IF}, $2f_{\mathrm{LO}} \pm f_{\mathrm{IF}}$, $4f_{\mathrm{LO}} \pm f_{\mathrm{IF}} \cdots$ is converted to IF at output. So the flicker noise of switching stage deteriorates the low frequency NF in direct-conversion mixers. In the G-mixer, when only one switching transistor at each transconductor transistor drain is conducting, the noise contributed to the output due to that switching transistor is negligible because it forms the cascade structure with the lower transconductor transistor. Actually, the switching stage contributes noise only when the LO signal crosses zero and two switching transistors conduct at the same time. The PSD of the output noise due to the white noise of one switch can be expressed as[6]

$$\overline{V_{\mathrm{n,Switching}}^2} = 4kT\gamma \times \frac{I}{\pi A} \times R_{\mathrm{L}}^2 \qquad (14)$$

where I is the bias current through the switching transistor and A is the LO amplitude. In a Q-mixer, noise from each switching transistor is injected into both I and Q outputs when the switching is not ideal. For example, noise of M5 is injected not only to IFI −, but also to IFQ + and IFQ −, which makes the output noise due to the switching stage in the Q-Path larger than that in a G-mixer. It is the same with the flicker noise distribution. However, according to Eq. (14), for large sinusoidal LO signals, the noise contributions of switching pairs are negligible in both the Q-mixer and G-mixer. Output noise is mainly contributed by the transconductor stage, and the Q-mixer exhibits approximately 3dB improvement in NF over the G-mixer. This analysis is validated by the plot of the simulated NF in Fig. 5. In commutating mode, the improvement of NF in the G-mixer is slightly less than 3dB because the 3dB NF advantage due to the transconductor and load stages is partially offset by the noise contribution from the switching transistors in another path. The NF increases rapidly in non-commutating mode because when the LO amplitude is lower, the flicker noise of the switching transistors begins to dominate the output noise of the mixers.

2.4　Image rejection analysis

Although the image problem does not exist in direct-conversion receivers with double side band (DSB) RF input, such as a UHF RFID reader, it is a common and severe problem in heterodyne receivers and direct-conversion receivers with single side band (SSB) RF input. The loss of image rejection derives from the device mismatch between the I and Q paths. While the influence of the load resistor mismatch on the image rejection is the same between the Q-mixer and G-mixer, the loss of image rejection introduced by transconductor stage mismatch and switching stage mismatch is different between the two topologies.

In the G-mixer, the mismatch of the transconductor stage between the I and Q paths leads to a mismatch in input impedance and transconductance. The former leads mainly to phase mismatch and the latter leads mainly to amplitude mismatch. In the Q-mixer, as the transconductor stage is shared between the I and Q paths and no image rejection loss will be introduced by a mismatch of the transconductor stage.

In the Q-mixer with non-ideal switching, more than one switching transistor at the drain of a transconductor transistor may conduct at the same time. For example, when LOI + is high and M5 is completely opened, LOQ crosses zero and M9 and M10 shall also be partially opened. The relative G_{SW} of those conducting switching transistors determines the ratio of the current routed to each output (I or Q output), which makes the matching between I/Q paths vulnerable to the mismatch in the switching stage. The G-mixer does not exhibit this routing effect because there is no interaction between the I and Q paths at the drain of the transconductor transistor.

This analysis can be verified through Fig. 6(a), which shows the simulated image rejection ratio (IRR) of the two mixers. In the IRR1 simulation, the switching stages are perfectly matched and the relative transistor gate length refers to the ratio of transconductor transistor gate length in I path to that in Q path. In the IRR2 simulation, the transconductor stages are perfectly matched and the relative transistor gate length refers to the ratio of switching tran-

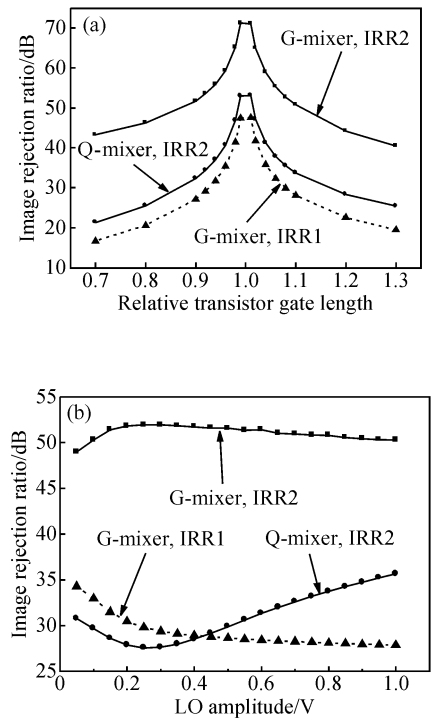

Fig. 6 (a) Simulated IRR versus relative transistor gate length, with LO amplitude of 5dBm; (b) Simulated IRR versus LO amplitude, with relative transistor gate length of 1.1

sistor gate length in the I path to that in the Q path. As expected, the IRR of the Q-mixer is immune to mismatch in the transconductor stage but more sensitive to mismatch in the switching stage. However, as the LO amplitude increases, the switching in the Q-mixer will be more ideal, and the loss of image rejection due to the switching stage will be reduced further, as shown in Fig. 6(b).

Table 1 Performance comparison of Q-mixer and G-mixer

Parameter	I_{DD} /mA	CG /dB	IIP3 /dBm	NF /dB	IRR1 /dB	IRR2 /dB	FOM /dB
Q-mixer	2.56	11.2	10.3	17.5	107	33	14.9
G-mixer	2.45	8.4	10.9	20	27	50	12.9

2.5 Summary

The simulated performances of the Q-mixer and G-mixer are summarized and compared in Table 1. The RF and LO frequency are 1.005GHz and 1GHz respectively, and the LO amplitude is 5dBm, which is a typical value in receivers. IRR1 and IRR2 are both simulated with a relative transistor gate length of 1.1. Linearity figures-of-merit (FOM) defined as $10\lg(\mathrm{OIP3(mW)}/P_{dc}\mathrm{(mW)})$ are also calculated for the two topologies, which indicates the higher performance of the Q-mixer in commutating mode.

3 Circuit design and optimization

The presented quadrature down-conversion mixer for UHF RFID readers is shown in Fig. 7. According to the analysis in Section 2, the Q-mixer topology is adopted here to consume less power while achieving the same performance as the G-mixer topology. Moreover, this topology also relaxes the design trade-offs between NF, CG, and linearity. To get high CG and low NF, higher bias current is expected in the transconductor stage, while lower bias current is preferred in the switching stage. Because previous works used current bleeding or folded structures to solve this problem, they either increased the circuit complexity

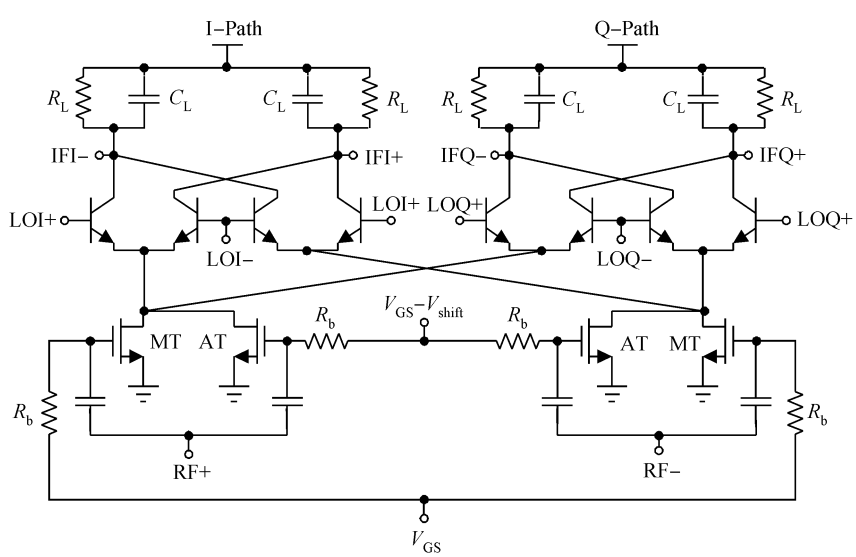

Fig. 7 Presented quadrature down-conversion mixer with shared transconductor stage

or occupied larger chip area. In the Q-mixer, the trade-off is solved inherently because the bias current in the transconductor stage is halved between the I and Q path, which enables us to optimize the transconductor stage without performance penalty in the switching stage.

In consideration of the adjacent channel interference from other readers, high linearity is required for a down-conversion mixer, and, as stated in Section 2.2, it is limited by the transconductor stage. So, the multiple gated transistor (MGTR) configuration first proposed by Kim *et al*. in Ref. [7] is adopted here, in which an auxiliary transistor (AT) operating in the sub-threshold region is superposed in parallel with the main transistor (MT) operating in the saturation region. The size and the gate bias of the MT and AT are different and carefully chosen to make the third-order inter-modulation component of the AT offset that of the MT, which gives the transconductance stage and, thus, the whole mixer a much higher IIP3. Furthermore, poly-silicon resistors are used as loads to assure linearity.

According to the noise analysis in Section 2.3, the low frequency noise is dominated by flicker noise of the switching pairs. Therefore, the parasitic vertical npn bipolar junction transistor (V-NPN BJT) in the deep n-well CMOS process, which shows a much lower corner frequency for flicker noise, is used as a switching transistor instead of MOSFET[8]. Also, the poly-silicon resistors are free of flicker noise and their resistance can be made larger to restrain the white noise contribution.

4　Chip implementation and measurements

The presented mixer was fabricated in a 0.18μm 1P6M RF CMOS process. As high frequency quadrature signals are not practical to obtain, a divide-by-two circuit is also designed and implemented to generate the quadrature LO signals. Special layout technologies, such as common-centroid, interdigitation, dummy, symmetry etc., are used to attain good matching and high IIP2. The microphotograph of the chip is shown in Fig. 8. The total die area including bonding pads is 0.85mm × 0.74mm, with 0.38mm × 0.48mm for the quadrature mixer core. The I/Q quadrature mixer including bias circuits draws a total of 3mA from a 1.8V power supply.

The RF and 2LO signals are generated by Vector Signal Generator E4438C and the output IF signals are displayed and analyzed by Oscilloscope MS08104A and Spectrum Analyzer E4440A. The down-converted

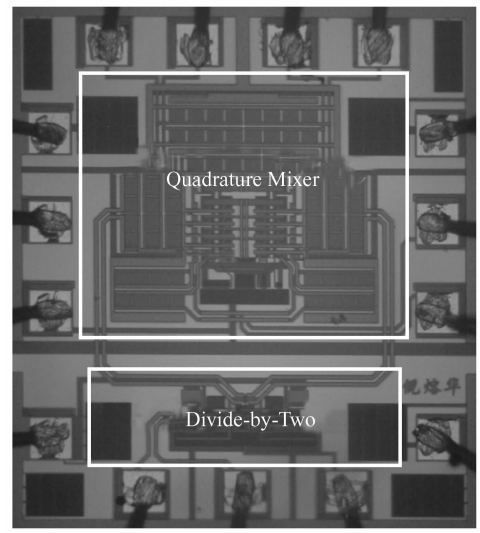

Fig. 8　Microphotograph of chip

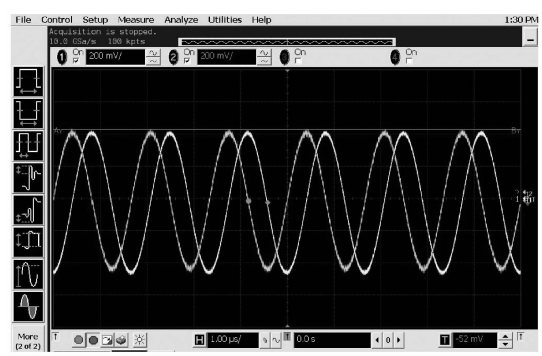

Fig. 9　I/Q output waveforms

I/Q waveforms are shown in Fig. 9, which indicates average phase error below 1.2° and amplitude error below 0.2dB, including imbalance introduced by divider, baluns, bonding, and buffers.

The measured CG is 12.5dB (IF = 500kHz), with a 1dB compression point P_{-1dB} of −5dBm, as shown in Fig. 10. The linearity is measured with a two-tone test at 915MHz LO frequency and 915.5MHz, 915.7MHz RF frequency. Figure 11 shows the output spectrum of the two-tone test. As shown in Fig. 12, the measured IIP3 and IIP2 are 10dBm and 58dBm, respectively. The SSB NF is measured 17.6dB at 1MHz,

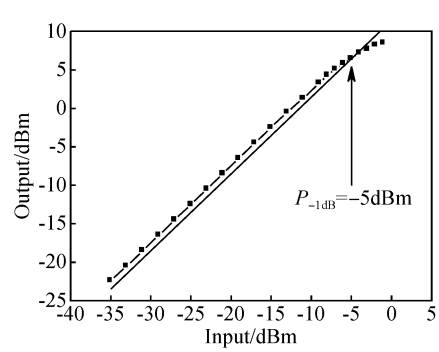

Fig. 10　Measured −1dB compression point

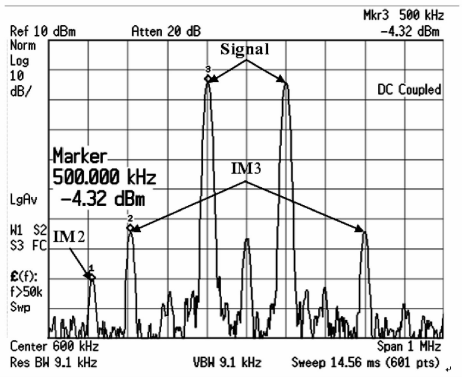

Fig. 11 Output spectrum in a two-tone test

with approximately 250kHz of corner frequency for flicker noise.

The measurement results are summarized and compared with some recently published mixers in Table 2. The presented mixer shows high linearity and low power consumption, achieving the highest linearity FOM among these mixers.

5 Conclusion

The performance of a quadrature mixer with a shared transconductor is analyzed and validated, which indicates its advantage over a conventional Gilbert mixer pair in commutating mode. A quadrature down-conversion mixer based on this topology is designed and optimized for UHF RFID reader applications. Measurement results show that the presented mixer achieves low power and high linearity without degrading other performance measures, which indicates its feasibility in low cost zero-IF or low-IF applications.

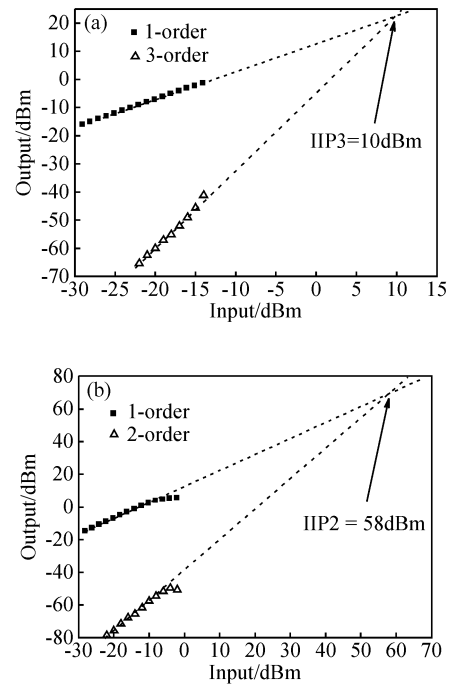

Fig. 12 Measured linearity (a) Measured IIP3; (b) Measured IIP2

Table 2 Performance summary and comparison

Reference	Kim[7]	Klumperink[9]	Vidojkovic[10]	Liu[11]	This work
Frequency/GHz	2.4	1	2.4	1.63	0.915
CG/dB	16.5	12	15.7	6.63	12.5
IIP3/dBm	9	5	1	1.5	10
SSB NF/dB	17.2	22.3	12.9	21.4	17.6
Power/mW	5.4	4	8.1	N/A	2.7
FOM/dB	18.18	10.98	7.62	N/A	18.19
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS

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一种用于超高频 RFID 阅读器的正交下变频混频器的分析与设计*

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摘要：分析了共用跨导级的正交下变频混频器的性能，包括电压转换增益、线性度、噪声系数和镜象抑制比，分析表明其在电流开关模式下比传统的 Gilbert 混频器对具有更好的性能. 设计并优化了一个基于共用跨导级结构的用于超高频 RFID 阅读器的正交下变频混频器. 在 915MHz 频段上，该混频器测得 12.5dB 的转换增益，10dBm 的 IIP3，58dBm 的 IIP2 和 17.6dB 的 SSB 噪声系数. 芯片采用 0.18μm 1P6M RF CMOS 工艺实现，在 1.8V 的电源电压下仅消耗 3mA 电流.

关键词：正交混频器；共用跨导级；RFID 阅读器；CMOS；低功耗；高线性度
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