第 29 卷　第 7 期
2008 年 7 月

半　导　体　学　报
JOURNAL OF SEMICONDUCTORS

Vol. 29　No. 7
July, 2008

High-Voltage MOSFETs in a 0. 5μm CMOS Process*

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Abstract: There is growing interest in developing high-voltage MOSFET devices that can be integrated with low-voltage CMOS digital and analog circuits. In this paper, high-voltage n- and p-type MOSFETs are fabricated in a commercial 3. 3/5V 0. 5μm n-well CMOS process without adding any process steps using n-well and p-channel stops. High current and high-voltage transistors with breakdown voltages between 23 and 35V for the nMOS transistors with different layout parameters and 19V for the pMOS transistors are achieved. This paper also presents the insulation technology and characterization results for these high-voltage devices.

Key words: high-voltage MOSFET; low-voltage MOSFET; 0. 5μm CMOS process; embedded manufacture technology
PACC: 7340L; 7340Q
CLC number: TN405　　**Document code**: A　　**Article ID**: 0253-4177(2008)07-1268-06

1 Introduction

There has been growing interest in developing high-voltage MOSFET devices that can be integrated with low-voltage CMOS digital and analog circuits[1,2]. High-voltage integrated circuits are used in a wide range of applications, such as aircrafts, automobiles, industrial robotics, medical instruments, and so on. By integrating high-voltage and low-voltage devices in the same chip, higher reliability and lower manufacturing costs can be achieved. Most high voltage integrated circuits are designed and manufactured in specially designed high-voltage processes that have optimal performance for both high-voltage devices and low-voltage devices. Features of the high-voltage process technology include epitaxial drift layers called "re-surf", self-isolation, and dielectric-isolation. Commercial use of these technologies has successfully resulted in developing high-voltage integrated circuits for smart power applications, motor control, and telecommunications[3,4]. High-voltage IC (HVIC) processes are exclusively offered by only a limited number of manufacturers and the extra steps in the HVIC process increases the manufacturing cost. Alternatively, it is possible to use a VLSI CMOS process for high voltage applications[4,5].

Several technologies have been explored for constructing high-voltage devices. Reference [6] successfully developed high-voltage nMOS and pMOS transistors in a 3μm standard p-well CMOS process. In this process, an n-guard and a p-well implant were used as the lightly doped drift regions for the high-voltage nMOS and pMOS transistors, resulting in breakdown voltages of 50V for the nMOS and 180V for the pMOS devices. Recently, high-voltage devices in a 0. 5μm BiCMOS process with breakdown voltages of 29V for the nMOSFET and 18V for the pMOSFET were also reported[7]. In BiCMOS technology, the p-well and the n-well have been used as the drift region in pMOS and nMOS devices, achieving higher-current capabilities and lower-on-resistance with the aid of the p^+ and n^+ buried layers under the p- and n-wells[8].

In this paper, high-voltage n- and p-type MOSFETs were fabricated in an IMEC 3. 3V 0. 5μm n-well CMOS process without adding any process steps. In the absence of a p-well, p^+ and n^+ buried layers, which are available only in a more complex BiCMOS process, and n-well and p-channel stops were used. We report on the experimental DC characterization of the high-voltage nMOS and pMOS devices in all regions of operation.

2 High voltage MOSFET structure

2. 1 0. 5μm CMOS n-well process considerations

The standard CMOS process used in this paper is designed by IMEC, a low-cost prototyping and small volume fabrication service for custom and semi-custom VLSI circuit development. There are 14 Masks and 17 photographs in total. This 0. 5μm n-well bulk CMOS process has singer poly triple-metal (SPTM) layers with lambda $\lambda = 0.3\mu m$, $0.6\mu m$ drawn features. The thin oxide $T_{ox} = 12.5nm$, the approximate n-well

* Project supported by the Research Program of Series Type Spectrum for Electronic Component and Device (No. 0105TJ002A)
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Received 26 December 2007, revised manuscript received 24 March 2008
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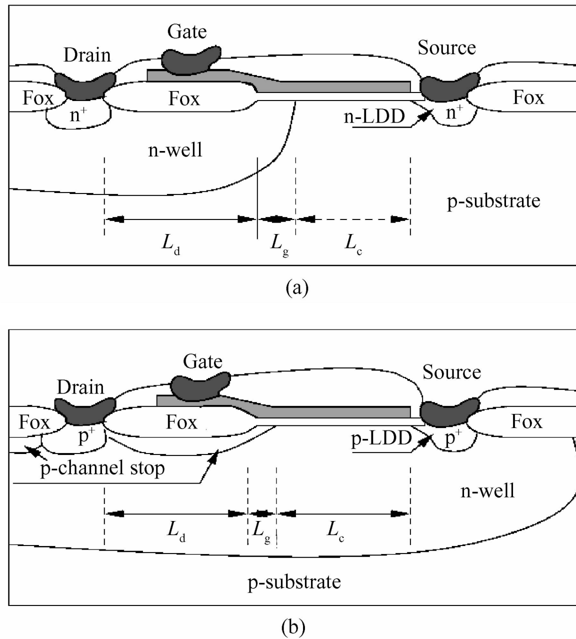

Fig.1　(a) Cross section of a high-voltage lateral diffused nMOS transistor; (b) Cross section of a high-voltage lateral diffused pMOS transistor

doping concentration is on the order of $1\times10^{17}\mathrm{cm}^{-3}$, the n^+ and p^+ doping levels are on the order of $1\times10^{20}\mathrm{cm}^{-3}$, the p-channel-stop implant concentration is on the order of $1\times10^{17}\mathrm{cm}^{-3}$, and the p-type substrate concentration is on the order of $1\times10^{15}\mathrm{cm}^{-3}$. The minimum channel length for the design rule is 0.5μm. The measured threshold voltage (V_{th}) and breakdown voltage (V_{BR}) of the standard nMOSFET and pMOSFET were $V_{tn}=0.77\mathrm{V}$, $V_{tp}=-0.93\mathrm{V}$, $BV_{dssn}=11\mathrm{V}$, $BV_{dssp}=-10\mathrm{V}$.

2.2　High voltage MOSFET structure

In a standard CMOS process, a p-channel-stop implant is used to prevent the formation of a parasitic conduction between two adjacent n^+ diffusions[9]. This implant extends under the field oxide, but a computer generated mask (p-channel-stop mask) prevents the p-channel-stop from implanting in the n-well. As a result, the p-channel stop implant can be selectively implanted into the n-well. This is a valuable and critical option because it gives users the flexibility to create lightly doped p-type regions in the n-well, which can be used to make the p-type drift section of a high-voltage pMOS transistor, as indicated in Fig.1(b).

The explicit field implant method can be implemented in any standard CMOS process without changing process steps. This method will not change the performance of the standard low voltage MOSFETs because it only changes the computer generated p-channel-stop mask. For this 0.5μm n-well CMOS process, the resulting p-type carrier concentration of the p-channel-stop is almost identical to the n-type carrier concentration of the n-well.

Table 1　Example of two sets of nMOSFET test structures

Set number	Subset number	L_g/μm	L_c/μm	L_d/μm	V_{BR}/V
Set0	Set0-1	0.3	1.5	3	34.30
	Set0-2	0.6	1.5	3	27.30
	Set0-3	0.9	1.5	3	22.54
	Set0-4	1.2	1.5	3	22.05
	Set0-5	1.5	1.5	3	21.56
Set10	Set10-1	0.3	6	9	32.55
	Set10-2	0.6	6	9	27.60
	Set10-3	0.9	6	9	24.25
	Set10-4	1.2	6	9	22.50
	Set10-5	1.5	6	9	21.25

3　Design and characterization of the high voltage nMOS devices

3.1　High-voltage nMOSFET test structures

High voltage nMOS devices with different channel lengths (L_c), n-well channel overlaps (L_g), and drift regions (L_d) were fabricated through a CMOS process. Table 1 lists part of the test structures with different layout parameters and tested breakdown voltages.

3.2　nMOSFET breakdown voltage variations

This 0.5μm CMOS process was designed for high-speed digital VLSI applications. As a result, this process has design limitations such as low junction breakdown and a very thin gate oxide for high-voltage applications. The estimated n-well-to-substrate breakdown voltage, which is the maximum breakdown voltage of all p-n junctions in a standard CMOS process, can be calculated by Eq.(1).

$$V_{BR}=\frac{\varepsilon(N_A+N_D)}{2qN_AN_D}E_{crit}^2 \tag{1}$$

where N_D is the carrier concentration of the n-well, N_A is the carrier concentration at the surface of the p-type substrate, ε is the permittivity of the silicon (1.04×10^{-12} F/cm), and E_{crit} is the required critical electric field for creating an avalanche process. The magnitude of E_{crit} is in the range $10^5\sim10^6$ V/cm with n-p junction doping densities from $10^{15}\sim10^{18}\mathrm{cm}^{-3}$. The calculated breakdown voltage (36V) was close to the measured n-well to the substrate breakdown voltage (33V). The n-well is used as the drift region for the high voltage nMOSFET drain, which is biased at a high voltage. Thus, the breakdown voltage of the n-well to the substrate sets the maximum voltage, which can be supplied at the drain of the high-voltage nMOSFET.

Measurement results indicate that the n-well to

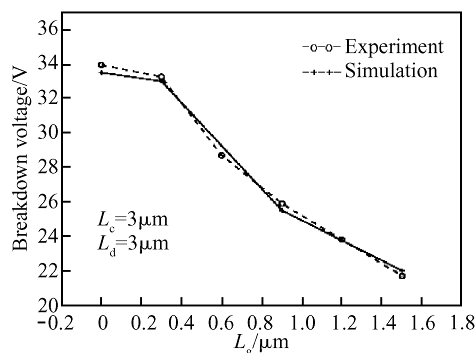

Fig. 2 Breakdown voltage variations based on the difference in L_g

channel overlap (L_g) has a significant effect on the breakdown voltage, as shown in Fig. 2. The variation in breakdown voltages (V_{BR}) from 23 to 35V was measured for L_g between 0.3 and 1.5μm. These experimental results confirm the simulation results and the breakdown analysis of the high-voltage nMOSFET, demonstrating a 12V increase in V_{BR} as L_g is reduced.

The effect of the drift region's length (L_d) on the nMOS device's breakdown is investigated on a set of nMOS transistors with different drift region lengths of 3.0, 6.0, 9.0, and 12.0μm. The breakdown voltages change only ±1V for these devices. This negligible variation in breakdown is attributed to the highly doped drift region ($1\times10^{17}cm^{-3}$). Thus, no significant voltage drop across the drift region could be achieved nor would any further increase in the drift region length have resulted in an increase in the breakdown voltage. A high voltage transistor's electric field in the drift region can be evenly distributed to increase the junction breakdown voltage if the concentration and depth of the drift region is carefully designed. Thus, the breakdown voltage is set by the natural p-n junction characteristics of the n-well to substrate junction. The maximum breakdown voltage with layout parameters (L_g = 0.3μm, L_d = 3.0μm, L_c = 1.5μm) is 34V compared to the measured n-well-to-substrate junction breakdown voltage of 33V. However, this device exhibits unusual characteristics in that there is no saturation region. Similar characteristics can be found for all nMOSFET devices with L_g = 0.3μm (Fig. 3). A device with optimum layout parameters (L_g = 1.2μm, L_d = 3.0μm, L_c = 1.5μm) and standard nMOSFET characteristics gives a 22V drain breakdown voltage for V_{gs} = 0V. This transistor exhibits the same V_t as that of the low-voltage nMOS device, which has a measured breakdown voltage of 11V. However, this high-voltage nMOS transistor breakdown voltage is lower than that of the n-well to substrate junction due to the high p-type surface concentration in the channel.

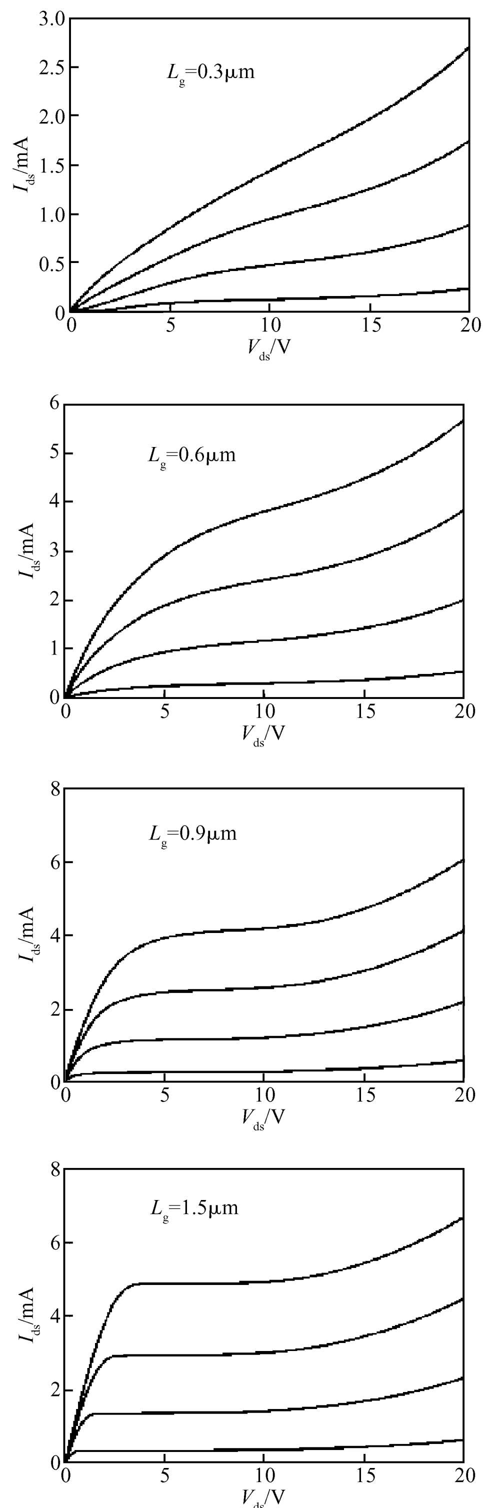

Fig. 3 Experimental results of I_{ds} versus V_{ds} characteristics

Circular geometries were used in the high-voltage device to limit edge effects. In order to evaluate these effects in the 0.5μm process, additional square-shaped high-voltage transistors were fabricated. These devices have the same layout parameters as the circular devices. The measured breakdown voltage (19V) for a square-shaped nMOS devices is about 3V lower than the breakdown voltage (21.56V) of high-voltage

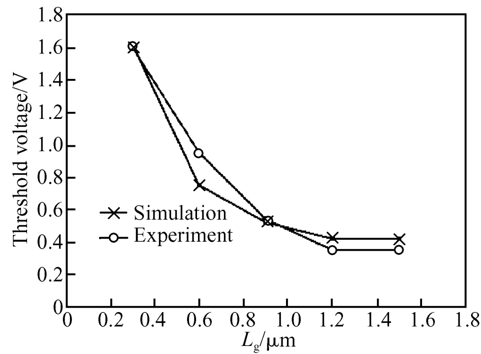

Fig.4 Experimental threshold variation based on L_g V_{ds} = 0.1V

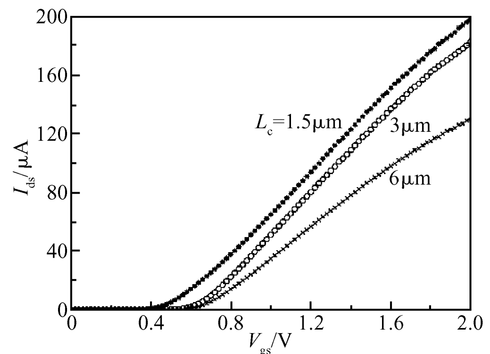

Fig.5 Effect of the channel length on the threshold voltage

nMOS device with comparable layout parameters (L_g = 1.5μm, L_d = 3.0μm, L_c = 1.5μm) and circular geometries. This experimental result indicates that the effect of an edge induced junction breakdown is weak in this 0.5μm CMOS process.

3.3 nMOSFET threshold voltage variations

Figure 4 shows the change in threshold voltage (V_t) as a function of the overlap distance (L_g) with a channel length of 6μm. A threshold voltage increase from 0.41 to 1.6V is caused by the interaction of the "bird's beak" with the edge of the n-well drift region. The n-well channel overlap has to extend beyond the edge of the "bird's beak" into the active region to create a continuous channel between the drain and the source. If the n-well ends closer to the "bird's beak" region, the nMOS device will require either a larger gate voltage for creating an inversion layer at the corner of the "bird's beak" or a larger drain bias voltage to increase the depletion region width in order to reach the channel. This phenomenon limits the performance of the high-voltage nMOSFET. The large threshold voltage will drive the device out of saturation. At the same time, further increases of the gate voltage will cause the gate oxide to breakdown. In particular, when L_g = 0, it takes more than 3V to turn on the transistors.

On the other hand, the high-voltage nMOS device exhibits low-threshold characteristics with a L_g larger than 1.2μm and L_c less than 1.5μm. Figure 5 shows the threshold voltage dependence on channel length (L_c) with fixed L_g = 1.2μm, indicating that the shorter the channel length, the lower the threshold voltage. Explanations for this phenomenon can be found in Ref.[9]. In order to achieve a compatible V_t between a high-voltage nMOSFET and a low-voltage nMOSFET, the minimum L_g and L_c should be larger than 0.9 and 3μm, respectively, setting the breakdown voltage at 22V.

3.4 nMOSFET on-state I_d versus V_{ds} characteristics

The current voltage characteristics of the high voltage nMOSFET with a V_{ds} of up to 20V and different values of L_g are shown in Fig.3. As L_g decreases, the transistors can not easily operate in the saturation region. The experimental results verify the device simulation results. An nMOSFET with L_g = 1.2μm, L_c = 1.5μm, L_d = 3μm was made to test the device performance. This device has the smallest geometric size for a circular high voltage nMOSFET structure that can be made according to the existing IMEC 0.5μm CMOS layout design rules.

3.5 Other nMOSFET characteristics

Punch-through between the drain and source is also an important consideration when laying out high-voltage nMOS transistors. As large voltages are applied to the drain of the high voltage transistor, the depletion region of the drain junction will extend under the gate region. Punch-through current will begin to flow when the drain's depletion region reaches the source junction. The depletion region width can be estimated by

$$W_1 = \left[\frac{2\varepsilon(\Psi_0 + V_R)}{2qN_A\left(1 + \frac{N_A}{N_D}\right)}\right]^{1/2} \quad (2)$$

Where N_A and N_D are the carrier concentrations for the p-type substrate and the n-well, respectively, q is the electron charge (1.6×10^{-19} coulomb), ε is the permittivity of the silicon (1.04×10^{-12} F/cm), $\Psi_0 = V_T \times \ln \frac{N_A N_D}{n_i^2}$ is the junction built-in potential, and n_i is the intrinsic carrier concentration. The estimated depletion width into the channel region is about 0.6μm with a 25V drain reverse bias. Thus, it is not possible to construct a high-voltage nMOS device with a minimum channel length that operates at a drain bias voltage above 25V. In order for the high-voltage transistors to operate optimally, punch-through must occur at a voltage greater than the avalanche break-

down of the drain junction. The punch-through voltage directly depends on the concentration of the substrate and the drift region. To avoid punch-through, the transistor channel length has to be increased. Experimental results show that for high-voltage nMOS transistors with a channel length (L_c) less than 1.5μm and the gate biased at 0V, I_{ds} increases rapidly with the drain bias. When the channel length is greater than 1.5μm, the drain-to-source current increases rapidly only when the junction reaches avalanche breakdown.

4 Characterization of the high-voltage pMOS devices

4.1 Structure of the high-voltage pMOS devices

The high-voltage pMOS devices were fabricated using a p-channel stop implant as the drift region in the n-well. Compared to the n-well drift region of the high-voltage nMOSFET, the p-channel stop implant is very shallow (about 0.1~0.3μm). Also, the p-channel stop implant doping concentration is compensated by the heavily doped n-well, resulting in a net doping concentration that is significantly lower than the original p-channel stop implant doping level. As a result, the high-voltage pMOS transistor has a high-series on-resistance in the drain area.

4.2 pMOSFET breakdown voltage variation

Our experimental results show that the breakdown voltage has a weak dependence on the length of the drift region. According to simulation results, the maximum electric field occurs at the corner of the p^+ drain junction rather than at the end of the drift channel. As a result, high voltage pMOS devices can be built with the minimum feature dimensions permissible by the process design rules. The maximum breakdown voltage achieved is 19V compared to 9V in the case of the low-voltage pMOS device.

4.3 pMOSFET current versus voltage characteristics

The high-voltage pMOSFET I_{ds}-V_{gs} characteristics in the linear region are shown in Fig. 6, where V_{ds} is set to -0.1V while sweeping the gate voltage from 0 to -2V. The I_{ds}-V_{gs} characteristics show that the p-channel stop implant drift region introduces a very high on-resistance. At a low drain current level, the voltage drop in the drift region is small and the current increases linearly with the gate bias. However, at a large drain current, the voltage drop across the drain resistance becomes significant, reducing the effective voltage drop across the channel. Thus the characteristics are dominated by the effective series resistance of the drift-region. This causes a change in the slope of the I_{ds} versus V_{gs} curve. The device I_{ds}-V_{ds} characteristics with a V_{ds} of up to -15V is shown in Fig. 7

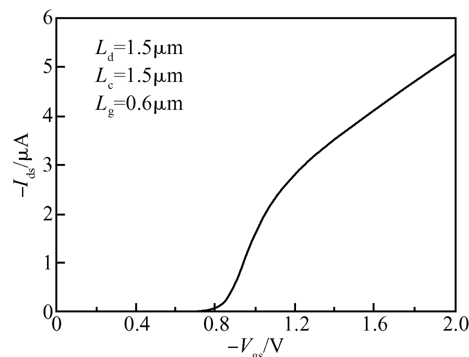

Fig. 6 Experimental results of the high-voltage pMOSFET linear region $V_{ds}=-0.1$V

5 Conclusion

The characteristics of high-voltage nMOS and pMOS transistors compatible with the standard 0.5μm CMOS process offered through MOSIS have been described. The detailed design procedures, which include 2D device simulations for high-voltage nMOS and pMOS transistors, are also presented. High-voltage nMOS and pMOS transistors with a threshold voltage similar to the low-voltage transistors and with high breakdown voltages were successfully produced. The experimental maximum avalanche breakdown voltages are 34V for the high voltage nMOS devices and 19V for the high-voltage pMOS devices. The simulations show a 2.0V maximum potential difference between the gate and the body of the high-voltage MOSFETs with the drain junction biased at the avalanche breakdown voltage. With the proper guard band structure, it is also possible to eliminate any cross talk

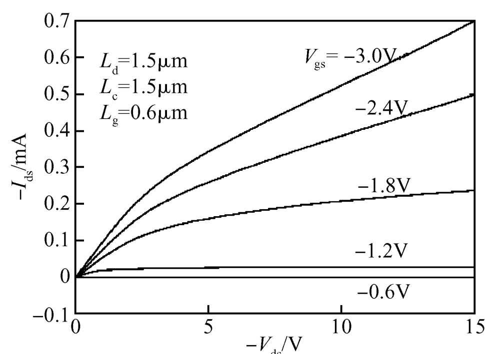

Fig. 7 On-state I-V characteristics with optimized layout parameters

between two junctions due to the presence of high-voltage potentials. Thus, high voltage MOSFETs can operate as reliably as low-voltage transistors in a mixed-signal design. These experimental data prove that it is possible to build custom transistors with a wide range of breakdown voltages without altering the manufacturing process for standard 0.5μm CMOS technology.

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基于 0.5μm CMOS 工艺的高压器件*

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摘要： 近年来，驱动类、音响类、接口类电路产品系列是 CMOS 集成电路发展的一个重要方向，这些电路中特有的高低压兼容结构是其重要的特点.相应地高低压兼容 CMOS 工艺技术应用也越来越广泛.本文研究了与常规 CMOS 工艺兼容的高压器件的结构与特性，在结构设计和工艺上做了大量的分析和实验，利用 n-well 和 n 管场注作漂移区，在没有增加任何工艺步骤的情况下，成功地将高压 nMOS，pMOS 器件嵌入在商用 3.3/5V 0.5μm n-well CMOS 工艺中.测试结果表明，高压大电流的 nMOS 管 BV_{dssn} 达到 23～25V，p 管击穿 BV_{dssp}＞19V.

关键词： 高压 MOS 器件；低压 MOS 器件；0.5μm CMOS 工艺；工艺兼容技术

PACC： 7340L；7340Q

中图分类号： TN405　　**文献标识码：** A　　**文章编号：** 0253-4177(2008)07-1268-06

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* 电子元器件型谱系列科研资助项目(批准号：0105TJ002A)

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2007-12-26 收到，2008-03-24 定稿

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