A Novel 4/5 Prescaler with Automatic Power Down*

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Abstract: An "automatic power down" method is introduced to design a 4/5 prescaler, with the characteristic of making one of its D-flip-flops power down when it operates in divide-by-4 mode. Implemented with the TSMC 0.25μm mixed-signal CMOS process, the 4/5 MOS current mode logic prescaler is designed with this automatic power down technique. The simulation results show that the new 4/5 prescaler is immune to the "wake-up" issue and thereby retains the same maximum operating frequency as the conventional prescaler. An integer-N divider with this proposed prescaler and with the division ratio 66/67 is manufactured, and it is estimated to save more than 20% of the power compared with the conventional 4/5 prescaler.

Key words: MCML prescaler; automatic power down; frequency synthesizer
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1 Introduction

In the design of an integer-N frequency synthesizer, a dual-modulus prescaler is required to provide two consecutive dividing ratios. This is a key component for integrated radio frequency transceiver design in terms of maximum operating frequency and power consumption[1]. Several CMOS high-speed dual-modulus prescalers, including true single phase clocking (TSPC) and MOS current mode logic (MCML) architecture have been reported[2~5]. Those reports pay much importance to improving the speed and power efficiency at the transistor circuit level; However, little attention was paid to optimizing the overall dual-modulus architecture. In this report, we present a method to reduce the MCML 4/5 prescaler's power consumption, with the characteristic of making one of its third D-flip-flop automatically power down when it operates in divide-by-4 mode. Simulation and measured results are reported to verify the expected performance.

2 General considerations

The dual-modulus prescaler is one of the most power-hungry components and may consume more than 40% of the power in the overall frequency synthesizer[6,7]. The conventional high-speed 4/5 prescaler is generally composed of three synchronous D-flip-flops, as shown in Ref. [6]. Operation analysis reveals that when the modulus-control signal (MC) is at the low level, the output frequency (f_{out}) is determined by the loop over the first two D-flip-flops and equals one-fourth of the input frequency. At this operation mode, the third D-flip-flop has no contribution to the output frequency but it offers a high-level signal to the former NAND gate. This high-level signal can be provided by other components rather than a power-hungry D-flip-flop. In order to achieve this, a novel 4/5 prescaler topology with an added OR gate and an inverter is proposed, as shown in Fig. 1. In the new topology, when the MC is at the low level, the prescaler still operates in divide-by-4 mode, but the third D-flip-flop is powered down by an nMOS named N1 whose gate voltage is set to zero. In order to keep all the D-flip-flops at the same DC operating points, two additional nMOS transistors are connected between the ground and the first two D-flip-flops, respectively. When it operates in divide-by-5 mode, the third D-

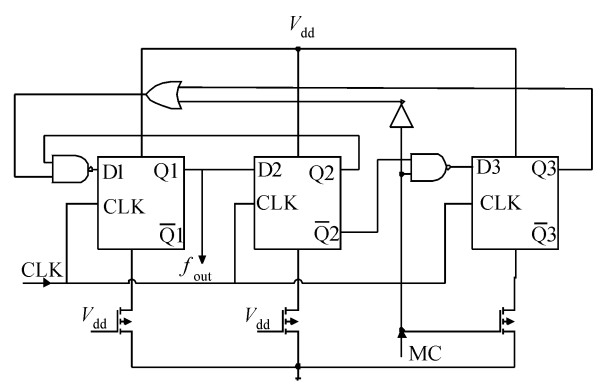

Fig. 1 Novel 4/5 prescaler with automatic power down

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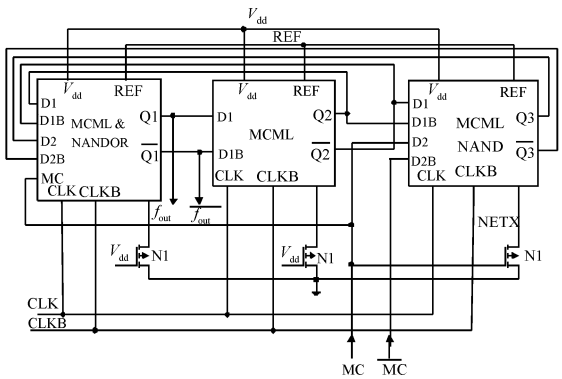

Fig. 2 Proposed 4/5 prescaler implemented with MCML

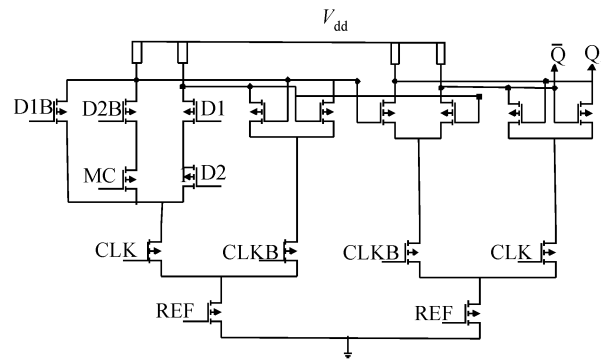

Fig. 3 Improved MCML D-flip-flop

flip-flop is active and the prescaler works as a conventional one. The MC of the dual-modulus prescaler is reused as the enable-signal to make the third D-flip-flop active or inactive. Therefore, unlike the conventional power down mode, dividers with this proposed prescaler do not need an external enable-signal, so this technique is called "automatic power down".

When this proposed 4/5 prescaler is applied to an integer-N divider, providing the division ration: $M = 5A + 4(N - A)$, the percentage of the power consumption saved (PS) by the 4/5 prescaler can be expressed as:

$$\mathrm{PS} = \frac{N - A}{3 \times [5A + 4(N - A)]} \times 100\% = 400\% \Big/ 3\left(4 + 1.25\,\frac{A}{N - A}\right) \quad (1)$$

where A, N are the values of the swallow and the programmable counter, respectively.

3 Proposed topology

A drawback of the above MCML 4/5 prescaler is that an OR gate is added in the critical feedback loop, which causes an additional delay and reduces the prescaler's maximum operation frequency. To overcome this limitation, the embedded technique, which is widely used to increase the maximum frequency[4,6], is applied to this MCML 4/5 prescaler. The conventional MCML 4/5 prescaler architecture and its operating mechanism can be found in Ref. [6] in detail, in which the NAND gate has already been embedded. Figure 2 is the full schematic of the proposal MCML 4/5 prescaler.

In order to embed the OR gate in Fig. 2, the first D-flip-flop is revised a little from the traditional one, as shown in Fig. 3. An additional transistor named MC is inserted, which cooperates with transistor D2B to replace the OR gate. Since the MC is differential, unlike that in Fig. 1, the inverter is unnecessary.

4 Experimental results

When the proposed prescaler switches from divide-by-4 to divide-by-5, the third D-flip-flop is in "sleep" mode. Since the prescaler usually operates in very high frequency, the third D-flip-flop should wake up quickly. In order to investigate the influence of the proposed architecture on the maximum operating frequency, a conventional MCML 4/5 prescaler is designed and implemented with a TSMC 0.25μm mixed-signal CMOS process. The size of this prescaler is optimized according to Ref. [8] to achieve the available maximum operating frequency with less power consumption. The proposed MCML 4/5 prescaler is also designed with the identical transistor sizes. In order to keep the same DC operating point for both the conventional and proposed prescaler, the switch transistors N1 have a rather larger periphery, as shown in Fig. 2.

This conventional MCML 4/5 prescaler consumes 3.3mA current with a maximum operating frequency of 8.0GHz under a power supply of 2.5V. This novel prescaler also consumes 3.3mA current in divide-by-5 mode, while consuming only 2.2mA current in divide-by-4 mode. Figure 4 shows the transient response of

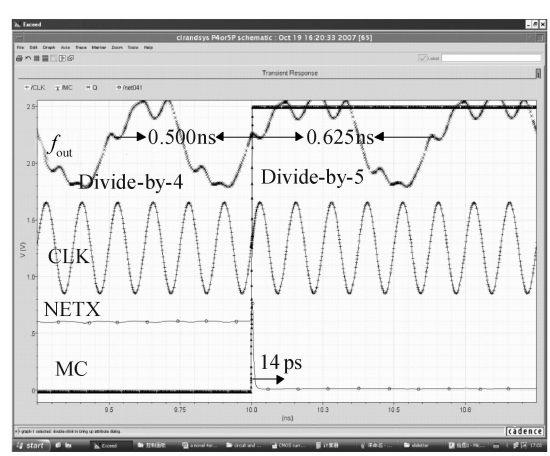

Fig. 4 Simulation of the proposed 4/5 prescaler at 8GHz

Fig. 5　Die photo of the proposed prescaler and its buffer

the proposed prescaler. At a frequency of 8.0GHz, when the MC signal is rising, the prescaler changes into divide-by-5 mode immediately. As indicated in Fig. 4, the NETX achieves a proper DC operating point within 14ps, from which it can be inferred that the wake-up time of the third D-flip-flop is very short. Therefore, the prescaler's maximum operating frequency is also 8.0GHz, which shows that the proposed architecture does no harm to the maximum operating frequency.

The above novel prescaler was applied to an integer-N divider with a division ratio of 66/67 and this integer-N divider was manufactured. Figure 5 is the die photo of the proposed prescaler and its buffer that is usually attached in the MCML frequency divider as a level-shifter. Its area is about $180\mu m \times 110\mu m$. From Eq. (1), in order to reduce the power consumption, the proposed prescaler should operate in the divide-by-4 mode as long as possible, which minimizes $A/(N-A)$. In order to achieve this goal, the values of the A, N must be 2, 16 for division ratio 66 and 3, 16 for division ratio 67, respectively. To measure the current's variety of the prescaler, a resistor is connected between the power supply line and the prescaler, and the current is achieved through dividing the measured voltage by the resistor. The currents' variabilities against time with division ratios 66/67 are shown in Fig. 6, where the input frequency of the CLK is 2.5GHz. In Fig. 6, at divide-by-4 mode, the prescaler consumes about 2.35mA of current, while consuming about 3.55mA in divide-by-5. From Eq. (1), compared

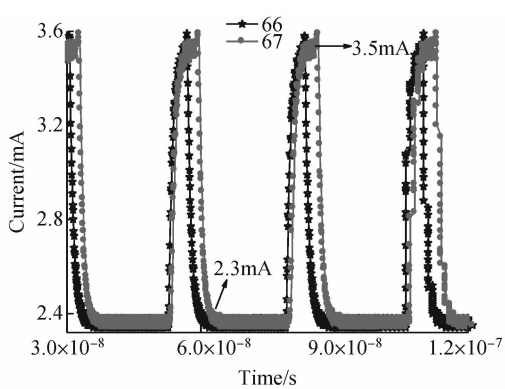

Fig. 6　Proposed prescaler consumed current varieties against time

with the conventional prescaler, the power reduction of this one is estimated to be 28.7% for division ratio 66 and 21.5% for the division ratio 67, respectively. The maximum operating frequency of the divider is about 3.2GHz, which is less than the simulation results mainly due to its successive buffer.

5　Conclusion

A method is presented in this report to reduce the MCML 4/5 prescaler's power consumption, with its characteristic of making one of its three D-flip-flops automatically power down when it operates in divide-by-4 mode. This technique can also be applied to various dual-modulus prescalers, such as the 2/3 TSPC prescaler, and the 8/9 and 16/17 MCML prescalers. The method to eliminate the influence to the maximum operating frequency due to the automatic power down architecture is discussed in detail. This simulation results show that the proposed MCML 4/5 prescalers is immune to the "wake-up" issue and retains the same maximum operating frequency as the conventional prescaler. A divider with this novel prescaler is manufactured and it is capable of saving more than 20% of the power compared with the conventional 4/5 prescaler.

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一种具有自适应节能的新型 4/5 高速双模预分频器*

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摘要：首次提出一种自适应节能方法用于设计 4/5 高速双模预分频器，它的特点是工作在除 4 模式时，其中一个 D 类触发器处于休眠状态. 使用台积电混合信号 0.25μm CMOS 工艺，采用这一自适应节能的设计方法，设计了一个具有源极耦合结构的 4/5 高速双模预分频器. 仿真结果证明，这一新型 4/5 高速双模预分频器不受休眠到工作转换状态的影响，最高工作频率保持不变. 同时，流片结果表明，当这一新型高速预分频器用于实现 66/67 分频时，可节省高达 20%以上的功耗.

关键词：MCML 预分频器；自适应节能；频率合成器

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