A Σ-Δ Fractional-*N* PLL Frequency Synthesizer with AFC for SRD Applications

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Abstract: A fractional-*N* frequency synthesizer for 433/868MHz SRD applications is implemented in a 0.35μm CMOS process. A wide-band VCO and an AFC are used to cover the desired bands. A 3bit third order sigma-delta modulator is adopted to reduce the out-band phase noise. The measurements show a VCO tuning range from 1.31 to 1.88GHz with AFC working correctly, an out-band phase noise of −139dBc/Hz at 3MHz offset frequency, and a fractional spur of less than −60dBc. The chip area is 1.5mm×1.2mm and the total current dissipation including LO buffers is 19mA from a single 3.0V supply voltage.

Key words: short range device; phase locked loop; adaptive frequency calibration; frequency synthesizer; sigma-delta
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1 Introduction

Relying on the advantages of low power, small bandwidth, and occupation of unlicensed industrial, scientific and medical (ISM) bands, short range devices (SRD) have been widely used in systems such as radio frequency identification (RFID), automatic meter reading (AMR) systems, and wireless interphones. Frequency synthesizers are among the most critical parts in SRDs. Nowadays, sigma-delta fractional-*N* PLL frequency synthesizers have proved to have overwhelming advantages over their integer counterparts in terms of lock time, reference spur, and phase noise[1,2]. In many cases, a voltage controlled oscillator (VCO) with a wide tuning range is implemented in PLL to cover the desired frequency bands and to compensate the process, voltage, and temperature (PVT) variations. In addition, the tuning gain of VCO is further increased to accommodate the scaling down of the supply voltage. A combination of digital and analog tuning mechanisms that can decrease the tuning gain of VCO and, hence, the PLL phase noise, has been reported[3]. As a result, various VCO frequency calibration techniques have been proposed to select the optimum sub-band automatically[3,4]. This work presents a sigma-delta fractional-*N* PLL frequency synthesizer with a wide-band fully integrated VCO and an adaptive frequency calibration (AFC) in 0.35μm CMOS technology. The test results show that the proposed PLL meets the requirements of 433/868MHz SRD bands, which are summarized in Table 1.

2 System level design considerations

Figure 1 illustrates the block diagram of the proposed frequency synthesizer. It consists of a crystal oscillator (XOSC), a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), a VCO, two divide-by-two circuits (DTC), a prescaler, an AM counter, a sigma-delta modulator (SDM), an AFC block, and a digital control block. All the blocks except the LPF are integrated on-chip, and the digital parts in the dashed lines in Fig. 1 are digitally synthesized.

The main PLL loop is a typical multiple frequency structure, where the DTC can easily provide quadrature I/Q LO signals for both the transmitter and receiver. Moreover, a DTC can improve the phase noise by 6dB. As a result, a wide band VCO is needed to cover the desired bands and to compensate the PVT variations mentioned above. An AFC block is included in the PLL to adaptively choose wanted sub-bands of VCO. At the beginning of operation, sw1 is turned off while sw2 is turned on. When the AFC starts to choose the wanted sub-band of VCO, sw1 will turn on and sw2 will turn off automatically after calibration

Table 1 PLL specifications for 433/868MHz SRD

Frequency band	433MHz, 868MHz
Channel spacing	12.5kHz (433MHz), 25kHz (868MHz)
Phase noise	−80dBc/Hz @ 12.5kHz −105dBc/Hz @ 100kHz
Spurious tone	< −40dBc
Lock time	<640μs

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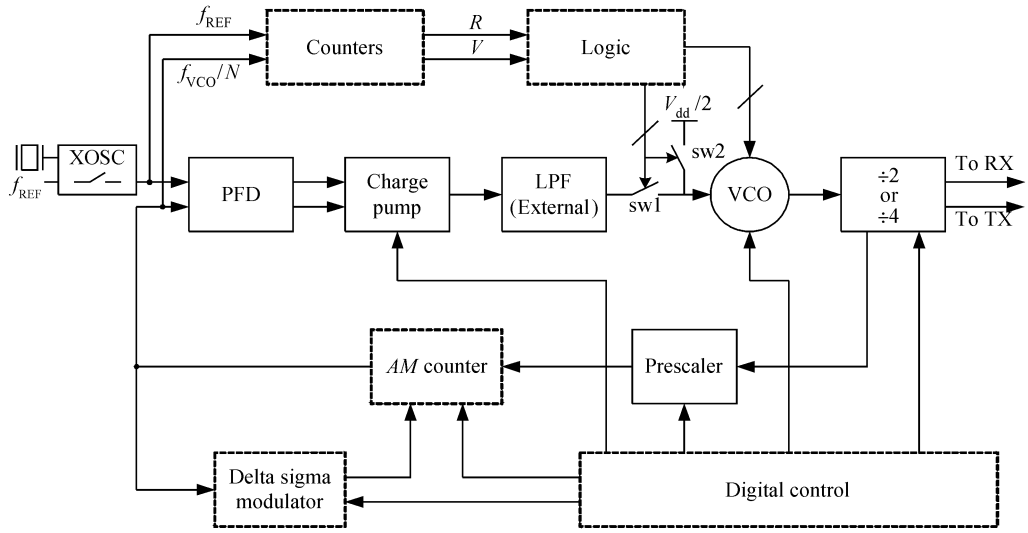

Fig. 1　Frequency synthesizer block diagram

finishes. Consequently, PLL will enter its locking operation.

The required PLL lock time is 640μs according to typical SRD applications. To leave some margin, the lock time is set to 500μs. A simplified equation for estimating the loop bandwidth is[5]:

$$T_L = \frac{4}{f_c} \tag{1}$$

So the loop bandwidth is 8kHz according to Eq. (1). Considering the external LPF implementation, the loop bandwidth can be adjusted by varying the values of R and C together with the current of CP while ensuring a phase margin of over 50° to guarantee the stability of the PLL. As indicated in the linear phase noise model of the CP PLL[6], the in-band noise will deteriorate while the out-band noise will improve when the loop bandwidth decreases. So a tradeoff between in-band and out-band noise has to be considered when choosing the loop bandwidth.

3　Circuit implementations

3.1　AFC

The required PLL turn-on time is 2～3ms according to typical SRD applications, so the time budget is enough for the calibration. As a result, due to the high area-efficiency of fully-digital implementation, the counter based AFC[4] is adopted in this design despite its long counts for the cancellation of the uncertainty of the initial phase difference of the two inputs of reference and divided VCO signal. The AFC block diagram is depicted in the upper part of Fig. 1. It is made up of two counters and a logic unit which consists of a data comparator and a state machine. The count numbers (R, V) of the two counters represent the frequencies of the two inputs. Then the count numbers are fed into the data comparator, whose results will induce the state machine to change the control bits of the digitally controlled capacitor array (DCCA) of the VCO. The state machine uses the binary search algorithm[4] to shorten the calibration time. In addition, the control voltage of the VCO is set to $V_{dd}/2$ in the calibration mode to ensure the linear transfer characteristic of the tuning curves of the VCO has good phase noise performance. The control signals of the switches (sw1, sw2) are generated by the logic unit in Fig. 1.

3.2　VCO

A complementary cross-coupled LC VCO is implemented in this design regarding the voltage headroom and its better phase noise performance compared to its single cross-coupled counterpart[7]. Figure 2 shows the schematic of VCO. According to the specifications, the VCO should cover the frequency range of 1.608～1.880GHz, so the LC tank consists of two varactors, a 5bit DCCA, and an on-chip differential inductor. An inversion-mode varactor is used instead of an accumulation-mode varactor due to process limitations. The quality factor Q of the inversion-mode varactor can be expressed as:

$$Q_{var} = \left(\omega C_{var}\left(\frac{L}{W\mu C_{ox}(V_{gs} - V_{th})} + \frac{W}{F^2 L}R_{G\_squa}\right)\right)^{-1} \tag{2}$$

where R_{G_squa} is the sheet resistance of the gate resistor and F is the number of the transistor fingers. The first half of the expression in the second bracket of Eq. (2) is the channel resistance, while the remaining half is the gate resistance. By setting the two resistances equal, an optimized Q can be given:

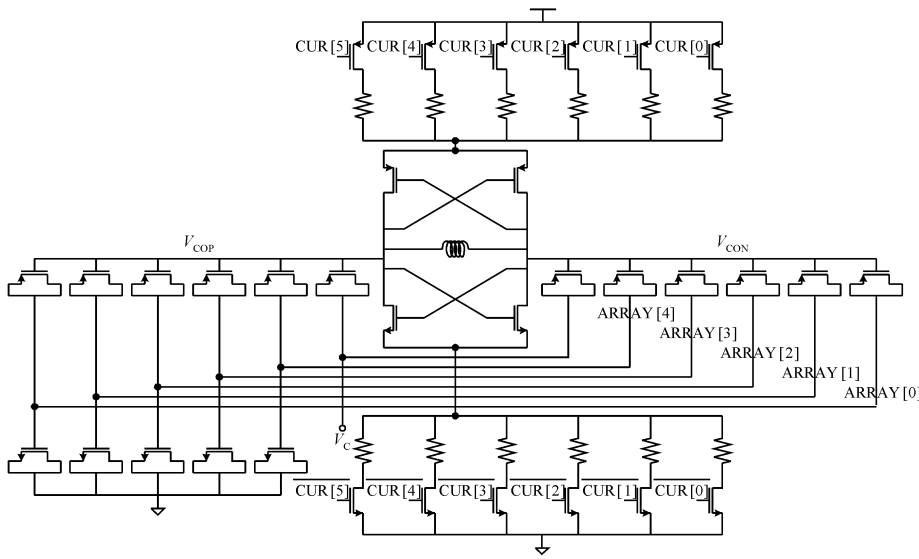

Fig. 2 Schematic of VCO

$$Q_{\text{var\_opt}} = \frac{F}{2\omega C_{\text{var}}}\sqrt{\frac{\mu C_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})}{R_{\text{G\_squa}}}} \tag{3}$$

As long as the channel resistance equals to the gate resistance, a higher F will result in better Q according to Eq. (3). The capacitors used in DCCA are pMOS capacitors instead of MIM to save chip area. The nMOS switches are connected as capacitors to improve the Q of the capacitor array. When the switch is grounded, there is hardly any parasitic capacitor at the common node of VCO outputs. When the switch is turned on, the common node is equivalently connected to a fixed capacitor to keep the common node stable. The dimensions of pMOS capacitors and nMOS switches are both binary weighted, and the minimum pMOS capacitance is 1/4 of that of the varactor to ensure the overlaps of the 32 tuning curves. The on-chip differential inductor is simulated by ADS momentum and ASITIC. In order to increase the Q of the inductor, a shunt structure with a substrate ground shield is adopted. Finally, a 2-turn, 8-side differential inductor with a simulated inductance of 8nH and Q of 10 is used in the design.

There are two operation regions of VCO, namely the current-limited regime and the voltage-limited regime. The phase noise performance will be best at the transition edge from the current-limited regime to the voltage-limited regime due to the optimization of the output oscillation swing[7]. In addition, considering that the frequency at the common node of each cross-coupled pair is twice the oscillation frequency, an LC filter is usually implemented to prevent the pair from degrading the Q of the LC tank[8]. However, the additional area occupied by the inductor and the small frequency range of the high impedance provided by the inductor makes the LC filter unattractive. In this design, a 6bit digital controlled resistor array (DCRA) scheme is carried out. The current of the VCO can be adjusted by changing both the up and down tail resistance in Fig. 2. Meanwhile, the tail resistors are binary weighted and can act as high impedance filters over a wide frequency range.

3.3 Prescaler

The VCO is followed by one or two DTCs to generate the 868 or 433MHz band, as shown in Fig. 1. The DTC consists of two current mode logic (CML) based D flip-flops that can operate at high frequencies. The CML is a typical structure with a current tail and resistor loads[9]. The divided by four of VCO signals are fed into the prescaler via I, NI, Q, and NQ four quadrature signals as depicted in Fig. 3(a). It has a phase switch block (SEL), two DTCs (DTC1 & DTC2), and a differential-to-single amplifier (Op-amp), and can realize a dual modulus of 4/4.5. The quadrature control signals Ctrl1 and Ctrl2 are produced by AM counters, while the output signal OUT3 is used to control the AM counters. The 4bit A-counter is designed to count down by 2 while the 6bit M-counter is designed to count down by 1 when the rising edge of OUT3 appears. At the beginning, the A and M counters work simultaneously at the modulus of 4.5. The M-counter will continue counting when the A-counter stops, and the modulus will be changed to 4. After the M-counter finishes, the modulus will be changed back to 4.5. As a result, the division ratio is:

$$4.5 \times \frac{A}{2} + 4 \times \left(M - \frac{A}{2}\right) = 4M + \frac{A}{4} \tag{4}$$

where A and M represent the count values of the A counter and M counter, respectively.

The schematic of SEL is illustrated in Fig. 3(b).

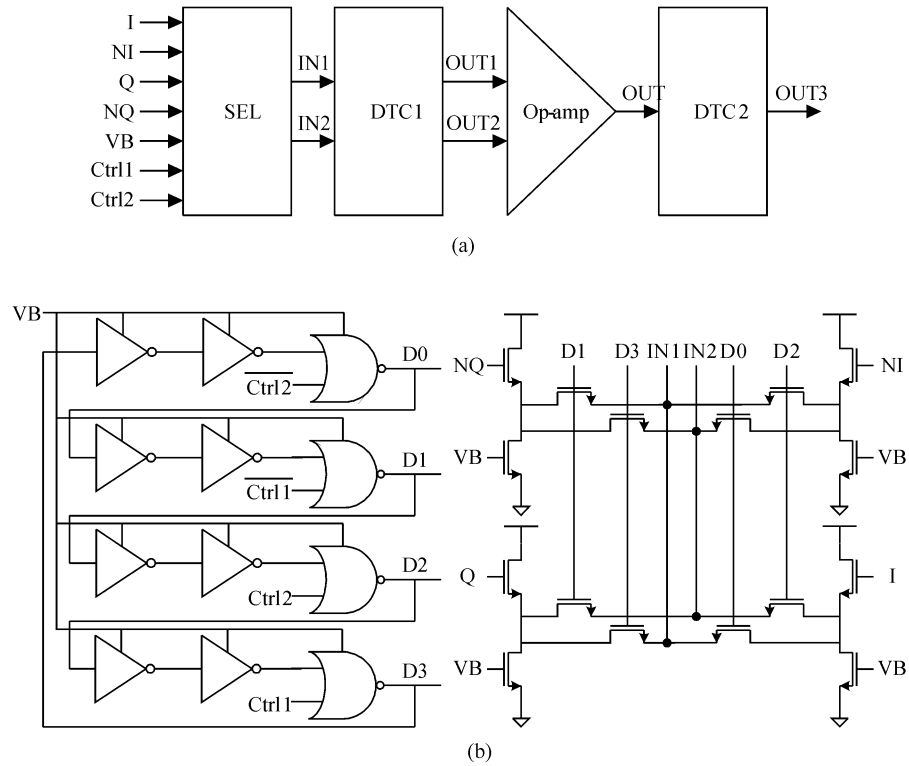

Fig. 3　(a) Block diagram of prescaler; (b) Schematic of SEL

It consists of a switch logic block on the left, and four source followers and eight switches on the right. Since the input frequency is over 400MHz, this gives a stringent requirement on the bandwidth of the source follower. However, there is no good method to increase the bandwidth of the source follower other than to increase the current, because changing other design parameters like the aspect ratio will also increase the parasitic capacitance. As a tradeoff between performance and power, the minimum channel length is adopted and the aspect ratio of the following switches is optimized.

DTC1 is also implemented with the typical CML structure with a current tail and dynamic loads[10]. The output swing can be varied by changing the bias of the pMOS loads from the digital control shown in Fig. 1. This ensures the DTC1 works correctly under any process variation and does not affect the function. The Op-amp in Fig. 3(a) is a two-stage amplifier. The first stage is a typical fully differential amplifier with diode connected pMOS loads, while the second stage is composed of a differential pair and an nMOS current source load with a single-end output. The aspect ratio of the pMOS loads of the first stage should be small enough to guarantee the bandwidth of the Op-amp. DTC2 is realized by connecting the negative output to the input of a true-single-phase-clocking (TSPC)[11] based D flip-flop that can operate at high frequencies and consumes less power than the CML structure.

3.4　Sigma-delta modulator and other building blocks

High order multi-bit quantization sigma-delta modulators have better noise shaping characteristics in terms of input range and output bit pattern than their single-bit and MASH counterparts[2]. Figure 4 shows the block diagram of the 3bit third order sigma-delta modulator adopted in this design. The input clock for all the delay parts, which is also the feedback signal of the PLL loop for PFD, is produced by *AM* counters, as illustrated in Fig. 1. The frequency synthesizer is programmed with a 23bit FREQ, after multiplying the programmed value by 2, the lower 14 bits FREQ[13:0] are fed to the sigma-delta modulator. The 3bit output of the sigma-delta will be added to the upper 10bit FREQ[23:14]. The upper 6bit and lower 4bit of this value are used as the restart values of the *M*-counter and *A*-counter, respectively. As shown in Fig. 4, the inputs of the sigma-delta modulator consist of the 14bit basis value, a 13bit frequency deviation value, and a dither. The dither is generated using the LSB of a 16bit linear feedback shift register (LFSR).

To avoid digital multiplication, the feed-forward factors of the sigma-delta modulator are 2, 0.5, and 1.5, which can be easily implemented by shifting operations[2]. As can be derived from Fig. 4, the noise transfer function (NTF) is:

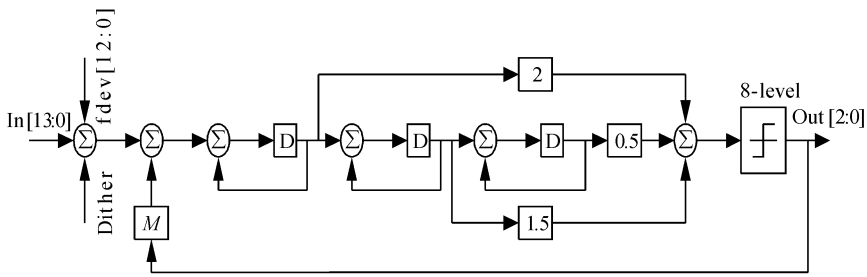

Fig. 4 Block diagram of the 3bit third-order SDM

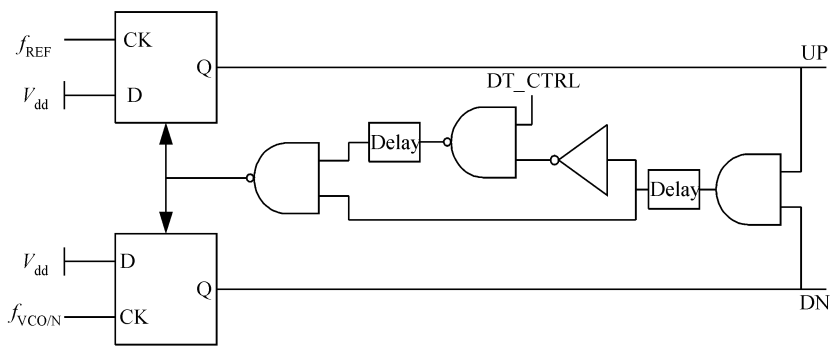

Fig. 5 Block diagram of PFD

$$\mathrm{NTF}(z) = \frac{(z-1)^3}{z^3 - z^2 + 0.5z} \tag{5}$$

The PFD used in this design is a three state architecture with standard D flip-flops. A delay cell is introduced to reduce the dead zone problem, and the choice of the delay time is critical in the whole design of the PLL. The delay time should be long enough to eliminate the dead zone, while short enough to decrease the ripples on the control voltage of the VCO. So the delay time can be adjusted through the DT_CTRL shown in Fig. 5.

A classical structure of a CP with a dummy branch using complementary switches and a programmable current scheme is adopted in this design. The controls of the switches are produced by a timing control scheme[12] to further suppress the spurious tones. Regarding the implementation of the sigma-delta modulator, an off-chip third order passive loop filter is used. The values of the resistors and capacitors are carefully chosen through behavioral simulations of PLL.

4 Measurement results

This fractional-N frequency synthesizer with AFC has been fabricated in 0.35μm CMOS technology. Figure 6 shows the die photomicrograph of the synthesizer with an area of 1.5mm×1.2mm.

To verify the synthesizer performance, a 4.9MHz reference clock was used in the measurement with the synthesizer operating in the 433MHz band and setting

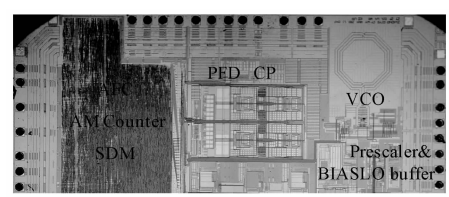

Fig. 6 Die photo

the PLL bandwidth to 8kHz and the CP current to 60μA. The AFC is verified to be working correctly by observing the control voltage of the VCO in an oscilloscope, shown in Fig. 7. The measured total lock time is about 500μs according to Fig. 7. The measured PLL locking frequency range is from 327 to 470MHz, so the VCO frequency range is from 1.31 to 1.88GHz. Hence, the tuning range is as wide as 570MHz. The current consumption of the whole frequency synthesizer together with the LO buffer is 19mA under the supply voltage of 3.0V. The noise in Fig. 7 comes from the instruments.

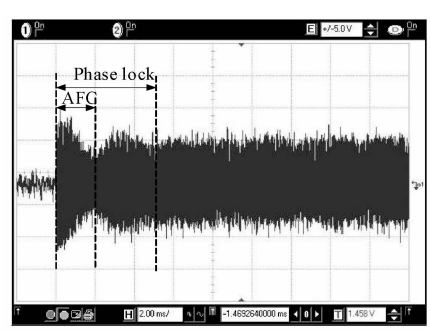

Fig. 7 Control voltage of VCO

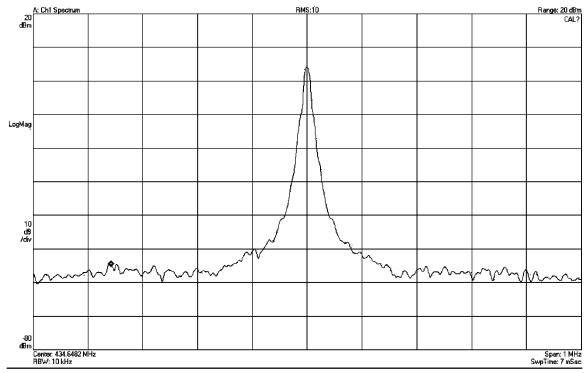

Fig. 8　PLL output spectrum at 434.6MHz

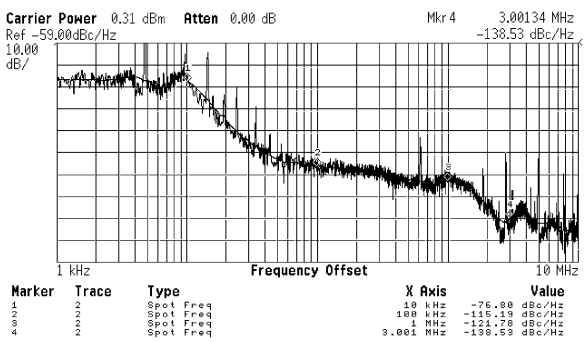

Fig. 9　PLL phase noise at 434.6MHz

Figure 8 depicts the measured PLL output spectrum at 434.6MHz. The fractional spur is under −60dBc in a 1MHz offset range. Figure 9 shows that the measured PLL phase noise of the 434.6MHz carrier frequency is −115dBc/Hz at 100kHz offset, −122dBc/Hz at 1MHz, and −139dBc/Hz at 3MHz. The in-band phase noise is −77dBc/Hz, which is quite high. The deterioration of the in-band noise may be due to the noise folding in the PFD and CP[4] or the relatively small bandwidth of the PLL[6]. The measured performances are summarized and compared to other designs reported recently in Table 2. According to Table 2, the chip area, the VCO frequency range, and the phase noise performances of the proposed synthesizer are among the best. Moreover, the proposed synthesizer consumes the least current. Only the lock time is the longest because of its small loop bandwidth.

5　Conclusion

A Σ-Δ fractional-*N* frequency synthesizer implemented in a 0.35μm CMOS process using a wide-band VCO and a fully digital AFC circuit for 433/868MHz SRD applications has been presented. A DCRA scheme is proposed for VCO to improve the phase noise while not significantly increasing the area. A novel structure for the prescaler is implemented in the design to save power. The measured total current consumption including the LO buffers for the transmitter is only about 19mA from a 3.0V supply. The total lock time including AFC is about 500μs. A 3bit third order Σ-Δ modulator is adopted to reduce the out-band phase noise. The measurement results show the out-band phase noise is −139dBc/Hz at 3MHz offset frequency and the fractional spur is less than −60dBc. Future work will focus on improving the in-band phase noise.

Table 2　Performance summary and comparison

	Lo[13], (JSSC 02)	Lee[4], (JSSC 04)	This work
Power supply	1.5V	2.8V	3.0V
Technology	0.5μm CMOS	0.5μm BiCMOS	0.35μm CMOS
Die size	0.9mm×1.1mm	3.8mm×1.2mm	1.5mm×1.2mm
Current dissipation	20mA	19.5mA	19mA
VCO frequency range	760～980MHz	1.15 ～ 1.75GHz	1.31 ～ 1.88GHz
Reference clock	25.6MHz	13MHz	4.9MHz
Loop bandwidth	80kHz	25kHz	8kHz
In-band phase noise	N.A.	−80dBc/Hz	−77dBc/Hz*
Out-band phase noise	−116dBc/Hz @ 400kHz −118dBc/Hz @ 600kHz (Carrier: 900MHz)	−129dBc/Hz @ 400kHz −139dBc/Hz @ 3MHz (Carrier: 1.4GHz)	−115dBc/Hz @ 100kHz* −122dBc/Hz @ 1MHz* −139dBc/Hz @ 3MHz*
Fractional spurious	−67dBc	−70dBc @ 300kHz	<−60dBc
Lock time (Including AFC)	<100μs (No AFC)	<150μs	<500μs

* Measured at the carrier frequency of 434.6MHz

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一种用于短距离器件的带自校准的Σ-Δ分数分频频率综合器

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摘要：介绍了一种应用于433/868MHz频段短距离器件的分数分频频率综合器.采用带自适应频率校准的宽带压控振荡器来覆盖要求的频段,并采用3位量化、3阶的Σ-△调制器来实现分数分频和改善锁相环的带外噪声.测试结果表明,自适应频率校准能够正常工作,压控振荡器的频率调节范围为1.31～1.18GHz,在3MHz频偏处的带外噪声为－139dBc/Hz,分数毛刺低于－60dBc.芯片采用0.35μm CMOS工艺,芯片面积仅为1.8mm^2,功耗仅为57mW.

关键词：短距离器件；锁相环；自适应频率校准；频率综合器；sigma-delta
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