A Low Noise, High Linearity CMOS Receiver for 802.11b WLAN Applications*

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Abstract: A 2.4GHz monolithic CMOS receiver with direct-conversion architecture is presented. This quadrature receiver is designed for 802.11b wireless LAN applications at the maximum data rate of 11Mbps as a low-cost solution. Five key blocks, i.e., a low noise amplifier (LNA), a down-conversion mixer, a variable gain amplifier, a low pass filter, and a DC-offset cancellation circuit, are designed based on system design and low noise high linearity considerations. The necessary auxiliary circuits are also included. Fabricated in SMIC 0.18μm 1p6m RF CMOS process, the receiver's performance is measured as: 4.1dB noise figure, −7.5dBm input third order intercept point (IIP3) for LNA & mixer at high gain setting, −14dBm IIP3 for the whole receiver, 53dBc @30MHz offset of adjacent channel power rejection, and less than 5mV output DC-offset. The receiver consumes 44mA under a 1.8V power supply with I, Q two paths.

Key words: 802.11b; wireless LAN; receiver; DC-offset cancellation; mixer
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1 Introduction

Wireless LAN (WLAN) is seen as the technology that can enable the most convenient link between existing wired networks and portable computing and communication equipment. Although there are several mature IEEE standards for WLANs, such as 802.11b, 802.11a, and 802.11g, products based on 802.11b gained mainstream acceptance as the first wireless networking products with acceptable speeds, affordable prices, and universal compatibility as certified by the Wi-Fi Alliance[1]. Moreover, 802.11b is upwards compatible with 802.11g. A super-heterodyne architecture was traditionally used to implement 802.11b RF transceivers[2,3] and a direct-conversion architecture is prevailing recently due to the advantages of high integration and low cost[4,5].

This paper presents a monolithic direct-conversion low noise, high linearity RF receiver targeted for 802.11b WLAN applications. This receiver completely consists of front-end circuits, that is, a low noise amplifier (LNA), a down-conversion mixer, a variable-gain amplifier (VGA), a low-pass filter (LPF), and a DC-cancellation circuit. The paper also presents some circuit design improvements and measurement results.

2 Receiver implementation

The block diagram of the direct-conversion receiver is shown in Fig. 1. LNA first amplifies the received RF signal with high/low gain and the amplified signal is directly down-converted to the baseband signal with 2.4GHz local oscillator (LO) signals. The baseband signal is first sent through a high-linear VGA in order to mitigate the low noise requirement of the succeeding filter stage. Channel selection is realized by a fourth-order Chebyshev LPF. Two casca-

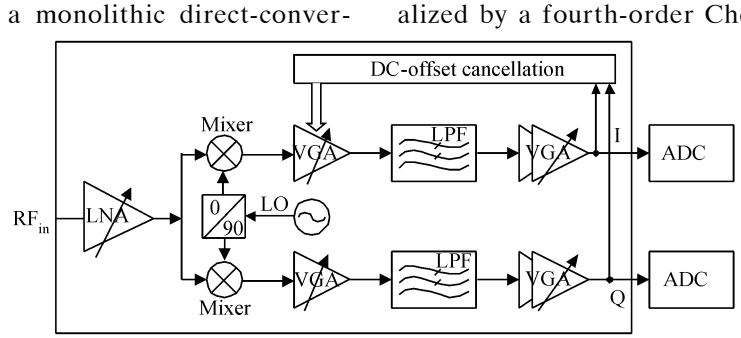

Fig. 1 Block diagram of the direct-conversion receiver

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ded VGAs are used to amplify the baseband signal further to meet the signal range required by analog-digital converters (ADC). The DC-offset caused in this receiver chain is reduced by the DC-offset cancellation circuit. A quadrature down-conversion scheme is adopted in this work to avoid loss of information[6].

2.1 Receiver system design

The goal of the system design is to determine the feasible specifications for the receiver and each building block from the standard, which is crucial for performance guarantee. 802.11b WLAN is a direct sequence spread-spectrum system with CCK modulation and the occupied channel bandwidth is 22MHz spaced 25MHz apart, providing a data rate up to 11Mbps. At this max data rate, the receiver sensitivity is −76dBm with a frame error rate (FER) of 8×10^{-2}[7]. Based on these physical layer (PHY) standards, a bit error rate (BER) of 10^{-5} at receiver output can be derived by the following equation:

$$\mathrm{BER}=1-(1-\mathrm{FER})^{1/L_{\mathrm{FER}}} \tag{1}$$

where L_{FER} is the number of bits in the frame. The simulated ideal $\mathrm{SNR}_{\mathrm{min}}$ of the receiver corresponding to 10^{-5} BER using ADS is around 11.4dB. However, there are many non-idealities in a real receiver chain, such as DC-offset, filter frequency response, ADC sampling rate, and I/Q mismatch. When these combined degradation effects are considered, in this work, 5% DC-offset, 4th order Chebyshev I LPF with 7MHz cut-off frequency, 44MHz of ADC sampling rate, 10% I/Q gain mismatch, and 5° phase mismatch, the required $\mathrm{SNR}_{\mathrm{min}}$ is 13.7dB, degraded by 2.3dB. From the relationship between sensitivity and noise figure (NF), expressed as,

$$\mathrm{NF}=\mathrm{Sensitivity}-\mathrm{SNR}_{\mathrm{min}}-(-174+10\lg(\mathrm{BW}))-\mathrm{margin} \tag{2}$$

a receiver NF of 11.8dB can be obtained, where 4dB design margin is added.

The other important specification for the receiver, the input third order intercept point (IIP3), can be given by

$$\mathrm{IIP3}=\frac{1}{2}(3P_{\mathrm{int}}-P_{\mathrm{sig}}+\mathrm{SNR}_{\mathrm{min}})+\mathrm{margin} \tag{3}$$

where P_{int} and P_{sig} are the interference and signal levels when the third order inter-modulation product (IM3) test is conducted. Again, some margin is added to account for implementation loss. There is an assumption that the IM3 is not larger than the noise effects of the receiver. Because there is no specific IIP3 test in 802.11b, the adjacent channel test can be used to estimate roughly the required IIP3 of the receiver, but some modification is needed[8]:

Table 1　System specifications for WLAN 802.11b direct-conversion receiver

Data rate	Sensitivity	Bit error rate	Max. input	$\mathrm{SNR}_{\mathrm{min}}$	IIP3	NF
11Mbps	−76dBm@ 8×10^{-2} FER	10^{-5}	−10dBm	13.7dB	−12dBm	11.8dB

$$\mathrm{IIP3}=\frac{1}{2}\times(3P_{\mathrm{int}}-P_{\mathrm{sig}}+\mathrm{SNR}_{\mathrm{min}}-4.75)+\mathrm{margin} \tag{4}$$

Substituting −38dBm P_{int}, −73dBm P_{sig}, and 4dB margin in Eq.(4), the required IIP3 is −12dBm. The receiver system specifications are summarized in Table 1.

2.2 LNA

A fully differential LNA, whose schematic is shown in Fig.2, is used in this work to reduce LO-RF feed-through and switching noise from digital circuits.

A cascoded structure with inductor source degeneration is adopted; the sizes of nMOS M1 and M2 and the inductances of L_{s1} and L_{s2} are key elements for input impedance match to 50Ω, and the parasitic capacitors introduced by input pad also must be included. Because the input signal is in a wide range from −76 to −10dBm, RF front-end can not handle the entire signal range with only one LNA gain setting. In this work, LNA has high and low two gain settings in addition to the sequence VGA gain control. The low gain setting is necessary for the consideration of mixer linearity while the input signal is high. Usually, there are two methods to achieve high/low gain. One is to use a different output load by a switch[9], which has a drawback of narrow gain difference between the high gain setting and low setting. The other is to use two different input signal paths[9,10], but its disadvantage is that two different input matching strategies are needed. In this work, when V_{h} is in high voltage level (at this time, V_{L} is low), nMOST M7 and M8 are off, nMOST M3, M5, M4, M6 are on, all signals go through *LC* load differentially and high gain setting is

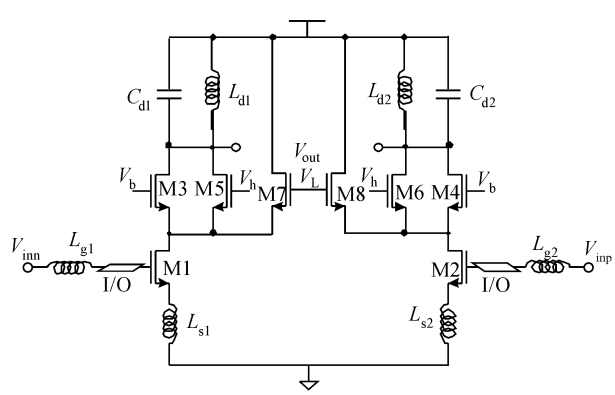

Fig.2　Circuit schematic of LNA

realized. When V_h is low (at this time, V_L is high), M5, M6 are off, and M7, M8 are on, part of the signal is bypassed to the power supply, and, as a result, a low gain setting is obtained. This method circumvents the drawback encountered in Ref. [10]. The simulated high gain and low gain under typical conditions (TT corner, 50° and 1.8V) are 26.3 and 4dB, respectively.

Besides input impedance match and high/low gain settings, another important issue in LNA design is the noise optimization. Noise optimization mentioned in Ref. [11] is derived based on a single MOST, so it is unsuitable for the whole LNA with a source on-chip inductor and a cascoded structure. When the effect of source on-chip inductor is included, the optimum width of the input nMOSTs (M1, M2 in Fig. 2) can be obtained by MATLAB to acquire good noise performance with satisfactory input impedance matching. According to the NF formula of a cascade system and a system NF requirement of 11.8dB, the NF of the LNA should be less than 2.5dB at high gain setting. In this work, the widths of M1, M2 are 200μm, and the simulated NF at typical conditions is 1.5dB, much better than the specification.

2.3 Down-conversion mixer

Not only is the desired signal amplified by LNA, but also the interferers. These interferers will generate non-linearity while going through the mixer, among which the most significant is the third order inter-modulation product. So IIP3 is an important linearity specification for the mixer. Traditional Gilbert active double-balanced mixers suffer limited linearity when applied in the low supply case, for example, the 0.18μm CMOS process, because high linearity requires large over-driven voltage for RF signal input MOSTs.

This paper presents an improved mixer circuit for the two-stage structure, and the schematic is shown in Fig. 3. The first stage is a *V-I* converter and the second stage implements frequency conversion from RF to baseband. With a source degeneration resistor R_s, the output current of the *V-I* conversion stage is:

$$I_{\text{out\_}V\text{-}I} = \frac{2v_{\text{RF}}}{R_s + 2/g_m} \tag{5}$$

where g_m is the transconductance of M1 and M2 of Fig. 3. $I_{\text{out\_}V\text{-}I}$ is proportional to v_{RF} when $R_s g_m \gg 1$, which means good linearity. Though there is a little decrease in mixer conversion gain, the resulting degradation in system noise performance is slight. Another non-linearity source is the switching pairs (M3 ~ M6 in Fig. 3) in the 2nd stage. It has been reported that the LO signal amplitude on the switching pairs' gates and DC-biasing current through switching MOSTs should be optimized for high linearity[12]. Under typical simulation conditions, the simulated IIP3 of the mixer is 11.6dBm, the 1dB compression point is 1.3dBm, the voltage conversion gain is 3dB, and the NF is 14.4dB@10MHz.

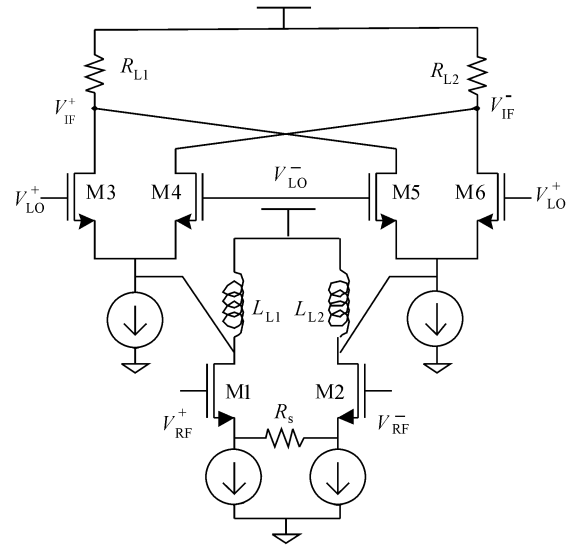

Fig. 3 Circuit schematic of down-conversion mixer

2.4 VGA and LPF

In order to handle a wide input signal range, three VGAs totaling 60dB gain are used with 0~20dB adjustable gain for every stage. For good noise performance and large dynamic range, one VGA is placed before the LPF and the other two after the LPF (see Fig. 1). The VGA schematic in this paper is shown in Fig. 4 (a).

The VGA is a closed-loop amplifier with resistive feedback. Gain control is realized by the ratio of the digitally programmable feedback resistor to the resistor in the forward path with 3dB/steps. This type of VGA has excellent linearity when the gain of the open-loop op amp is high. The schematic of the op amp is shown in Fig. 4 (b), in which a simple two-stage structure is chosen. The pMOS input stage has some advantages over nMOS input such as bigger GBW, lower noise, etc. M7, M8 move the RHP zero to LHP and cancel the non dominant pole. The simulation results of op amp under typical conditions are: DC gain 65dB, GBW 150MHz, phase margin (PM) 67°. The simulation results of VGA are: 19.9~0.3dB of variable gains, 14MHz of 3dB-BW, 61° of PM with 5pF load, and the input referred noise is about 4.95nV/$\sqrt{\text{Hz}}$.

According to the requirement for receiver selectivity, the adjacent channel power rejection (ACPR) of 50dBc at 30MHz offset must be met for a channel selection LPF. A Butterworth filter has an excellent pass-band ripple factor, but its stop-band suppression

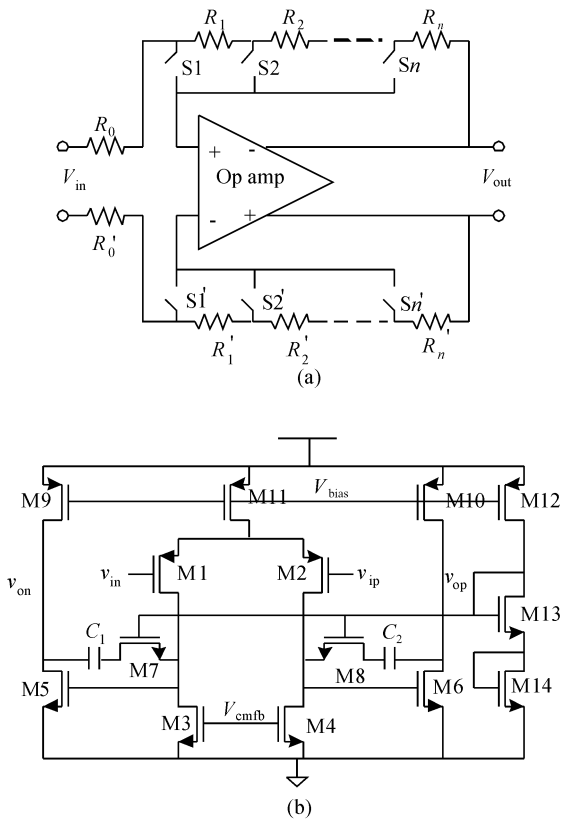

Fig. 4　(a) Schematic of VGA; (b) Circuit schematic of op amp

capability is inferior to a Chebyshev I filter of the same order. As a compromise between circuitry complexity and the overall performance of the receiver, a fourth-order Chebyshev I filter is chosen as the baseband filter to select the desired channel and suppress the adjacent channel interference. As for the cut-off frequency of the LPF, the higher it is, the less attenuation for the adjacent channel interference and the more noise passed to the demodulator; the lower the cut-off frequency is, the more significant portion of the signal spectrum is rejected. As a result, there is a trade-off between cut-off frequency and receiver SNR. By using SystemVue, the cut-off frequency of the fourth-order Chebyshev I LPF is determined to be around 7MHz. In this work, the fourth-order LPF is implemented by cascading two second-order Tow-Thomas LPFs. Simulated results under typical conditions are: a 7.6MHz cut-off frequency with 0.3dB in-band ripple; a 55dBc ACPR at 30MHz offset.

2.5　DC-offset cancellation circuitry

DC-offset is one problem in a direct-conversion receiver and can lead to receiver saturation, making it lose the capability of handling input signals. The DC-offset must be reduced to some extent to meet the system NF specification. Figure 5 is the DC-offset cancellation circuit adopted in this work. A feedback low

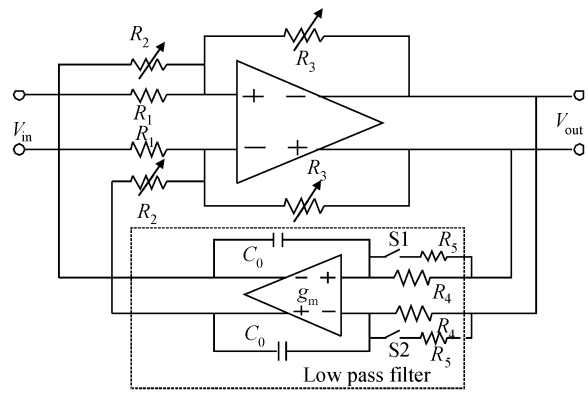

Fig. 5　DC-offset cancellation with fast setting

pass filter is employed here to extract the DC-offset at VGA output and substrate it at VGA input; the closed loop is equivalent to a high pass filter (HPF) and attenuates the DC-offset to an acceptable level. The transfer function is:

$$V_{\text{out}} = V_{\text{in}} \frac{1}{g_{\text{m}} R_1} \times \frac{1 + g_{\text{m}} R_2 R_4 C_0 s}{1 + (R_2 R_4 C_0 s)/R_3} \qquad (6)$$

This equation reveals that the DC-offset is reduced by a factor of $1/g_{\text{m}}R_1$ using this cancellation circuit. One key specification of this cancellation is the corner frequency f_{c} of the HPF. For losing as little desired information as possible, f_{c} should be low enough, which is contradictory to areas of resistor R_4 and capacitor C_0. As a tradeoff between performance and chip area, f_{c} is chosen as 100kHz here, and for decreasing area further, C_0 is connected between the input and output of the g_{m} block. In order to reduce the time needed for DC-offset calculation which happens for the case of receiver initialization, transition between R_x and T_x, or receiver gain change, resistor R_5 is added in parallel with R_4, and the resistance of R_5 is only one tenth of R_4. When DC-offset is recalculated, switches S1 and S2 are closed and fast setting is realized. Simulation results show that the setting time is less than 5μs and the output DC offset is below 5mV.

3　Experimental results

The receiver IC was fabricated in a 0.18μm 1p6m CMOS process and its die micrograph is shown in Fig. 6. The bare die is bonded on a printed circuit board (PCB) with external components mounted on PCB, such as SMA connecters, Balun, off-chip match devices, etc.

The input reflection parameter S_{11} was measured by an Agilent Network Analyzer (E5071B 300kHz～8.5GHz ENA Series) and the result is shown in Fig. 7. In the whole 802.11b WLAN frequency range from 2.4 to 2.483GHz, S_{11} is less than −11dB, and S_{11} is only −17.5dB at a frequency around 2.49GHz,

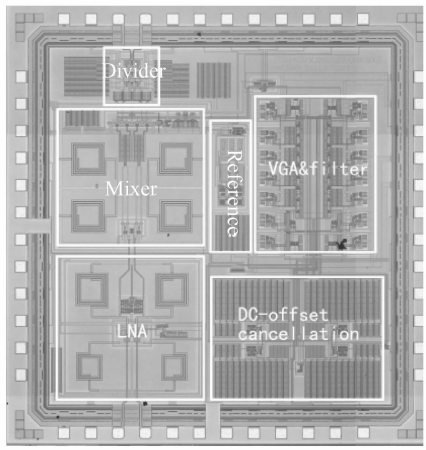

Fig. 6 Micrograph of the receiver

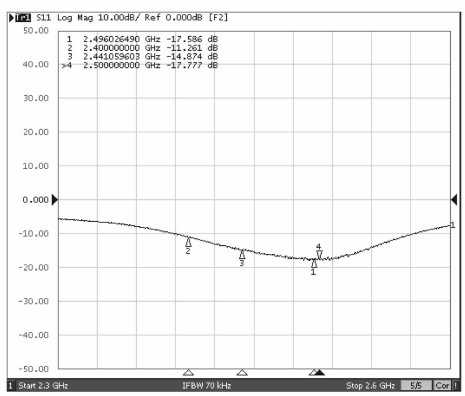

Fig. 7 Measured S_{11} of receiver

which means good input impedance matching performance.

The receiver gain was measured by an Agilent spectrum analyzer (E4440A 3Hz～26.5GHz PSA Series). Loss introduced by instruments cable and Balun in PCB was measured to be 2.2 and 0.9dB, respectively. Then, a 2.446GHz −80dBm signal is added at the input of receiver, LO is 2.44GHz, LNA is set at high gain, producing −57.05dBm with 6MHz frequency. The mixer output spectrum is shown in Fig. 8. The gain of LNA and mixer at high LNA gain setting is

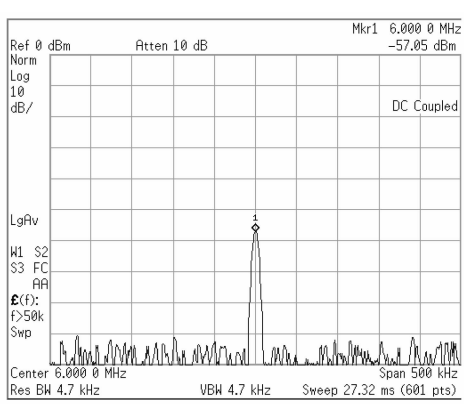

Fig. 8 Mixer output spectrum at high LNA gain

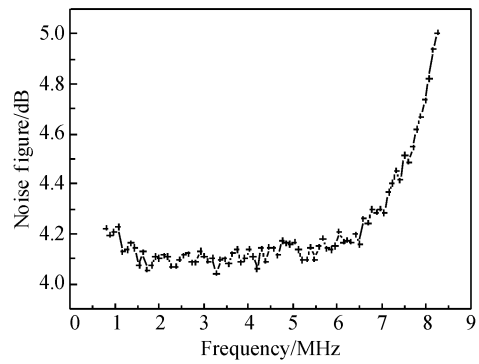

Fig. 9 Measured DSB NF of receiver at maximal gain setting

26dB after calibration, 3dB less than the simulated result. A possible reason is the real Q of the on-chip inductor is lower than that used in simulation. At the low LNA gain setting, with the same input signal, the output spectrum of the mixer is −79dBm, and there is a 22dB difference which verifies the simulated high/low gain setting of LNA. The gain of the VGA is measured in similar way, and summarized in Table 2.

The noise figure of the receiver was measured using the Y parameter method, and the instruments include an Agilent 346C noise source and an E4440A 3Hz～26.5GHz PSA. The measured double-side band (DSB) receiver NF is shown in Fig. 9 at the max. receiver gain. In the whole passband, the NF is around 4.1dB and begins to increase at LPF cut-off frequency, much better than the system specification. At this measured NF, this receiver has a sensitivity of −83dBm for 11Mbps. One reason for such a low NF is that each block is designed carefully for low noise performance, and the other reason involves non-idealities, for example, I/Q mismatches are nearly null because there is no PLL included in this work.

Using a two-tone test, the measured IIP3 of LNA & mixer is −7.5dBm at high LNA gain setting, as shown in Fig. 10, and the measured IIP3 of the whole receiver is about −14dBm, shown in Fig. 11, at the test condition of high LNA gain and 12dB IF gain. The measured IIP3 is 2.5dBm worse than the simulated result. The receiver channel selectivity was measured using an Agilent network analyzer. The out-

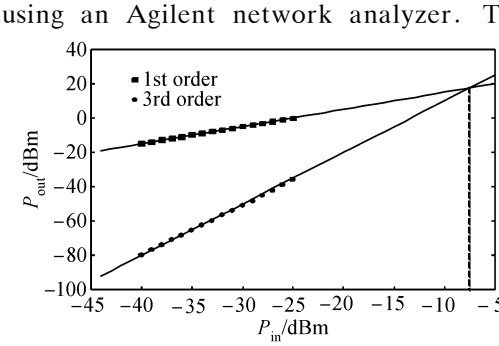

Fig. 10 Measured IIP3 of LNA & mixer at high LNA gain

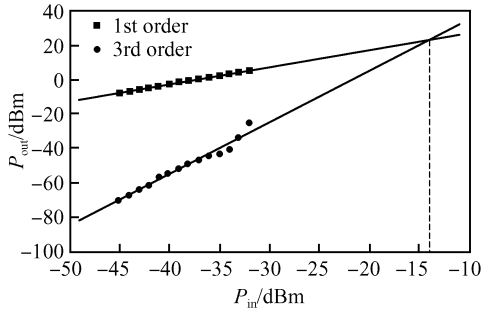

Fig.11　Measured IIP3 of whole receiver

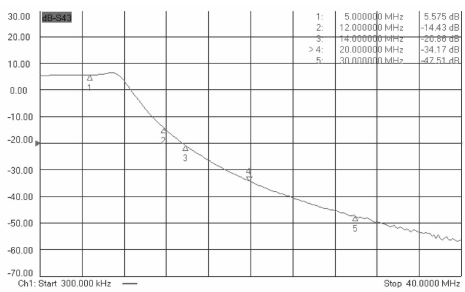

Fig.12　Out-channel attenuation of receiver

channel attenuation performance is shown in Fig. 12, and 53dBc ACPR at 30MHz offset is achieved.

The measured receiver performance and comparison are summarized in Table 2.

Table 2　Summary of measured receiver performance and comparison

Reference	[4]	[5]	[9]	[10]	This Work	Spec
Sensitivity /dBm	/	−88	−77	−80	−83	−76
NF/dB	5.4	4.8	3.5	/	4.1	11.8dB
IIP3@max gain/dBm	−4	−15	9*	−12	−14	−12
Voltage gain/dB	92	88	/	/	89	n/a
Channel selectivity /MHz	7**	8** 39dBc@ 25MHz	/	7.5**	7.7** 53dBc@ 30MHz	/ 50dBc@ 30MHz
Output DC-offset /mV	/	/	/	/	<5	n/a
Power/mW	261	165	260	108	79.2***	n/a
Technology	0.5μm BiCMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	n/a

* IIP3@min gain

** Cut-off frequency

*** Not including power consumption of PLL

4　Conclusion

This paper presents an integrated 0.18μm CMOS direct-conversion receiver with low noise and high linearity performance. This quadrature RF receiver chain includes five key blocks: an LNA, down-conversion mixer, three stages of VGAs, a fourth-order Chebyshev I LPF, and a DC-offset cancellation circuit. The receiver can handle correctly the RF signal of the frequency range from 2.4 to 2.483GHz, and achieves a 4.1dB NF, less than −11dB S_{11}, 53dBc ACPR at 30MHz offset, and less than 5mV output DC-offset. The IIP3 of LNA & mixer at high gain setting is −7.5dBm, the IIP3 of the whole receiver is around −14dBm. The measured receiver performance shows the system specifications are almost satisfied and the receiver is suitable for 802.11b WLAN application.

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应用于 802.11b 无线局域网的低噪声高线性度的 CMOS 射频接收机*

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摘要：实现了一个单片集成、直接转换结构的 2.4GHz CMOS 接收机.这个正交接收机作为低成本方案应用于 802.11b 无线局域网系统，所处理的数据传输率为该系统的最大速率——11Mbps.基于系统设计以及低噪声高线性度考虑，设计了低噪声放大器、直接转换混频器、增益可变放大器、低通滤波器、直流失调抵消电路及其他辅助电路.该芯片采用中芯国际 0.18μm 1p6m RF CMOS 工艺流片，所测的接收机性能如下：噪声系数为 4.1dB，高增益设置下低噪声放大器与混频器的输入三阶交调点为 -7.5dBm，整个接收机的输入三阶交调点为 -14dBm，相邻信道干扰抑制能力在距中心频率 30MHz 处达到 53dBc，输出直流失调电压小于 5mV.该接收机采用 1.8V 电源电压，I，Q 两路消耗的总电流为 44mA.

关键词：802.11b；无线局域网；接收机；直流失调抵消；混频器

EEACC：1265B；2570D

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