A Low Jitter PLL in a 90nm CMOS Digital Process

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Abstract: A low jitter phase-locked loop (PLL) that does not need analog resistors and capacitors is designed and fabricated in a 90nm CMOS digital process. The metal parasitic capacitor is used in the PLL loop filter. Test results show that when the PLL is locked on 1.989GHz, the RMS jitter is 3.7977ps, the peak-to-peak jitter is 31.225ps, and the power consumption is about 9mW. The locked output frequency range is from 125MHz to 2.7GHz.

Key words: PLL; PFD; charge pump; VCO
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1 Introduction

The development of VLSI requires high performance clock generators, which mainly use PLL-based structures. However, a large amount of digital switches make the on-chip noise environment worse. The supply and substrate noise result in high output signal jitter in PLLs. As the clock period decreases, the tolerance of clock jitter is confined to narrow limits. Therefore, the design of a low jitter PLL is an urgent demand.

For a custom charge pump PLL design, the loop bandwidth is constrained to be well below the lowest operating frequency for stability[1]. But, low jitter PLL requires a high loop bandwidth to reject the voltage control oscillator (VCO) internal or supply/substrate noise. Fortunately, the self-biased structure suits the low jitter PLL design because the loop bandwidth tracks the reference frequency and both the damping factor and the loop bandwidth to reference frequency ratio are immune to power, voltage, and temperature (PVT) variation[2]. However, PLL loop filters usually need analog processes, which provide high-density linear capacitors and polysilicon resistors. Furthermore, analog processes are about two years behind digital processes[3], limiting PLL design in a new generation of CMOS processes.

In this work, a low jitter PLL based on self-biased technology is presented. Because the process has no high-density linear capacitors, the metal parasitic capacitor is used as the PLL loop capacitor. Low jitter performance is achieved through well-designed circuits and layouts.

2 Charge pump PLL and self-biased technology

A charge pump PLL consists of five blocks including the phase frequency detector (PFD), charge pump (CP), loop filter, VCO, and divider. When the PLL loop bandwidth is smaller than the signal frequency, a simple transfer function can be used to analyze PLL systems[1]. Figure 1 shows a linear model of a second order charge pump PLL.

We can get the closed loop transfer function from Fig. 1 as:

$$H(s)=\frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s+1)}{s^2+\frac{I_P K_{VCO} R_P}{2\pi N}s+\frac{I_P K_{VCO}}{2\pi C_P N}} \tag{1}$$

The nature frequency and the damping factor can be written as:

$$\omega_n=\sqrt{\frac{I_P K_{VCO}}{2\pi C_P N}} \tag{2}$$

$$\zeta=\frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi N}} \tag{3}$$

Both values above are fixed when circuits' parameters are determined. In order to make the natural

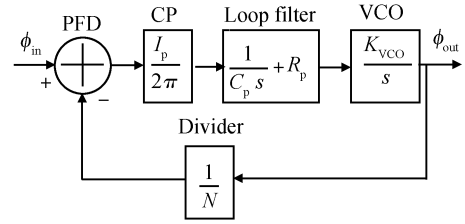

Fig. 1 Linear model of a second order charge pump PLL

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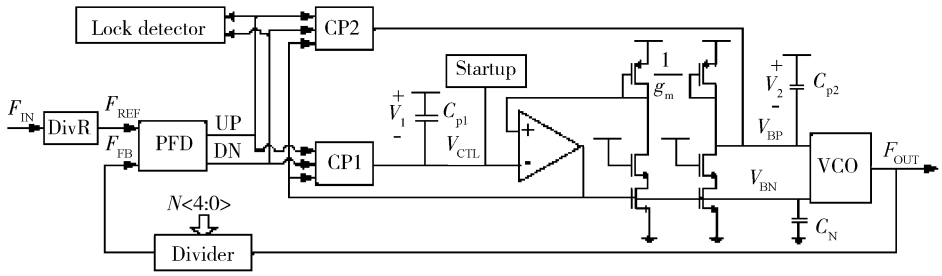

Fig. 2 PLL structure

frequency track the reference frequency, the self-biased PLL adopts the replica current feedback bias technology[2]. The relationships of the circuit parameters are shown below:

Charge pump current: $I_P = xI_{BUF}$ (4)

Loop filter resistor: $R_P = \frac{y}{2g_m} = \frac{y}{\sqrt{4\beta I_{BUF}}}$ (5)

VCO frequency: $\omega_{osc} = 2\pi \frac{g_m}{2nC_d} = 2\pi \frac{(\beta I_{BUF})^{1/2}}{2nC_d}$ (6)

VCO gain: $K_{VCO} = 2\pi \frac{\beta}{2nC_d}$ (7)

where I_{BUF} is the bias current of each buffer in the VCO, β equals $u_n C_{ox} W/L$, C_d is the effective buffer output capacitance, and $1/g_m$ is the equivalent resistance load of the VCO buffer. The natural frequency and damping factor of the self-biased PLL can be written as:

$$\omega_n = \frac{(xN)^{1/2}}{2\pi}\left(\frac{2nC_d}{C_P}\right)^{1/2}\omega_{REF} \quad (8)$$

$$\zeta = \frac{y}{4}\left(\frac{x}{N}\right)^{1/2}\left(\frac{C_P}{2nC_d}\right)^{1/2} \quad (9)$$

Thus, the damping factor is fixed and the natural frequency tracks the reference frequency. The PLL's stability is not influenced by PVT variation because on-chip capacitance matching is easy.

Reference [4] considers the different VCO gain K_1 and K_2 (sensitive to V_1 and $V_1 - V_2$, respectively), as shown in Fig. 2. More accurately, the natural frequency and damping factor can be rewritten as[4]:

$$\omega_N = \frac{1}{R_0}\sqrt{\frac{x_1}{C_{P1}N}}\sqrt{I_{BUF}K_1R_0^2} \quad (10)$$

$$\zeta_0 = \frac{yx_2}{2} \times \frac{K_2}{K_1}\sqrt{\frac{C_{P1}}{x_1N}}\sqrt{I_{BUF}K_1R_0^2} \quad (11)$$

where $I_{CP1} = x_1 I_{BUF}$, $I_{CP2} = x_2 I_{BUF}$, R_0 is the unit resistance of VCO buffer load, and $I_{BUF}K_1R_0^2$ is a constant over VCO linear range. The 3rd order degradation approximation of the damping factor is[4]:

$$\zeta = \zeta_0[1 - e^{-T_{ref}/\tau_2}] = \zeta_0\Gamma \quad (12)$$

where $\tau_2 = RC_{p2}$ and T_{ref} is the reference signal period. Better performance could be obtained through optimizing parameters C_{P1}, C_{P2}, x_1, x_2, and y.

3 Circuit designs

The PLL structure is shown in Fig. 2. For a typical second order PLL, the loop filter is a resistor in series with a capacitor[3]. In order to obtain the resistor described by Eq. (5), diode-connected transistors are used. Two charge pumps (CP1, CP2) are used to drive the capacitor and resistor separately. The two voltage drops are summed to form the control voltage by replicating the voltage across the capacitor with a voltage source placed in series with the resistor[2]. The loop filter for this PLL is equivalent to a resistor ($1/g_m$) in series with a capacitor (C_{P1}).

3.1 PFD circuit

PFD compares the feedback signal phase with the reference signal phase and generates voltage pulses. The pulse width represents the phase difference of the two signals. If the pulse width is too narrow to open the charge pump switch, the PFD/CP circuits suffer from a dead zone[3]. The dead zone is highly undesirable because it will cause tracking jitter[3]. Therefore, a buffer delay has been added to the reset path to eliminate the dead zone, as shown in Fig. 3.

3.2 Charge pump circuit

In order to achieve zero phase error, the charge pump circuit does not need to transfer charges to the

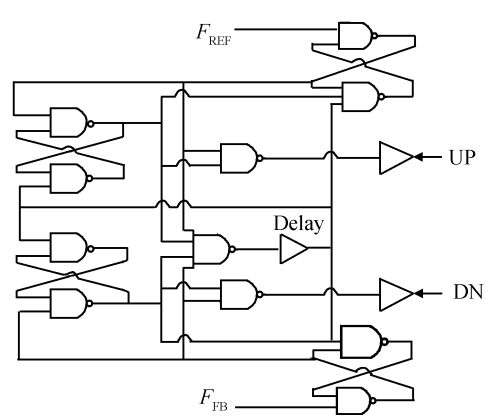

Fig. 3 PFD circuit

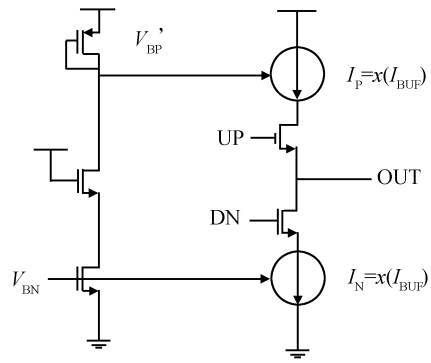

Fig. 4　Charge pump circuit

loop filter when the PLL is locked. Beyond the eliminating dead zone design in the PFD circuit, the charge pump circuit uses replica current feedback technology to make the charge current and the discharge current equal, as shown in Fig. 4. The charge current control signal V'_{BP} is generated by the V_{BN} signal in the charge pump circuit. Both the charge and the discharge current control signals are stable. PFD/CP simulation results are shown in Fig. 5. The relationship between the phase difference and the voltage change is linear and there is no apparent dead zone; The charge and the discharge currents are nearly the same in the VCO control signal's working range.

3.3　Voltage control oscillator

VCO is the key block in low jitter PLL designs. Any ripple on control or power/ground signals result in bad phase noise performance, represented as jitter

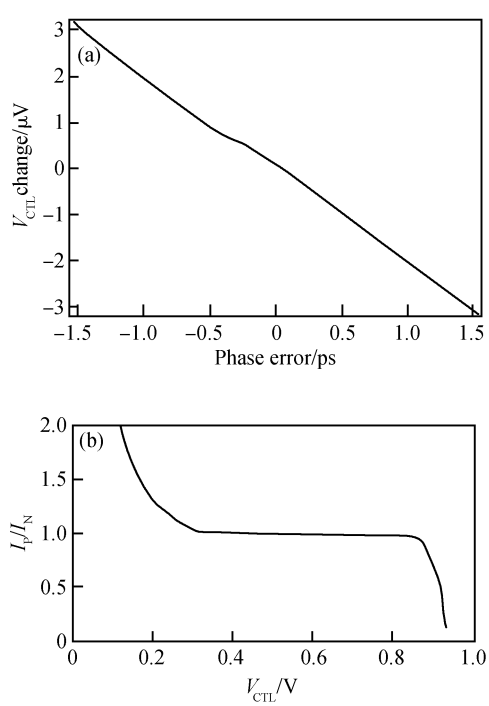

Fig. 5　(a) Relationship between V_{CTL} change and phase error; (b) I_P/I_N changes with V_{CTL}

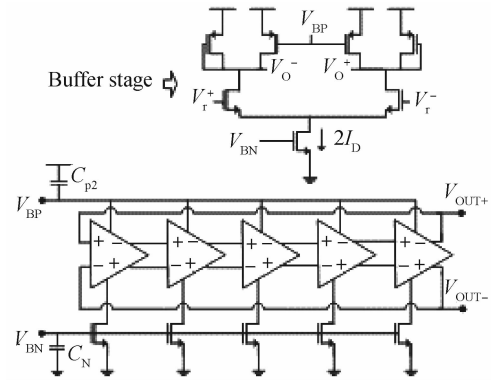

Fig. 6　VCO circuit

in the time domain. We adopt some design methods to minimize the VCO phase noise based on Hajimiri and Lee's theory[5,6]. Lee and Hajimiri[6] point out that the phase noise in differential oscillators grows with the number of stages and the phase noise in single-end oscillators is independent of the number of stages for a given power dissipation. We still choose a differential topology because it is immune to power/ground noise. The structure of the VCO is shown in Fig. 6. Two capacitors have been added to the V_{BN} and V_{BP} nodes to reject supply/substrate noise. V_{OUT+} and V_{OUT-} are the VCO output signals. Reducing the number of VCO stages achieves better phase noise performance, but results in a lower oscillating amplitude that is easily disturbed by outer noise sources. Therefore, a five stage VCO is chosen for proper phase noise performance and output frequency range. We adjust the transistors' size in each buffer stage to have a linear load resistor and a better P/N ratio, because better waveform symmetry can prevent low frequency noise from transferring to the frequency range near the oscillating frequency. For fully correlated noise sources, only noise around N time oscillating frequency could influence the VCO output signal phase[6]. Therefore, symmetry and compactness are important in VCO layout design.

3.4　Loop filter

Digital processes do not provide high-density linear capacitors and polysilicon resistors, but they are abundant in metal layers. Using the MOS transistors' parasitic capacitor as the loop filter capacitor is an option, but it creates leakage current that will cause jitter on the VCO output signal. However, the metal parasitic capacitor is a low cost choice, shown in Fig. 7. The crossed area between the metal wires connected to nodes A and B should be as large as possible to obtain large capacitance in the limited area. The left side of Fig. 7 denotes capacitances between the same metal layers and the right side denotes the inter-

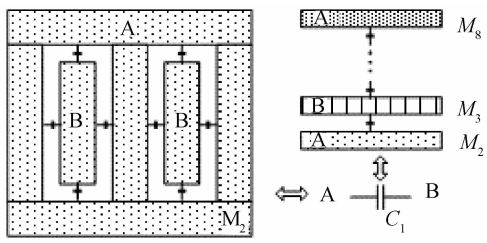

Fig. 7 Metal parasitic capacitance

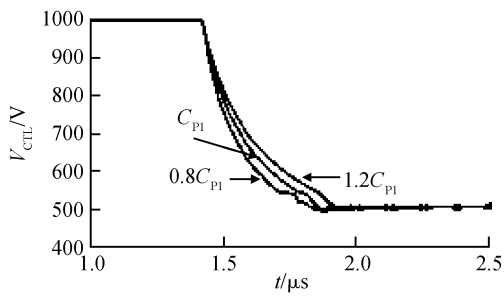

Fig. 8 Transient simulation results of the V_{CTL} signal

layer capacitances. Interlayer capacitances in digital technologies may experience process variances as high as 20%[3]. However, Eqs. (8～11) indicate that the stability of the self-biased PLL is not very sensitive to the variance of C_P. Figure 8 shows the transient simulation results of the V_{CTL} signal in the PLL's startup and the lock acquisition processes. The PLL's stability is acceptable when the capacitor C_{P1} value varies 20%.

3.5 Lock detect circuit

When PLL is locked, up and down pulses are narrower than the delay time value. The lock detect circuit detects these narrow pulses and counts for some update (reference) periods, then produces a high voltage signal, as shown in Fig. 9.

3.6 Startup circuit

When power is on, the VCO cannot start oscillating because the control voltage (V_{CTL}) signal is on power voltage. So a startup circuit is needed to pull the V_{CTL} down to near half the power voltage where the VCO can start oscillating. In Fig. 10, MOS transistors s1, s2, and s3 are used as switches. When the START signal voltage is low, s2 is turned on and s1 and s3 are turned off. When the START signal voltage changes from low to high, s2 is turned off and s1 and s3 are turned on. Then the V_{CTL} signal voltage is

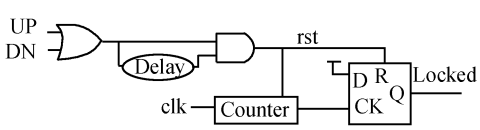

Fig. 9 Lock detect circuit

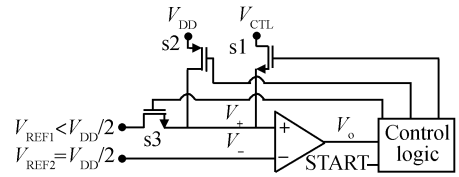

Fig. 10 Startup circuit

pulled down by V_{REF1} until the V_+ voltage is lower than $V_{DD}/2$. This process is shown in Fig. 8. After this process, the V_O signal voltage changes from high to low and the switch s1 is turned off. The PLL is enabled to start the lock acquisition process.

4 Layout design

The PLL was fabricated in a 90nm CMOS digital process and the layout area is 213μm × 212μm. The layout shape is rectangular and can easily be used as an IP in large digital systems. Decap capacitors are inserted into the margin of the main sub layouts and below the metal parasitic capacitors. In order to minimize the influence of switch noise in digital circuits, the layout is divided into analog and digital parts, as shown in Fig. 11. The VCO, charge pump, and loop filter belong to the analog part and have an independent power supply. The power grid covers the PLL devices. Moreover, the distance between VCO buffer stages should be minimized and kept symmetrical to maximize the correlation of the noise from the substrate and supply perturbations[6]. The orientation of each stage and the shape and length of connecting wires between buffer stages are identical. Dummy MOS transistors are added to give each stage identical load capacitance.

5 Test results

Jitter is the key performance of the PLL as a

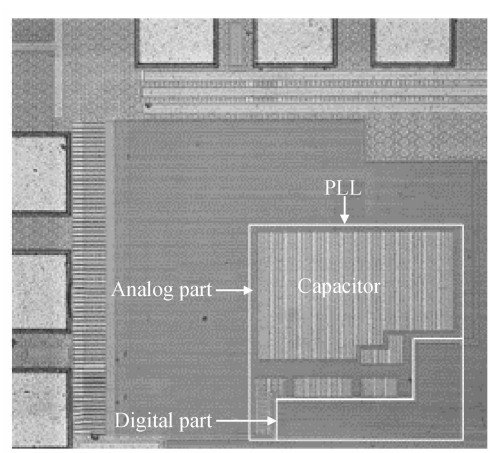

Fig. 11 Die micrograph of the PLL

Table 1　Jitter performances

Input /MHz	Output /MHz	Pk-pk jitter/ps	RMS jitter/ps	Input /MHz	Output /MHz	Pk-pk jitter/ps	RMS jitter/ps
30	450	36.6	4.57	100	1800	13.19	2.13
30	720	23.52	3.32	150	300	37.02	5.81
30	960	19.06	2.89	150	2100	33.37	4.51
50	600	19.74	2.82	150	2700	16.46	2.36
50	1000	20.24	2.73	200	400	28.15	4.16
50	1600	21.69	3.38	200	1000	17.55	2.82
100	400	27.61	4.3	200	1200	16.3	2.43
100	1000	18.91	3.24				

clock generator. We test the PLL output signal's jitter performance using an arbitrary waveform generator, power supply, and oscilloscope. Jitter results are computed by TDSJIT3 jitter analysis software inner oscilloscope. The jitter performance of some typical input/output signals' frequency is shown in Table 1. The input/output ports in Table 1 is the F_{REF}/F_{OUT} signal in Fig. 2 and the output frequency is controlled by the divider ratio N. Figure 12 shows that the RMS jitter is 3.7977ps and the peak-to-peak jitter is 32.225ps when the VCO output signal's frequency is locked on 1.989GHz. Figure 13 shows the startup process. The low pulse represents when the V_{CTL} signal is being pulled down. After 1.68μs, the PLL is locked and the "locked signal" changes to high. The PLL bandwidth is acquired by analyzing the output signal's spectrum[7]. As shown in Fig. 14, the PLL bandwidth

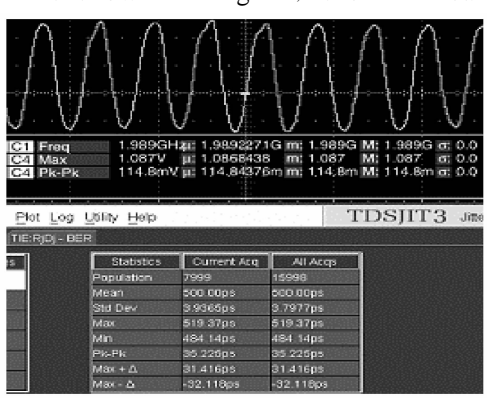

Fig. 12　Jitter testing result

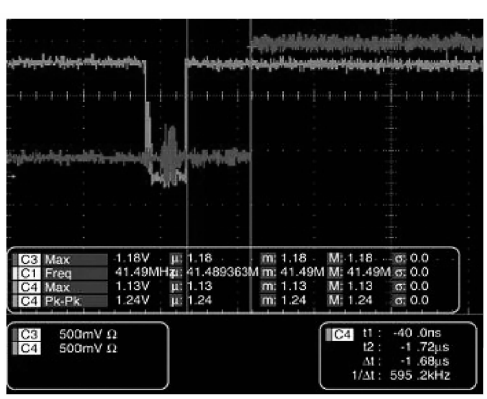

Fig. 13　Startup process

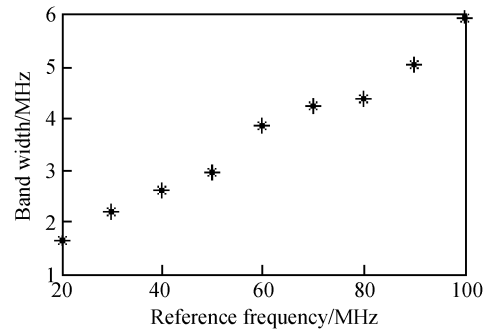

Fig. 14　PLL bandwidth

Table 2　PLL performance summary

Process technology	90nm CMOS
Supply voltage	1.0V
Die size	213μm ×212μm
Reference frequency	25 ～200MHz
Output frequency	125MHz～2.7GHz
Multiplication factor	2～32
Period jitter	3.7977ps$_{rms}$, 32.225ps$_{pk\text{-}pk}$@1.989GHz
Power dissipation	9mW@2GHz

tracks the reference frequency so that low jitter performance is achieved. The overall PLL performance is summarized in Table 2.

6　Conclusion

This PLL is fabricated in a new emergent digital process, which does not provide a high-density linear capacitor. Using metal parasitic capacitance is a low cost solution for PLL IP in a large digital system. Low jitter performance and a wide output frequency range are achieved at moderate power consumption.

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用 90nm CMOS 数字工艺实现的低抖动时钟锁相环设计

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摘要：用 90nm CMOS 数字工艺设计实现了一个低抖动的时钟锁相环. 锁相环不需要“模拟”的电阻和电容，采用金属间的寄生电容作为环路滤波器的电容. 测试结果显示，锁相环锁定在 1.989GHz 时的均方抖动为 3.7977ps，周期峰峰值抖动为 31.225ps，核心功耗约为 9mW. 锁相环可稳定输出的频率范围为 125MHz 到 2.7GHz.

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