Using 3D TCAD Simulation to Study Charge Collection of a p-n Junction in a 0.18μm Bulk Process

Liang Bin†, Chen Shuming, and Liu Biwei

(*Computer School, National University of Defense Technology, Changsha* 410073, *China*)

Abstract: Single event transient of a real p-n junction in a 0.18μm bulk process is studied by 3D TCAD simulation. The impact of voltage, temperature, substrate concentration, and LET on SET is studied. Our simulation results demonstrate that biases in the range 1.62 to 1.98V influence DSET current shape greatly and total collected charge weakly. Peak current and charge collection within 2ns decreases as temperature increases, and temperature has a stronger influence on SET currents than on total charge. Typical variation of substrate concentration in modern VDSM processes has a negligible effect on SEEs. Both peak current and total collection charge increases as LET increases.

Key words: charge collection; p-n junction; very deep sub-micro; 3D device simulation; radiation
EEACC: 2550
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2008)09-1692-06

1 Introduction

When alpha particles emitted from packaging materials and heavy ions in space (e.g., galactic cosmic rays) strike off-biased drain junctions of transistors, single event effects (SEEs) such as single event upset (SEU), digital single event transient (DSET), and multi-bit upset (MBU) may originate. Solutions to harden devices to SEEs require an in-depth understanding of the basic mechanisms responsible for charge collection. A p-n junction is a basic element to construct more complex transistors and the charge collection of p-n junctions has always been a focus in the field of radiation effects.

Measuring the single event transient (SET) current induced by heavy ions striking a simple p-n junction by numerical simulation or heavy ion tests has been proven to be useful for investigating charge collection. Much research has been done on charge collection of a simple p-n junction in standard bulk or epitaxial processes. The influences of bias voltages[1~3], linear energy transfer (LET)[2,3], substrate concentration[1~4], temperature[5,6], minority carrier lifetime[1], species and energy of incident ions[2,7,8], and ion track structure[3] on SET current pulses and charge collection have been widely investigated. However, earlier studies have many weaknesses, including: (1) SET current measured by the heavy ion test has a non-negligible error compared to the actual one generated in circuits due to insufficiently short system response time and the relatively large capacitance of the oscilloscope probe. A typical scope probe capacitance will overload minimum geometry device drive current so it is essentially impossible to directly measure the transient in deep submicron technology[9]. (2) Large devices have been used widely for earlier research, for example, p-n junctions of tens of micrometers diameter has been used in Refs. [2,3,5,6,8], and even larger p-n junctions with 1mm diameter have been used in Ref. [7]. However, in very deep sub-micro (VDSM) processes, the dimensions of the widely used devices are much shorter, with typical width and length less than a few micrometers. (3) The thickness of the epitaxial layer is much larger than that of modern VDSM processes. Earlier investigation used 4 to 20μm thick epitaxial layers[5~7], while the epitaxial thickness of a typical VDSM process is less than 2μm. (4) In previous 3D device simulations, bottom substrate contacts were widely used, but it was demonstrated that there are notable differences for SET currents with bottom and top contacts[10]. (5) Very high bias voltages were used, for example, bias voltages from 5 to 32.5V in Ref. [2], 5V in Refs. [3,4], 3 to 10V in Refs. [5,6], and 10V in Ref. [8], which are much higher than the nominal voltages in VDSM process.

Recent validation studies have proven that the predictions of 3D simulators can be highly accurate[11]. In this paper, heavy ion induced SET current in a p-n junction of a 0.18μm standard bulk process has been investigated by 3D device simulation. In our work, insufficiencies in previous studies have been avoided. We did not use a simple abrupt p-n junction

† Corresponding author. Email: liangbin@nudt.edu.cn
Received 10 January 2008, revised manuscript received 7 May 2008

but a real one generated by process simulation and calibration. We used top substrate contact, trim devices, and bias voltages near the nominal voltage in a typical 0.18μm process.

In the remainder of this paper, we first introduce the device structure used in our work and describe the primary physical models and parameters used in device simulation. We then analyze the impacts of voltage, temperature, substrate concentration, and LET on SET current separately. Finally, we draw the crucial conclusions of our work.

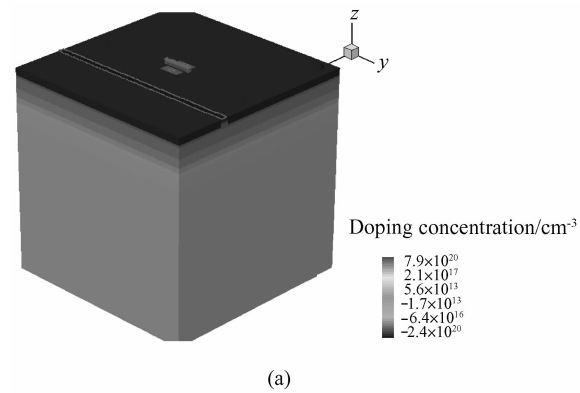
2 Experiment

For our study of SET current of a p-n junction, we used Sentaurus TCAD V2007.03 from Synopsys. Sentaurus TCAD is a widely used process and device simulator. All simulations were conducted using the YINHE computing cluster. The dimensions of the simulation structure are 10μm×10μm×10μm, and the device contains about 165,000 grid points. The average duration of the 3D device simulation was around 2 days by double threads with 3GHz CPU frequency. For all simulations, the following physical models were used: (1) Fermi-Dirac statistics, (2) band-gap narrowing effect, (3) doping dependent SRH recombination and Auger recombination, (4) temperature, doping, electric filed, and carrier-carrier-scattering impacts on mobility, (5) incident heavy ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 0.1μm and a Gaussian temporal profile with a characteristic decay time of 250fs.

The technology modeled in this work is a 0.18μm bulk CMOS process manufactured by SMIC foundry. We first calibrated the doping profiles within the 3D nMOS model by process simulation and an inverse modeling approach[12,13] and then used the drain-substrate junction of the calibrated nMOS model for our work in this paper. The 3D nMOS model was validated before the actual device simulations. For the 3D nMOS model and spice model provided by SMIC, we obtained good agreement with the *I-V* characteristics. Figure 1 (a) is the calibrated 3D nMOS model and Figure 1 (b) is the section of the drain junction used in our work. The junction depth of the drain junction is about 140nm, the peak concentration of the n^+ drain is $5.1\times10^{20}\,cm^{-3}$, and the width of the drain is about 0.6μm.

3 Bias dependence of SET current

In this section, bias dependence of the SET current has been investigated under two LETs of 30 and



(a)

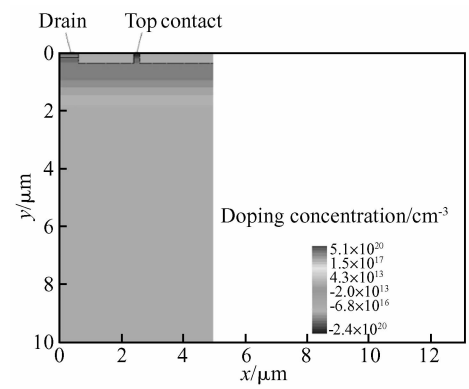


Fig.1　(a) Calibrated 3D nMOS model; (b) Section of the drain junction

5MeV·cm^2/mg. The bias voltages used in our work are between 1.62 and 1.98V (1.8V±10%), which is the normal voltage range of an SMIC 0.18μm standard bulk process.

Figure 2 (a) shows that as the bias voltage increased from 1.62 to 1.98V, the peak current increased from 6.36 to 7.23mA under LET of 30MeV·cm^2/mg, and the relative increase is about 12.0%. Charge collected within 2ns increased from 430.5 to 433.5fC, and this increase is negligible.

As illustrated in Fig. 2 (b), under LET of 5MeV·cm^2/mg, the peak current increased from 2.80 to 3.09mA and the relative increase is about 10.4%. Charge collected within 2ns increased from 50.4 to 50.5fC, and this increase is also negligible.

Our simulations indicate that bias distinctly influences SET current shape and has a very weak influence on total charge collected in the 1.62 to 1.98V range. The peak of the SET current is dominated by charge collection through funnel-assisted drift, and bias voltage has an important impact on carrier velocity and drift. Therefore, the peak current increased markedly as bias increased.

However, it is diffusion but not drift that determines the total collected charge, due to the much shorter duration of funnel-assisted drift over diffusion. In typical VDSM processes, funnel-assisted drift

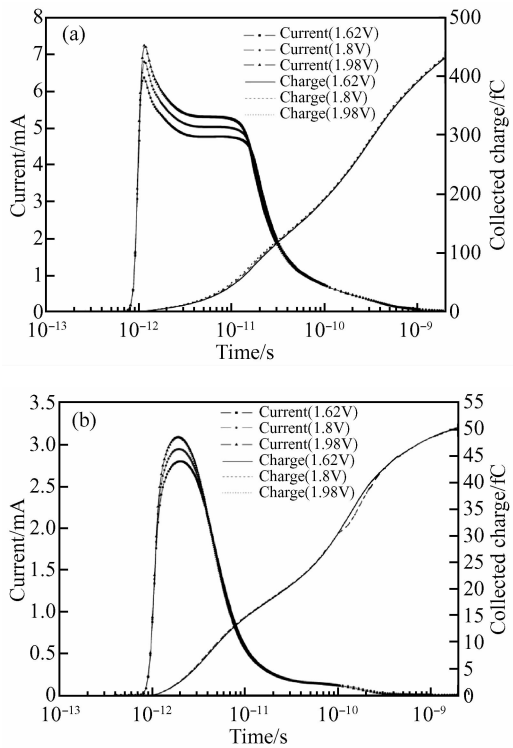


Fig. 2 Influence of bias voltages on SET current and total charge collected within 2ns under LET of 30MeV · cm^2/mg (a) and 5MeV · cm^2/mg (b)

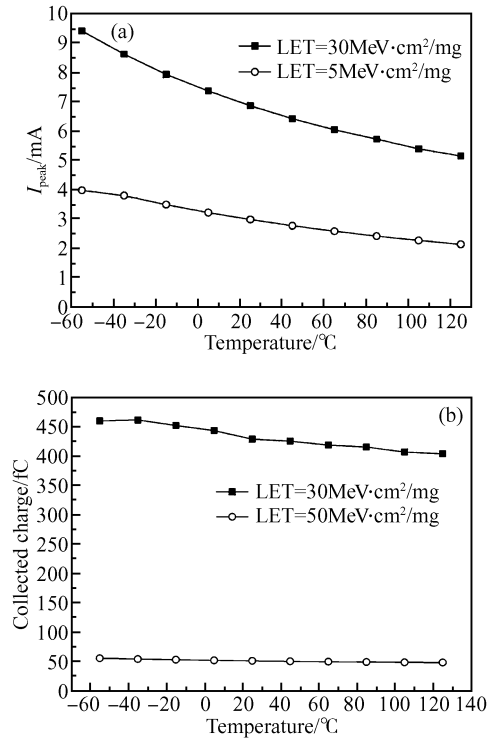


Fig. 3 Temperature dependence of peak current (a) and total charge collected within 2ns (b)

collection lasts about tens of picoseconds. Bias voltage has an inconspicuous effect on diffusion and on total charge[1]. The tendency of total charge with voltage in our work is consistent with Ref. [1] but conflicts with earlier experimental results in Ref. [2]. It was shown in Ref. [2] that total charge collected increased with increasing bias. This contradiction is probably due to the different biases used. Biases used in Ref. [2] were from 5 to 32.5V. The depletion region is very wide under those high biases and much charge was collected by drift. In our work and Ref. [1], the bias was much lower and charge collection was mostly due to diffusion.

4 Temperature dependence of SET current

In this section, temperature dependence of SET current has been studied under LET of 30 and 5MeV · cm^2/mg. The temperature simulated in our work is from −55 to 125℃, which is the temperature range enforced by the typical military standard.

Temperature dependence of peak current has been illustrated in Fig. 3 (a). When temperature increased from −55 to 125℃, peak current decreased from 9.4 to 5.1mA under LET of 30MeV · cm^2/mg and the relative decrease is 45.7%. Under LET of 5MeV · cm^2/mg, peak current decreased from 4.0 to 2.1mA and the relative decrease is 47.5%.

As shown in Fig. 3 (b), total charge collected within 2ns decreased from 460 to 404fC under LET of 30MeV · cm^2/mg, and the relative decrease is 12.2%. Under LET of 5MeV · cm^2/mg, total charge decreased from 55.0 to 47.7fC and the relative decrease is 13.3%.

Our work indicates that both peak current and total charge collected within 2ns decreases as temperature increases and temperature has a more significant impact on peak current than on total charge. Our conclusions about the temperature dependence of the peak current are consistent with Refs. [5, 6]. Peak current is proportional to carrier velocity, which itself is a complex function of mobility and electric field. As temperature increases, carrier mobility decreases and results in a lower peak current.

With regard to temperature dependence of the total charge, simulation results in our work are in slight disagreement with the experimental results in Ref. [6]. Reference [6] demonstrated that total charge remains nearly constant with temperature. However, the variance of the measured charge values in Ref. [6] is about 10%, and it can be considered approximately that our conclusion agrees with [6] within this error.

Furthermore, the authors of Ref. [6] assumed that the total charge will increase slightly as temperature increases due to band-gap narrowing. Our work

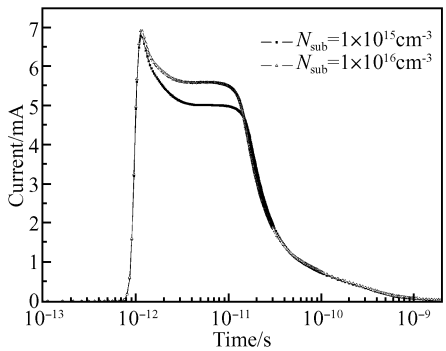


Fig. 4　Influence of substrate concentration on SET current

negated this assumption in Ref. [6]. In fact, total charge is determined both by charge deposition of incident ions and charge collection efficiency. Although charge deposition increases as temperature increases because of band-gap narrowing, charge collection efficiency due to drift and diffusion is also influenced by temperature.

As temperature increases, carrier mobility decreases and results in less charge collected by drift. To the first order, the amount of charge collected by diffusion depends on the minority carrier diffusion length L_p, which itself depends on the am-bipolar diffusion coefficient D^* and minority carrier lifetime τ. Due to contrary data on lifetime as a function of temperature, we cannot draw a conclusion about temperature dependence of charge collection by diffusion.

Since the minority lifetime depends strongly on the specific processing conditions, there is no generally acceptable law to describe its temperature dependence. Minority lifetime may increase, decrease, or stay constant as temperature increases. Thus, we predict that total charge will also increase, decrease, or stay constant as temperature increases for different manufacturing processes.

Nevertheless, both our simulation results and the experimental results in Ref. [6] indicate that the influence of temperature on total collection charge is not significant.

5　Influence of substrate concentration on SET current

In this section, the influence of substrate concentration on SET current has been researched. Lightly-doped substrate of $1\times10^{15}\,cm^{-3}$ and moderately-doped substrate of $1\times10^{16}\,cm^{-3}$ has been simulated in this paper. We obtained two p-n junctions by process simulation, and all processes were the same except for initial substrate concentration. SET currents of the two p-n junctions under LET of 30MeV · cm^2/mg and 1.8V bias voltage has been illustrated in Fig. 4. Peak currents of slightly-doped and moderately-doped substrates were 6.79 and 6.92mA, respectively, and the peak current of moderately-doped substrate was a little higher (about 1.9%) than that of slightly-doped substrate.

Charge collections within 2ns have been obtained by integration of the SET currents. Total charge collected was 495fC for moderately-doped substrate and 432fC for slightly-doped substrate. When the substrate concentration increased from 1×10^{15} to $1\times10^{16}\,cm^{-3}$, the total charge increased about 6.3%.

Simulation results in our work demonstrated that peak current decreases slightly as the substrate concentration increases. Our conclusions agree with Ref. [1] but conflict with Ref. [2]. Reference [2] suggests that peak current decreases as the substrate concentration increases because: (1) The depletion region become narrower as the substrate concentration increases and less charge is deposited in the depletion region. (2) The funnel process is controlled by the dielectric relaxation time of the semiconductor, which is proportional to the substrate resistivity. The collapse of the funnel in moderately-doped substrate is faster than that of slightly-doped substrate. (3) Minority mobility decreases as the substrate concentration increases.

Although most factors have been considered in Ref. [2], electric field was ignored. The depletion region becomes narrower as the substrate concentration increases and the voltage drop across the depletion region remains constant, resulting in a stronger electric filed in the depletion region. It is the stronger electric filed that accounts for the higher peak current in moderately-doped substrate.

Very high bias voltages have been employed in Ref. [2], and the electric field in the depletion region was very strong even with slightly-doped substrate. The velocity of the carriers was therefore saturated or near saturated and the stronger field has a negligible effect on carrier velocity. While in our work and Ref. [1], the biases were much lower and the electric field had a remarkable effect on carrier velocity. To summarize, peak current is related not only to depletion width and charge deposited in the depletion region, but also to electric field.

Previous studies have demonstrated that total collection charge decreases as the substrate concentration increases[1~4], but our simulation results show a different tendency. This contradiction is probably due to the shorter collection time in our work. The collection time in earlier investigations was mostly larger than 100ns compared to 2ns in our work. In fact, there were similar results in Ref. [3]. It was demonstrated

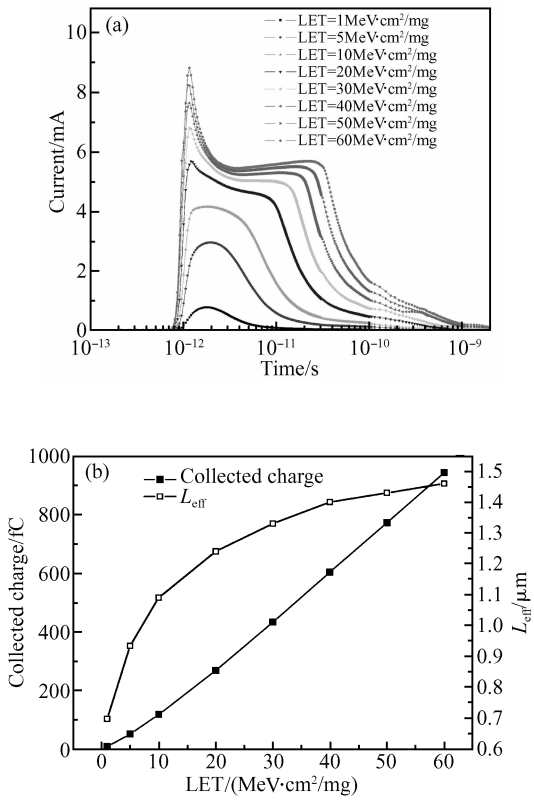


Fig. 5 SET currents (a) and total collection charge and effective collection depth (b) under different LETs

in Ref. [3] that although total charge decreases as substrate concentration increases, the charge collection in 200ps is larger for moderately-doped substrate than for lightly-doped substrate.

If we increase the simulation time, we may obtain results consistent with Refs. [1～4]. We are only concerned with charge collection within 2ns because the duration of most SEEs is less than 2ns.

In our work, peak current and total collection charge increases as the substrate concentration increases, but the extent is quite small. The typical substrate resistivity for modern VDSM process is 8 to 12Ω · cm, and the corresponding concentration is 1.73×10^{15} to $1.14\times10^{15}\,cm^{-3}$, which is within the range studied in this paper. We conclude that for modern VDSM processes, the typical variation of substrate concentration has a negligible effect on SEEs.

6 Influence of LET on SET current

The influence of LET on SET currents has been investigated within the 1 to 60MeV · cm^2/mg range. SET currents under different LETs are illustrated in Fig. 5 (a), and charge collection and effective collection depth are depicted in Fig. 5 (b). Both peak current and total charge increase as LET increases due to an increase in charge deposited along the ion track[2].

Interestingly, the SET current shape changes as LET increases. SET current has one peak below LET of 10MeV · cm^2/mg, while it has two peaks above 20MeV · cm^2/mg. The second peak may due to carrier-carrier scattering, and similar phenomena were observed in Ref. [14] by device simulation with a single nMOS transistor.

Dividing total charge by charge deposited in unit length, effective collection depth L_{eff} is obtained. L_{eff} is 0.7μm under LET of 1MeV · cm^2/mg, which is consistent with the depth of p-well implantation in our calibrated process. L_{eff} increases as LET increases, illuminating that charge deposited out of the p-well can also be collected. When LET continues to increase, L_{eff} saturates gradually. L_{eff} is 1.5μm under LET of 60MeV · cm^2/mg, which agrees with the typical collection depths in modern VDSM processes[15].

7 Conclusion

Single event transient of a real p-n junction in a 0.18μm bulk process has been studied by 3D TCAD simulation. The impact of voltage, temperature, substrate concentration, and LET on SET currents has been widely studied.

Our simulation results demonstrate that the biases within the 1.62 to 1.98V range have distinct influences on DSET current shape and very weak influences on total charge collected. Peak current and charge collection within 2ns decrease as temperature increases, and temperature has a stronger influence on SET currents than on total charge. The typical variation of substrate concentration in modern VDSM processes has a negligible effect on SEEs. Both peak current and total collection charge increases as LET increases. Charge collection depth L_{eff} is 0.7μm under LET of 1MeV · cm^2/mg. As LETs continue to increase, charge collection depth increases and gradually saturates with L_{eff} of 1.5μm under LET of 60MeV · cm^2/mg.

References

[1] Abadir G B, Fikry W, Ragai H F, et al. A device simulation and model verification of single event transients in n^+p junctions. IEEE Trans Nucl Sci, 2005, 52(5): 1518

[2] Heileman S J, Eisenstadt W R, Fox R M. CMOS VLSI single event transient characterization. IEEE Trans Nucl Sci, 1989, 36(6): 2287

[3] Dussault H, Howard J W, Block R C, et al. Numerical simulation of heavy ion charge generation and collection dynamics. IEEE Trans Nucl Sci, 1993, 40(6): 1926

[4] Dodd P E, Sexton F W, Winokur P S. Three-dimensional simulation of charge collection and multiple-bit upset in Si devices. IEEE Trans Nucl Sci, 1994, 41(6): 2005

[5] Laird J S, Hirao T, Onoda S, et al. Temperature dependence of heavy ion induced current transients in Si epilayer devices. IEEE

Trans Nucl Sci,2002,49(3):1389
[6] Guo G,Hirao T,Laird J S,et al. Temperature dependence of single event transient current by heavy ion microbeam on p+/n/n+ epilayer junctions. IEEE Trans Nucl Sci,2004,51(5):2834
[7] Onoda S,Hirao T,Laird J S,et al. Transient currents generated by heavy ions with hundreds of MeV. IEEE Trans Nucl Sci,2006,53(6):3731
[8] Dussault H,Howard J W,Block R C,et al. High energy heavy-ion-induced single event transients in epitaxial structures. IEEE Trans Nucl Sci,1994,41(6):2018
[9] Benedetto J,Eaton P,Avery K,et al. Heavy ion-induced digital single-event transients in deep submicron processes. IEEE Trans Nucl Sci,2004,51(6):3480
[10] Turowski M,Raman A,Jablonski G. Mixed-mode simulation and analysis of digital single event transients in fast CMOS ICs. 14th International Conference on Mixed Design of Integrated Circuits and Systems,2007:433
[11] Dodd P E,Shaneyfelt M R,Horn K M,et al. SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments. IEEE Trans Nucl Sci,2001,48(6):1893
[12] Turowski M,Raman A,Jablonski G. Mixed-mode simulation and analysis of digital single event transients in fast CMOS ICs. 14th International Conference on Mixed Design of Integrated Circuits and Systems,2007:433
[13] Amusan O A,Witulski A F,Massengill L W,et al. Charge collection and charge sharing in a 130nm CMOS technology. IEEE Trans Nucl Sci,2006,53(6):3253
[14] Kobayashi D,Saito H,Hirose K. Estimation of single event transient voltage pulses in VLSI circuits from heavy-ion-induced transient currents measured in a single MOSFET. IEEE Trans Nucl Sci,2007,54(4):1037
[15] Mavis D G,Eaton P H. SEU and SET modeling and mitigation in deep submicron technologies. IEEE 45th Annual International Reliability Physics Symposium,Phoenix,2007:293

0.18μm 工艺下 p-n 结电荷收集的三维 TCAD 模拟

梁　斌†　陈书明　刘必慰

（国防科技大学计算机学院，长沙　410073）

摘要：采用三维 TCAD 模拟的手段，针对 0.18μm 工艺下的真实 p-n 结，研究了偏压、温度、衬底掺杂浓度和 LET 对辐射诱导的 SET 电流脉冲的影响.研究结果表明，在 1.62～1.98V 的范围内，偏压对电流脉冲的形状有明显影响，而对 2ns 内的电荷收集总量几乎没有影响；电流脉冲峰值和 2ns 内的电荷收集总量均随着温度的增加而降低，但温度对电流脉冲峰值的影响更大，而对电荷收集总量的影响相对较小；在典型的现代工艺条件下，衬底掺杂浓度的起伏对单粒子加固性能的影响基本可以忽略；电流脉冲的峰值和电荷收集量二者均随着 LET 的增加而增加.

关键词：电荷收集；p-n 结；超深亚微米；三维器件模拟；辐射
EEACC：2550
中图分类号：TN386　　**文献标识码**：A　　**文章编号**：0253-4177(2008)09-1692-06

† 通信作者.Email:liangbin@nudt.edu.cn
2008-01-10 收到，2008-05-07 定稿