A Monolithic InGaP/GaAs HBT Power Amplifier Design with Improved Gain Flatness

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Abstract: A monolithic power amplifier designed for 3GHz communication applications with improved gain flatness is studied based on InGaP/GaAs hetero-junction bipolar transistor technology in a commercial foundry. To improve gain flatness in a simple way, no external component was used in the real circuit except the decoupled bypass capacitors and RF choke. The measured linear gain is 23dB with gain flatness of ±0.25dB, satisfying the design goal and matching well with simulation results. This 2-stage power amplifier can deliver 31dBm linear output power and 44% power-added efficiency in the 400MHz bandwidth. The successful design with improved gain flatness is the result of superior distortion compensation and a coil model used as the RF choke.

Key words: power amplifier; MMIC; HBT
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1 Introduction

Recently, monolithic microwave integrated circuit (MMIC) low noise amplifiers (LNA), MMIC voltage controlled oscillators (VCO), and MMIC mixers with CMOS technology have been reported with excellent performances. However, CMOS technology is still limited for high efficiency power amplifiers (PA). Moreover, the recent advancement InGaP/GaAs hetero-junction bipolar transistor (HBT) technology is promising for superior device performance, such as high output power, high efficiency, and high linearity[1]. Therefore, HBT technology is remarkably attractive for modern digital communication, portable phone applications, and radar systems.

In this work, a monolithic power amplifier was designed and implemented in a commercial foundry, with improved gain flatness. The measured linear gain is 23dB with a gain flatness of ±0.25dB, achieving the design goals and matching well with simulation results. This 2-stage power amplifier can deliver 31dBm linear output power and 44% power-added efficiency (PAE) in the 400MHz bandwidth. The successful design with improved gain flatness is the result of superior distortion compensation and a coil model used as the RF choke.

2 Device fabrication

The InGaP/GaAs HBT power device in this paper has an emitter width of 2μm and an emitter length of 20μm. This emitter can endure 40mA typical operation current with 160mA maximum current. The emitter current density is 25mA/μm^2 for a 5V emitter supply. The breakdown voltage of the device is 10.4V and the offset voltage is 0.1V. The section plane view schematic of InGaP/GaAs HBT structure grown by MOCVD is shown in Fig. 1 and Fig. 2. The n^+ InGaAs contact layer, the n^+ InGaAs graded cap layer, the n^+ GaAs cap contact layer, and the n InGaP emitter layer make up the emitter layer. The base layer is the p^+ GaAs base layer. There are three layers with the collector layer, including the n^- GaAs collector layer, the n^+ GaAs subcollector layer, and the GaAs substrate.

In order to increase reliability, an extra ballasting resistance of 5Ω with ballasting capacitors of 15pF is generally implemented in an InGaP/GaAs HBT power amplifier circuit. The fabricated first stage has 24

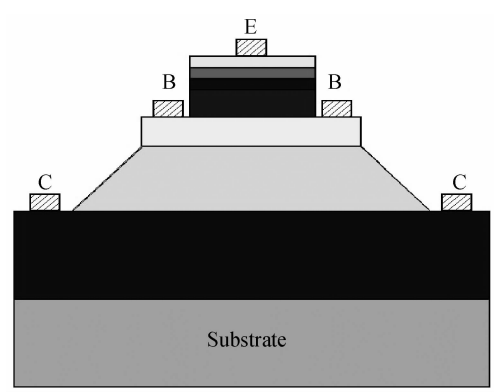

Fig. 1 Schematic cross-sectional view of an InGaP/GaAs HBT

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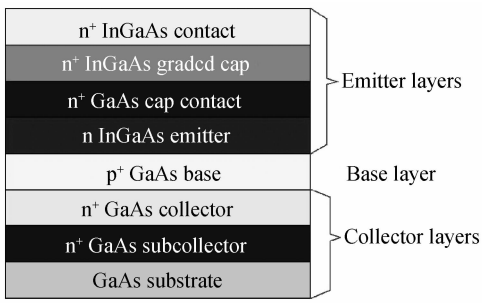

Fig. 2 Schematic structural view of an InGaP/GaAs HBT

fingers for the emitter and the second stage has 128 fingers. The total emitter area is $6080\mu m^2$.

3 Circuit design

Modulated signals for modern communication systems continuously vary in amplitude and phase, so any non-linear characteristics of the device, such as changes of base-collector capacitance and transconductance, will bring forth distortion to an ideal frequency spectrum[2,3]. Since a key characteristic of linear power amplifiers is gain flatness[4~6], a gain compression compensation circuit is employed to improve performance in this power amplifier design. An effective methods to improve the gain compression is to increase the base-emitter DC bias voltage slightly as the input power increases[7,8].

Here, an improved biasing circuit is shown in Fig. 3. In this improved biasing circuit, the input signal is amplified by HBT1, HBT2, and other passive components. The base of HBT2 is connected to the capacitor C_1 and the bias resistors R_1, R_2, and R_3. Then the HBT2 base-collector diode was forward biased. The V_{cap} (the voltage of the capacitor C_1, as shown in Fig. 3) was decreased by R_2 and R_3 to provide the base voltage of HBT2. When the input power increased, the DC voltage was changed by the capacitor with the base-collector diode of HBT2. Consequently, the base voltage of HBT1 slightly increased as the input power increased, and the gain compression and phase distortion improved.

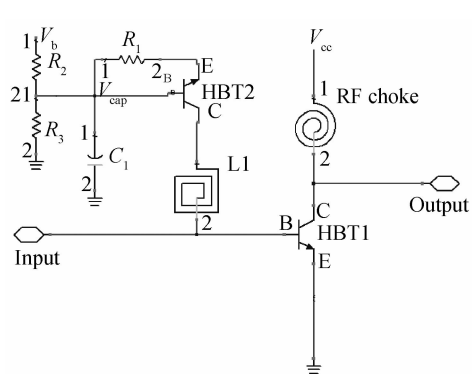

Fig. 3 Circuit topology of the improved integrated diode biasing circuit

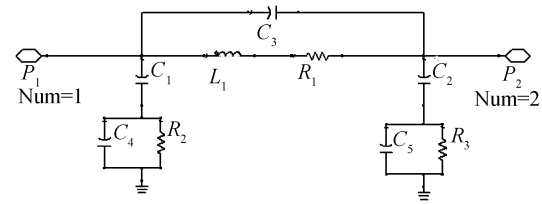

Fig. 4 Circuit topology of tradition coil model

4 RF choke analysis

The entire circuit of the InGaP/GaAs power amplifier was designed in an Agilent advanced design system (ADS) and simulated with Harmonic Balance by ADS. In simulation, there is an impractical phenomenon for application whereby the type of RF choke has no influence on the simulation result.

The off-chip RF choke had a large current (> 700mA), which was out of range of commercial components. Thus, we made a coil by ourselves. The tradition coil model is shown in Fig. 4. We extracted the improved T model equivalent circuit of coil from the measured *S*-parameters, as shown in Fig. 5.

The RLC values in the equivalent circuit shown in Fig. 5 were calculated based on *S*-parameter by ADS. The relationship between the quality factor of the inductor with arbitrary impedance load and *S*-parameter is:

$$Q_{\text{inductor}} = \{2\text{Im}(S_{11} + S_{22}|F|^2) + 4\text{Im}(S_{21})\text{Re}(F)\}/\{(1-|S_{11}|^2-|S_{21}|^2) + (1-|S_{22}|^2-|S_{12}|^2)|F|^2 - 2\text{Re}[(S_{11}S_{12}^* + S_{2122}^*)F^*]\}$$ where $F = \dfrac{S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$.

The *S*-parameter of the coil was simulated by momentum of ADS, while the L_{eff} and self resonance frequency (SRF) was calculated by the *S*-parameter of the equivalent single port network shown in Fig. 5[9].

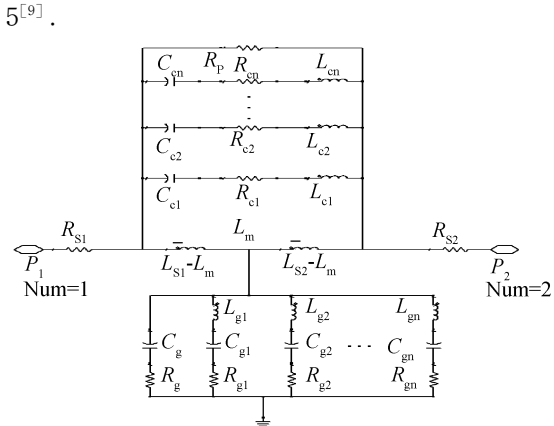

Fig. 5 Circuit topology of improved T model equivalent circuit of coil

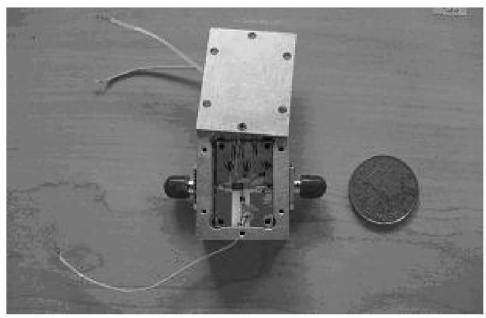

Fig. 6　Photo of the PA test module with one Yuan coin

When the inductor of the coil was tuned to the minimum gain flatness, the output impedance usually deviated from the conjugate-matched impedance. Therefore, there is a trade-off between the minimum gain flatness and the maximum output power, so that repeated adjustments are necessary. The designed RF choke consisted of a coil with a 3mm inner diameter and winding with a 20mil diameter.

5　Results

The power amplifier was installed on the specially designed test module shown in Fig. 6. Microstrip on substrate of 20mil Rogers4003 coupled the signal from the output of the monolithic to the test module. The measured module loss was from 1.7 to 2dB. The power amplifier demonstrated a small-signal gain of 23dB with gain flatness of ±0.25dB, as shown in Fig. 7. The bias was 5V on the input and output stages and corresponded to the drain current of 71.2 and 804.5mA, respectively. Figure 8 shows the output power and the big-signal gain versus input power curves and the corresponding power-added efficiency.

6　Conclusion

With improved gain flatness, a monolithic power amplifier using InGaP/GaAs hetero-junction bipolar transistor technology was investigated in this work. The measured linear gain is 23dB with a gain flatness of ±0.25dB, achieving the design goals and matching well with simulation results. This 2-stage power amplifier can deliver 31dBm of linear output power and 44% power-added efficiency in the 400MHz bandwidth. The successful design with improved gain flatness is due to the superior distortion compensation and the coil model used as the RF choke.

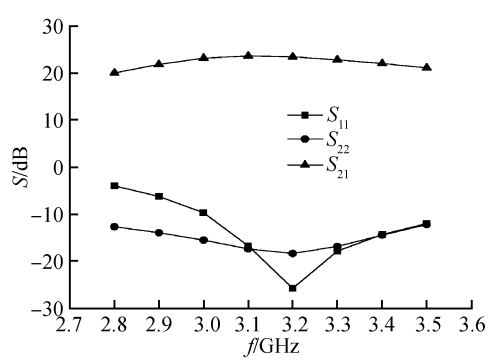

Fig. 7　Measured small-signal gain of the PA

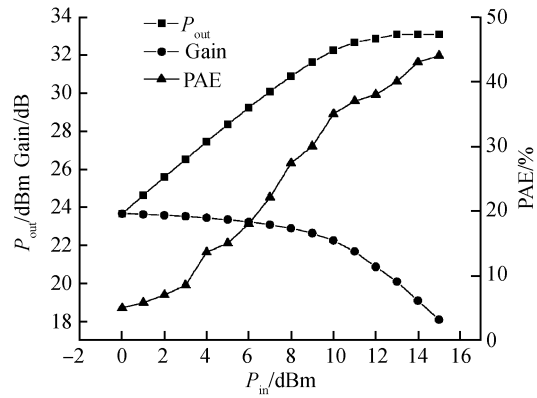

Fig. 8　Measured output power, PAE and the big-signal gain versus input power

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改善增益平坦度的新型 InGaP/GaAs HBT 功率放大器单片设计

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摘要：介绍了一款应用于 3GHz 通信的基于改进增益平坦度的功率放大器设计，其由商用 InGaP/GaAs 异质结双极性晶体管（HBT）工艺制作.为了以简单方式改善增益平坦度，除了耦合旁路电容以及射频扼流圈外，在实际电路中没有加入额外部件.其测量线性增益为 23dB，大信号增益平坦度为 ±0.25dB，非常贴近仿真和目标值.此两级功放 400MHz 带宽下的输出线性功率为 31dBm，增益附加效率为 44%.本电路通过良好的失真补偿电路和扼流圈模型的使用，成功地改善了增益平坦度.

关键词：功率放大器；MMIC；HBT

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