Design of a Bandgap Reference with a Wide Supply Voltage Range*

Sun Yueming, Zhao Menglian†, and Wu Xiaobo

(*Institute of VLSI Design, Zhejiang University, Hangzhou* 310027, *China*)

Abstract: An on-chip voltage reference with a wide supply voltage range is required by some applications, especially that of power management (PM) controller chips applied to telecommunication, automotive, lighting equipment, etc., when high power supply voltage is needed. Accordingly, a new bandgap reference with a wide supply voltage range is proposed. Due to the improved structure, it features a high power supply rejection ratio (PSRR) and high temperature stability. In addition, an auxiliary micro-power reference is introduced to support the sleep mode of the PM chip and reduce its standby power consumption. The auxiliary reference provides bias currents in normal mode and a 1.28V reference voltage in sleep mode to replace the main reference and save power. Simulation results show that the reference provides a reference voltage of 1.27V, which has a 3.5mV drift over the temperature range from −20 to 120℃ and 56μV deviation over a supply voltage range from 3 to 40V. The PSRR is higher than 100dB for frequency below 10kHz. The circuit was completed in 1.5μm BCD (Bipolar-CMOS-DMOS) technology. The experimental results show that all main expectations are achieved.

Key words: wide supply voltage range; bandgap reference; line regulation; sleep mode; micro power
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1 Introduction

Bandgap reference is widely applied in most analog and mixed signal integrated circuits (ICs). Since some ICs, especially PM ICs, work under a wide operating voltage range, typically 24V/48V in communication apparatus, 14V/42V in automobiles, and 3 to 40V in lighting such as LED equipment. Thus, a bandgap reference capable of operating with a wide supply voltage range is demanded in such applications.

As a voltage reference, the bandgap reference should provide a voltage independent of power supply and temperature. Moreover, high PSRR is also a critical feature since the power supply ripples will affect its stability[1] and influence its output reference voltage.

A typical bandgap reference contains two voltage sources with opposite temperature coefficients (TC) to compensate its temperature drift. The positive TC (PTC) voltage source consists of a transistor pair with different emitter areas. Their base-emitter voltage difference (ΔV_{BE}) is an ideal PTC voltage source. The voltage with negative TC (NTC) is derived from the forward voltages of pn junctions. By aboratively matching the opposite TCs of two voltage sources, accurate temperature compensation can be achieved over a certain range[2,3].

In the conventional topology, the offset voltage (V_{OS}) of the amplifier is a major error source and is unpredictable since it is a random error produced from dispersion during the manufacturing process[4]. Moreover, this structure restricts the operating supply voltage range because the common mode input voltage of the amplifier is limited[5]. The margin of the amplifier also restricts the PSRR.

In this paper, a novel bandgap reference structure is proposed. Different from conventional structures, its PTC voltage is directly generated by an inner amplifier. Moreover, the inner amplifier is supplied by a pre-regulated reference voltage, which guarantees its normal operation over a wide supply voltage range. It also effectively improves the PSRR and load regulation of the reference. The novel bandgap reference was implemented in 1.5μm BCD (bipolar-CMOS-DMOS) technology and verified by experimental results.

2 Proposed bandgap reference

Figure 1 shows a conventional bandgap reference and Figure 2 shows the complete schematic of the proposed bandgap reference. The reference is different from conventional one. It is composed of two parts: a micro-power reference and a power supply independent bandgap reference. It can be implanted in-

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† Corresponding author. Email: zhaoml@zju.edu.cn
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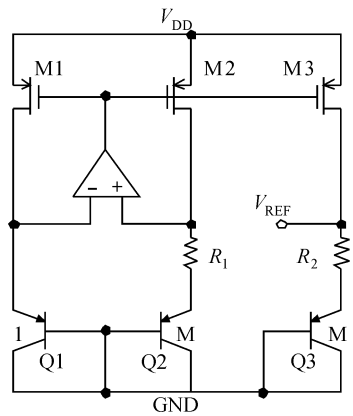

Fig. 1 Conventional bandgap reference

to a typical switch mode power supply (SMPS) controller IC. In addition, it supports the prevailing sleep-mode technique. When the controller is shut down, only the micro-power reference is active, providing a rough threshold voltage for the startup comparator. While the controller is working, the supply-independent bandgap reference will be activated to provide a more precise reference voltage.

2.1 Micro-power reference

This circuit has two characteristics: providing a primary reference voltage of 1.28V for the RUN comparator when the controller is in sleep mode and providing a PTAT current for the supply-independent bandgap reference and other circuit blocks when the controller is working. While working as the primary reference, its typical quiescent current is less than $10\mu A$, which makes it feature micro-power dissipation. By using transistors that can endure high voltage, it can be directly supplied by V_{IN}, which may vary from 3 to 40V.

The principle of this circuit is shown in Fig. 3.

Here, m is the ratio of the emitter areas of QA2 and QA1, α is the current gain of M1 ~ M3, and β is the current gain of M4 ~ M6. A resistor R_1 of several mega ohms determines the current I_A. The forward voltages of the base-emitter (V_{BE}) of QA1 and QA2 are:

$$V_{BE\_QA1} = V_T \ln \frac{I_{M2}}{I_{ss}} \tag{1}$$

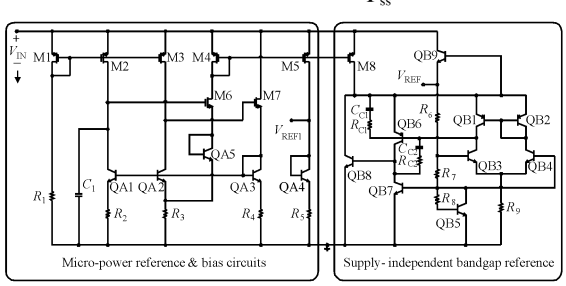

Fig. 2 Proposed supply-independent bandgap reference

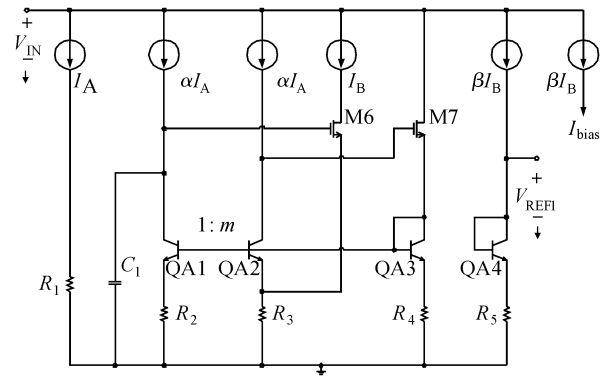

Fig. 3 Micro-power reference

$$V_{BE\_QA2} = V_T \ln \frac{I_{M3}}{m I_{ss}} \tag{2}$$

where $V_T = kT/q$, k is the Boltzmann's constant, q is the electron charge, T is the temperature in Kelvin (or absolute temperature), and I_{SS} is the reverse saturation current of the base-emitter junction of QA1.

Using the current mirror M1 ~ M3, the current I_{M2} and I_{M3} is:

$$I_{M2} = I_{M3} = \alpha I_A \tag{3}$$

Then the voltage across R_2 and R_3 becomes:

$$V_{R2} = I_{M2} R_2 = \alpha I_A R_2 \tag{4}$$

$$V_{R3} = (I_{M3} + I_{M4}) R_3 = (\alpha I_A + I_B) R_3 \tag{5}$$

Because QA1 and QA2 share the same base node, the base voltage is:

$$V_{BE\_QA1} + V_{R2} = V_{BE\_QA2} + V_{R3} \tag{6}$$

From Eqs. (1) ~ (5), we can derive:

$$R_3 I_B + \alpha I_A (R_3 - R_2) = V_T \ln m \tag{7}$$

Here, R_2 is equal to R_3. Thus, a proportional to absolute temperature (PTAT) current is obtained as:

$$I_B = \frac{V_T \ln m}{R_3} \tag{8}$$

Therefore, the output voltage of the micro-power voltage reference is:

$$\begin{aligned} V_{REF1} &= V_{BE\_QA4} + I_{PTAT} R_5 \\ &= V_{BE\_QA4} + \beta \frac{R_5 V_T \ln m}{R_3} \end{aligned} \tag{9}$$

where V_{BE_QA4} has a negative temperature coefficient. Thus, a stable reference voltage with a near zero temperature coefficient can be obtained by choosing appropriate values of β, R_3, R_5, and m.

Because the bias current I_A is generated by R_1, this reference does not need a startup circuit. Moreover, the accuracy of R_1 is not critical because the reference voltage does not depend upon I_A.

Transistors M7 and QA3 form a feedback loop to keep QA1 and QA2 working in the forward active region. If the supply voltage V_{IN} rises, the voltage across R_2 and R_3 will also rise, as well as the gate voltage of M7. Then the current flowing through M7 and QA3 rises too, pulling up the base voltage of QA3, QA1,

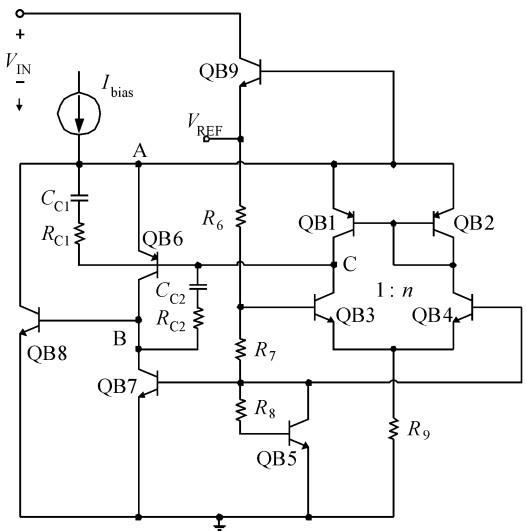

Fig. 4　Proposed supply-independent bandgap reference

and QA2. As a result, QA1 and QA2 keep their status in the forward active region. Transistor M6 works as a voltage controlled resistor. Because R_2 equals R_3, when supply voltage V_{IN} climbs up, the voltage variation over gate and source nodes of M6 is approximately equal. So the current flowing through M6 is not influenced by the supply voltage.

In the layout of this bandgap reference, R_5 is replaced by several trimmable resistors to achieve a precise predicted reference voltage after tape-outing.

2.2　Supply-independent bandgap reference

Using a unique structure to generate the reference voltage, the bandgap reference has good line regulation. Different from the micro-power reference above, it can supply a current up to 1mA, which is significant to the SMPS controller. In addition, this reference can be shut down in sleep mode to save power. The detailed circuit is shown in Fig. 4.

Usually, bipolar transistors have a smaller offset and higher gain than MOS transistors[6]. Thus, bipolar transistors are adopted as input differential pairs to reduce the offset and to provide a higher gain.

Here, the parameter n is the ratio of the emitter junction sizes of QB3 and QB4. I_{bias} is a bias current provided by the micro-power reference. Transistors QB1～QB4 and resistor R_9 constitute an OTA circuit. While working stably, the currents flowing through QB3, QB4 differential pairs will tend to be equal. Thus, the difference of the base-emitter voltage of QB3 and QB4 is:

$$\begin{aligned}\Delta V_{BE} &= V_{BE\_QB3} - V_{BE\_QB4} \\ &= V_T \ln\frac{I_{QB3}}{I_{ss}} - V_T \ln\frac{I_{QB4}}{nI_{ss}} = V_T \ln n \end{aligned} \tag{10}$$

The base nodes of QB3 and QB4 clamp the voltage drop across R_7, generating a PTAT current

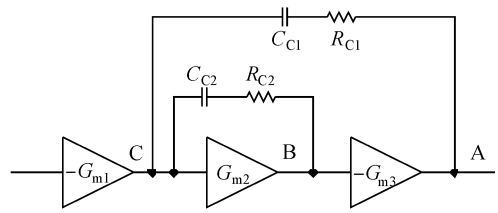

Fig. 5　Reversed nested Miller compensation

through R_7. The reference voltage includes two parts: the PTC voltage across R_6 and R_7, which is produced by the PTAT current, and the NTC voltage of V_{BE}.

$$\begin{aligned}V_{REF} &= V_{BE\_QB5} + \frac{\Delta V_{BE}}{R_7}(R_6 + R_7) \\ &= V_{BE\_QB5} + \frac{V_T \ln n}{R_7}(R_6 + R_7) \end{aligned} \tag{11}$$

Transistors QB6～QB9 constitute a feedback loop to stabilize the collector current of QB5. If this current falls, the voltage across R_7 will become smaller, which is amplified by the OTA. The base of QB6 is connected to the reverse output terminal of OTA; therefore, it also rises. Transistor QB7 is biased by QB5, so it always works in the forward active region. QB6 and QB7 can be regarded as a simple amplifier. Therefore, the voltage rising of the base of QB6 causes a significant reduction in the collector current of QB8 and then an increase in the base voltage of QB9. As a result, the current flowing through R_6, R_7, and QB5 rises and succeeds in compensating the initial current fluctuation. Thus, the current flowing through QB5 stabilizes.

Here transistor QB9 is the key component. It works in the forward active region. The current flowing through QB9 ensures the large current output ability of V_{REF} up to 1mA. In addition, because QB9 is forward biased, the voltage on node A equals the reference voltage plus V_{BE} (forward-biased diode voltage drop of QB9). It is about 2V in this design and is power supply-independent, ensuring the circuit can be supplied by a wide voltage range.

2.3　Frequency compensation

As mentioned above, the amplifier used to stabilize the reference voltage is as a three-stage amplifier, as shown in Fig. 5, and only the inner stage constituted by QB6 and QB7 has a positive G_{m2}. Here, the points A, B, and C correspond to those in Fig. 4. In this situation, reversed nested Miller compensation (RNMC) is the most suitable approach[7]. Based on the Miller effect, the dominant pole p_1 is related to the compensation capacitor C_{C1}. Therefore, the value of C_{C1} determines the system's stability. Here, nulling resistors are introduced to cancel the RHP zero and to achieve a better high-frequency dynamic range. More-

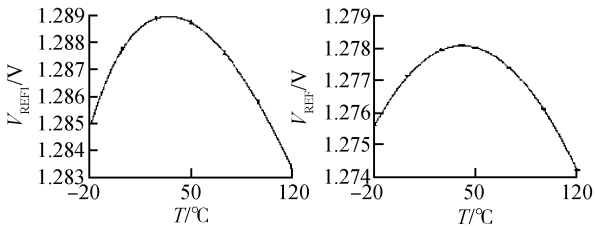

Fig. 6 Simulated temperature dependence of output reference voltage

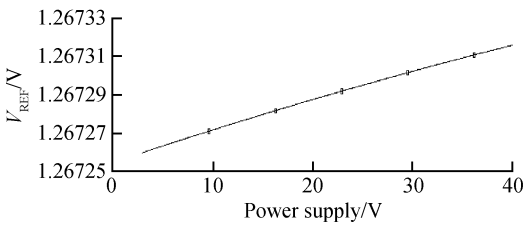

Fig. 7 Simulated output voltage of bandgap reference circuit versus power supply

over, a proper resistor load at the output node can also reduce the output impedance for better stability.

3 Simulation and experimental results

Simulations of the proposed bandgap reference were preformed in 1.5μm BCD technology. Figure 6 shows the simulated output voltages of the two references, micro-power reference, and supply-independent reference, respectively, when temperature sweeps from −20 to 120℃. Here, a supply voltage of 12V is applied. The V_{REF1} of the micro-power reference has a maximum drift of ±3mV around the mean output voltage of 1.286V. The V_{REF} of the supply-independent reference has a maximum drift of ±1.7mV around the mean output voltage of 1.276V.

Figure 7 shows the simulated output voltage of power supply-independent reference as a function of the power supply voltage at 27℃. The figure shows that the line regulation of 1.5μV/V is achieved over the supply voltage range from 3 to 40V with a maximum quiescent current of 80μA.

Powered by a 12V supply, the simulated PSRR curve of the bandgap reference is shown in Fig. 8. The curve shows that the PSRR is higher than 100dB for frequencies below 10kHz.

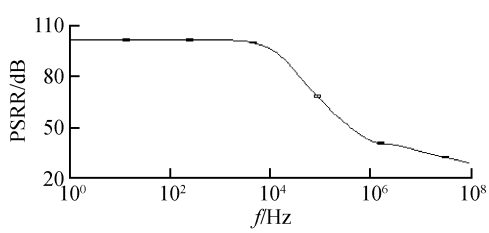

Fig. 8 Simulated PSRR of the bandgap voltage reference

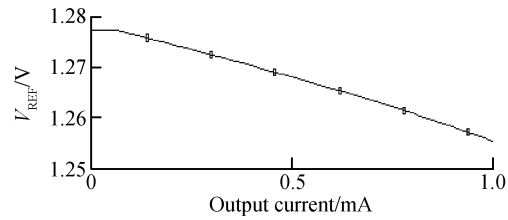

Fig. 9 Simulated output voltage of bandgap reference circuit versus output current

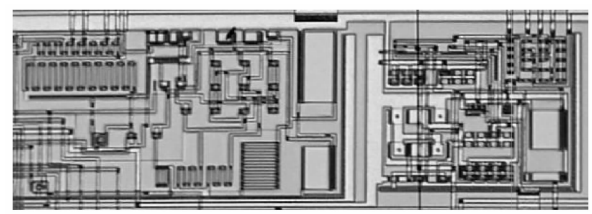

Fig. 10 Photograph of proposed bandgap reference

Figure 9 shows the simulated output voltage of the bandgap reference as a function of the operating current when powered by a 12V supply. The V_{REF} is nearly linear with the operating current and the maximum variation is about 22mV.

The bandgap circuit was fabricated in 1.5μm 2p2m BCD technology. The chip photograph is shown in Fig. 10. The circuit area is 1180μm × 434μm including two trimming resistor arrays.

The testing schemes are shown in Fig. 11.

Adjusting the supply voltage from 2.5 to 16V, the measured line regulation curve is plotted in Fig. 12. The curve is flat over a wide range of input voltages from 2.5 to 10V with a drift of about 300μV. A dramatic change happens when V_{IN} exceeds 10V. This is due to the transistor breakdown under high voltages, which is restricted by the process. The working voltage could extend to 40V if the proper high voltage process is available.

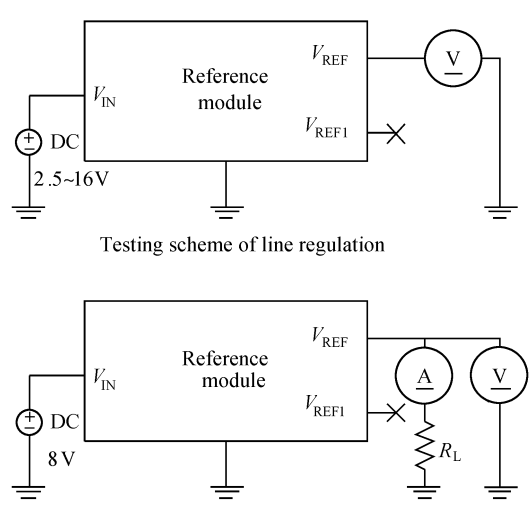

Fig. 11 Testing schemes for line and load regulation

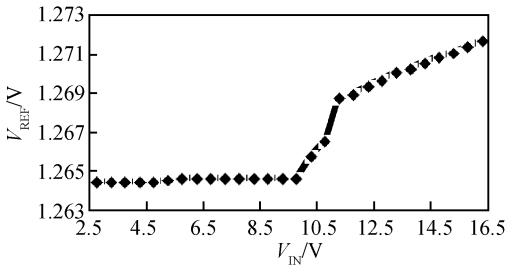

Fig. 12　Measured output voltage of bandgap reference circuit versus power supply

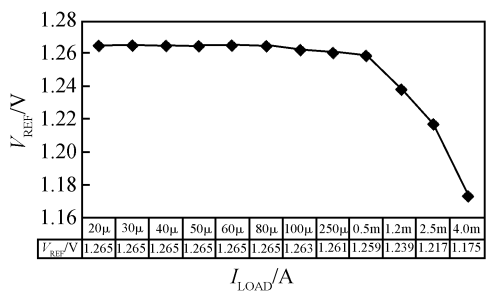

Fig. 13　Measured reference voltage versus output current curve of the bandgap reference circuit

The load regulation was tested at a supply voltage of 8V. A microampere meter in series with a load resistor R_L is used to monitor the current. By adjusting R_L, the curve of V_{REF} versus output current is obtained, as shown in Fig. 13.

For supply voltages between 2.5 and 10V, the test shows that the maximum quiescent current of this reference is 66μA in normal mode and 10.5μA in sleep mode.

Table 1 summarizes the reference specifications obtained from simulation and measurement, respectively.

Table 1　Simulated and measured results of the proposed bandgap reference

Specification		Simulated	Measured
Supply voltage range		3 ～ 40V	2.5～10V*
Supply dependency		1.5μV/V	40μV/V
Temperature coefficient		−20～120℃	–
		20ppm	
Load regulation		0 ～ 1mA	0 ～ 100μA
		22mV/mA	20mV/mA
PSRR (<10kHz)		102dB	–
Maximum quiescent power consumption	Sleep mode	90μW	105μW
	Normal mode**	556μW	660μW

* Limited by recent process

** The value at supply voltage of 10V

Table 2 presents a comparison between the reference and reported wide-range supplied bandgap references and shows that the proposed reference offers better line regulation than those previously reported.

Table 2　Comparison of wide-range supplied bandgap reference

	Rincon-Mora[8]	Paul[9]	This work
Year	1998	2005	2007
Technology	2μm CMOS with an added P-base layer	0.5μm-BCD	1.5μm-BCD
Supply voltage range	1.2 ～ 10V	4～ 8V	2.5 ～10V
Measured line regulation	408μV/V	2mV/V	40μV/V

4　Conclusion

A bandgap reference featuring supply-independent performance over a wide range of supply voltages was designed and fabricated in 1.5μm BCD technology. A novel structure was proposed to improve its performances such as PSRR and temperature stability. Moreover, an auxiliary micro-power reference was introduced to support the sleep mode and reduce its standby power consumption. Experimental results showed that besides wide supply voltage adaptability, a near zero temperature coefficient of 20ppm/℃, a line regulation of 40μV/V, a PSRR higher than 100dB, and a load regulation of 22mV/mA were also achieved.

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一种宽电源电压带隙基准源的设计*

孙越明 赵梦恋† 吴晓波

（浙江大学超大规模集成电路设计研究所，杭州 310027）

摘要：提出一种可在宽电源电压范围下工作的带隙基准源设计.由于采用了一些新的结构，使得其电源抑制比和温度稳定性有明显提高.为支持电源管理芯片的休眠工作模式以降低待机功耗，电路中专门设置了一个辅助的微功耗基准，在正常模式下为电路提供偏置，在休眠模式中替代主基准以节省功耗.仿真结果表明，该基准源提供的 1.27V 基准电压在 －20 至 120℃范围内的最大温漂为 3.5mV.当供电电压由 3V 变化至 40V 时，基准电压的变化为 56μV.在低于 10kHz 的频率范围内基准源具有大于 100dB 的电源抑制比.芯片采用 1.5μm BCD(Bipolar-CMOS-DMOS)工艺设计与实现.实验结果证实上述设计目标已基本实现.

关键词：宽电源电压；带隙基准；线性调整率；休眠模式；微功耗

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† 通信作者.Email：zhaoml@zju.edu.cn

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