A Low Power Dissipation Wide-Band CMOS Frequency Synthesizer for a Dual-Band GPS Receiver

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Abstract: This paper presents a wide tuning range CMOS frequency synthesizer for a dual-band GPS receiver, which has been fabricated in a standard 0.18μm RF CMOS process. With a high Q on-chip inductor, the wide-band VCO shows a tuning range from 2 to 3.6GHz to cover 2.45 and 3.14GHz in case of process corner or temperature variation, with a current consumption varying accordingly from 0.8 to 0.4mA, from a 1.8V supply voltage. Measurement results show that the whole frequency synthesizer consumes very low power of 5.6mW working at L1 band with in-band phase noise less than -82dBc/Hz and out-of-band phase noise about -112dBc/Hz at 1MHz offset from a 3.142GHz carrier. The performance of the frequency synthesizer meets the requirements of GPS applications very well.

Key words: PLL; GPS; frequency synthesizer; VCO; low power; CMOS RF
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1 Introduction

Recently, wireless communications are becoming more common in everyday life. Most people have a cellular phones, PDAs, or notebooks that use wireless communications. The wireless communication system consists of many components, such as low-noise amplifiers (LNA), mixers, filters, power amplifiers, frequency synthesizers, and base-band modems. Among them, the frequency synthesizer is one of the key components for high quality communications.

The global positioning system (GPS) is a satellite broadcast system providing the fundamental physical quantities of absolute position, velocity, and time information to users. The GPS signal from the satellite uses two RF bands: a primary signal at 1575.42MHz (L1 band) and a secondary signal at 1227.6MHz (L2 band). The ultimate goal of a GPS receiver is to extract the accurate position and time information from the weak satellite signals. Although the position error can be considered as a figure of merit, there exist various sources of position error. One is from the satellite itself, another is due to a propagation delay variation, and the other is from receiver impairments such as noise and jitter.

The main drawback of the current GPS system is its poor sensitivity performance in a multipath environment. To overcome this limit, the GPS modernization plan, adding a new modernized civil code called L2 C/S on L2 band, was announced. The L2 C/S code achieves better tracking performance in a multipath environment. So embedded GPS in wireless phones will make the L1/L2 dual-band receiver the most widely used of all GPS applications until nearly every satellite has the L2 civil signal, requiring a low-cost, highly integrated chip solution.

Traditionally, GPS radios were implemented in bipolar processes. However, in order to satisfy the increasing demand for lower cost and higher levels of integration, CMOS implementation is becoming more and more popular and important. Several successful implementations of integrated GPS receivers in CMOS processes were reported in Refs. [1]~[4].

This paper describes the design and implementation of a low power and wide-band CMOS frequency synthesizer for a single chip L1/L2 dual-band GPS receiver in a 180nm CMOS process that can receive both L1 and L2 band signals.

2 Circuit implementation of the frequency synthesizer

In many applications, phase-locked loops (PLL) are implemented with wide tuning ranges in order to cover the desired operating frequency bands and to accommodate process, voltage, and temperature (PVT) variations.

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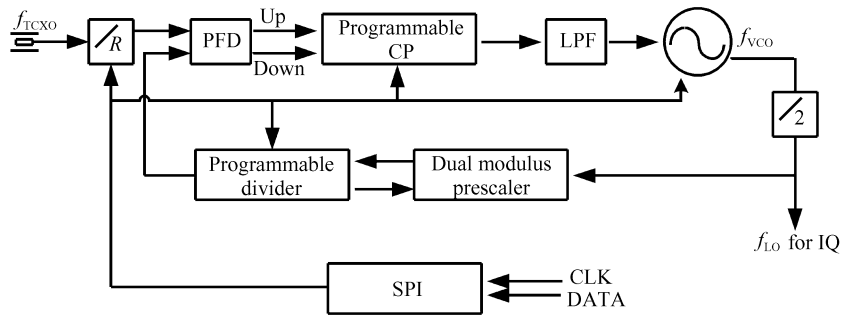

Fig. 1 Block diagram of the implemented frequency synthesizer

The block diagram of the implemented frequency synthesizer is illustrated in Fig. 1. The phase-locked loop frequency synthesizer consists of a voltage controlled oscillator (VCO), prescaler, dividers, phase frequency detector (PFD), charge pump, and loop filter. The key parameters in the PLL frequency synthesizer are the phase noise, power consumption, and lock-in time.

For better phase noise, the phase noise of the VCO should be reduced, possibly by reducing the loop bandwidth. But this will increase the lock-in time. Therefore, the reference frequency and loop bandwidth also should be carefully designed[5]. Circuit implementation details are as follows.

2.1 Voltage controlled oscillator

Figure 2 shows a simplified view of the implemented VCO architecture. To cover a wide frequency range and reduce the lock-in time, the switched-capacitor bank LC-VCO has been used. The LC tank is composed of the MIM capacitor array with 6bit switches for coarse tuning, nMOS differential varactors for fine tuning, and one symmetrical differential on-chip inductor with relatively high Q. To secure a wide frequency range, the parasitic capacitances from the active devices and metal connections have to be suppressed. Much effort is devoted to the tradeoff between phase noise and tuning range by adjusting the size of the active devices such as negative g_m-cell and MIM capacitors' switching transistors, as well as layout. The resonant tank impedance is linearly dependant on the oscillator frequency, so the tank voltage is lower at the L2 band. To maintain the tank voltage swing even at low band, the tail current is designed to be controllable depending on the frequency by 5bit switches. The total current of the active core can vary between 0.4 and 0.8mA. Base bias resistors R_b are high enough not to degrade phase noise performance. The quality factors of the inductor and varactor are about 24 and above 50, respectively.

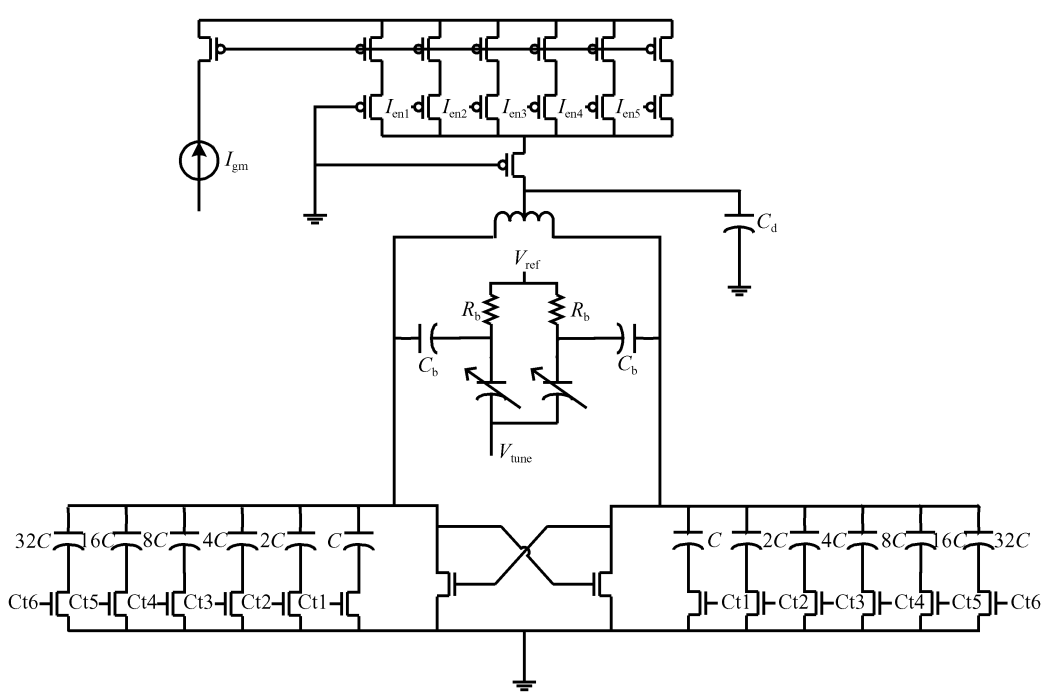

Fig. 2 Diagram of the proposed wide-band VCO

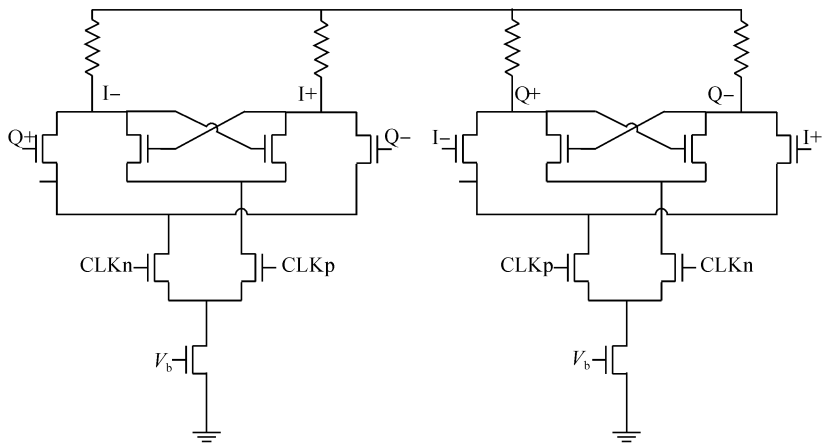

Fig. 3 High frequency divide-by-two circuit

For the sake of low power consumption and symmetrical VCO output, an nMOS cross-coupled negative g_m-cell topology is chosen.

The phase noise of a local oscillator also corrupts the spectrum and degrades the C/N_o (carrier-to-noise power density). The phase noise requirement originates from the reciprocal mixing of the phase noise spectrum by the in-band thermal noise itself. The effective C/N_o at the mixer output can be written as

$$\left(\frac{C}{N_o}\right)_{OUT} = \frac{C}{N_o + N_{PN}} = \left(\frac{C}{N_o}\right)_{IN} \times \left(\frac{1}{1+\sigma_{rms}^2}\right) \quad (1)$$

where σ_{rms}^2 is the absolute rms jitter of the local oscillator.

To obtain less than 0.1dB loss, the average phase noise should be lower than -80dBc/Hz[2]. This number is quite loose. From this fact, it can be inferred that a small-sized ring VCO is promising for low cost. However, from the viewpoint of low power consumption, an LC resonator-based VCO is still advantageous.`

According to Leeson's VCO phase noise model, as the VCO gain (K_{vco}) increases, the phase noise degrades. In this design, the K_{vco} is reduced to 100 and 35MHz/V at the L1 and L2 bands, respectively. The VCO gain is kept proportional to the frequency over the whole frequency range (2～3.6GHz). It is indeed not necessary to keep K_{vco} fixed. A linear variation with frequency holds the PLL gain, bandwidth, and phase margin constant. In this PLL, the VCO is only used in the most linear range of the tuning voltages, between 0.7 and 1.5V.

2.2 High frequency divide-by-two circuit

The circuit of the high-speed divide-by-two flip-flop is given in Fig. 3. The master and slave latches are clocked by differential clock signals. Both latches are composed of a clocked differential sensing amplifier pair and an inversely clocked latch pair.

The key to the high-speed operation of the flip-flop is the limitation of the internal swing. The smaller the transitions to be made, the faster the latches can change state. Another tradeoff is present in the transistors of the latch pair. When their transconductance is large, fast latching is possible, but changing state will be more difficult. Only nMOS transistors are implemented to limit the parasitic drain capacitance and to minimize the power consumption. The VCO frequencies are divided by two, then are provided as the LO signal of the down-conversion mixer.

2.3 Phase-frequency detector

The phase-frequency detector schematic is shown in Fig. 4. It is a commonly employed circuit that inserts pulses on up and down outputs of a certain minimum width, even when the phase difference is zero. This eliminates the dead zone problem of the PLL.

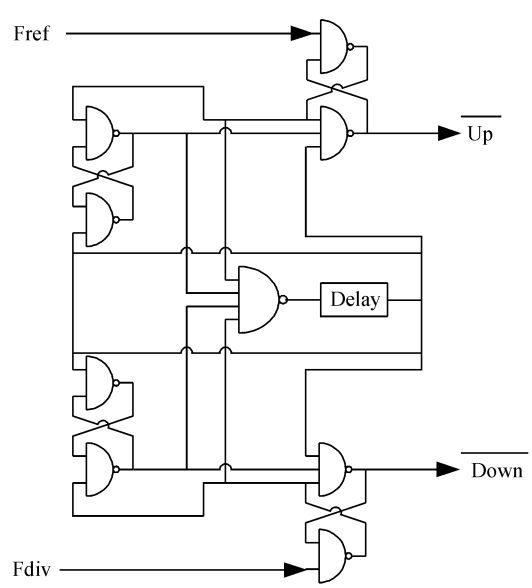

Fig. 4 PFD circuit

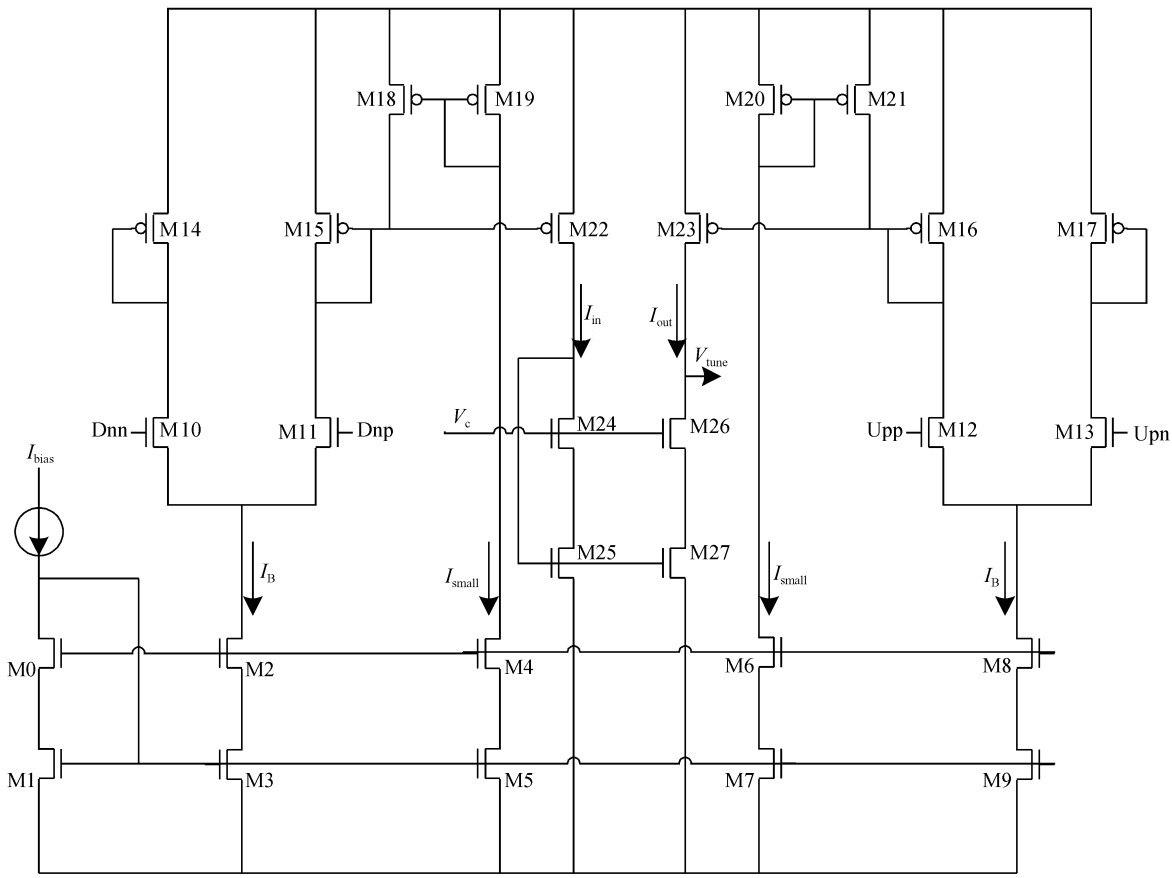

Fig. 5 Charge pump circuit

2.4 Programmable charge pump

The proposed charge pump circuit is shown in Fig. 5. It consists of a wide-swing current mirror and a symmetric charge pump pair that is composed of pump-up and pump-down circuits. The pump-up and pump-down circuits consist of a differential input pair M12-M13, current mirror load M16, bias current sources I_B and I_{small}, and weak pull-up current mirror M20-M21. The symmetric charge pump inputs are driven by PFD. The pump-up circuit receives the differential input signals from PFD to control the production of the charge current. On the other hand, the pump-down circuit controls the production of the discharge current. When Upp is high, the bias current I_B is steered through M12. The difference between I_B and I_{small} flows through M16 and is mirrored to M23. When Upp is low, the current in M16 begins to go to zero. If the charge pump circuit has no weak pull-up circuit M20-M21, there will be a long time-constant conducted current in M16 that we have not well-controlled. To overcome this problem, the weak pull-up circuit M20-M21 and I_{small} are inserted. Thus, when Upp is low, M20 mirrors I_{small} to M21 and M21 pulls up the gate of M16 to V_{DD} so that M16 could be turned off within a short period of time. The wide-swing current mirror mirrors the pump-down current to discharge node V_{tune}. Using this structure, we can accurately mirror the pump-down current. During the design of the current mirror, it is important to make sure M25～M27 is in the saturation region. The reason for including M24 is to decrease the drain-source voltage of M27. Therefore, the output current I_{out} more accurately matches the input current I_{in}.

2.5 Loop filter and prescaler

The loop filter design is a big challenge, as it determines the PLL settling time and the output phase noise characteristic. The simplest configuration is a passive filter that uses two capacitors and a resistor. The resulting PLL is then type-Ⅱ, third order. We need a tradeoff between settling time and output phase noise to determine the bandwidth of the PLL.

For the sake of reducing power consumption, TSPC logic DFF (as shown in Fig. 6.) is chosen to form the dual modulus prescaler. The total dynamic current consumption of the prescaler and the programmable divider is less than 0.1mA.

3 Experimental results

This GPS receiver chip has been fabricated in a

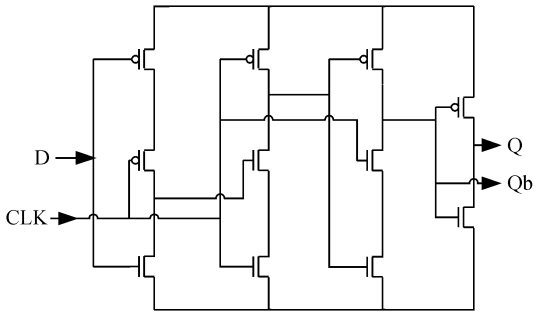

Fig. 6 TSPC DFF circuit

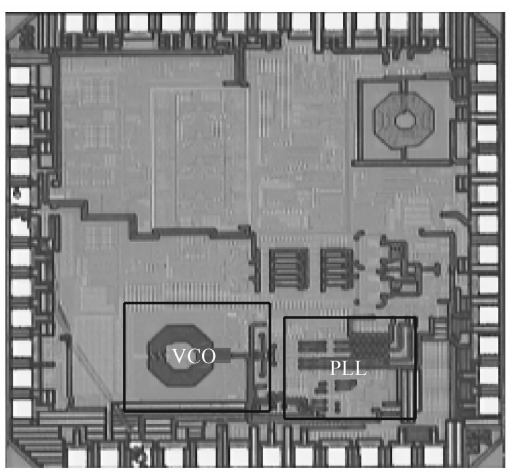

Fig. 7 Die microphotograph of the complete CMOS receiver front end

0.18μm RF CMOS process with five metal levels, as shown in Fig. 7. The availability of the triple well allows isolation of the nMOS transistor from the substrate. High quality factor MOS varactors are available; meanwhile Q for the inductor is about 24 at 3.2GHz.

The measurement results are summarized in Table 1 and meet the requirements of GPS applications very well. The whole frequency synthesizer consumes a very low power of only 5.6mW working at the L1 band, or only 6.1mW working at the L2 band; and the lock-in time is about 15μs.

Table 1 Summary of measurement results

Some key performance requirements	Experimental results
Supply voltage	1.6～2V (Typical = 1.8V)
Current consumption	3.1mA(L1 band) 3.4mA(L2 band)
VCO frequency range	2～3.6GHz
VCO gain	100MHz/V (L1 band) 35MHz/V (L2 band)
In-band phase noise	< −82dBc/Hz
Out-of-band phase noise	−112dBc/Hz@1MHz (L1 band) −115dBc/Hz@1MHz (L2 band)
Reference spurious	−65dBc @13MHz
Lock-in time	About 15μs

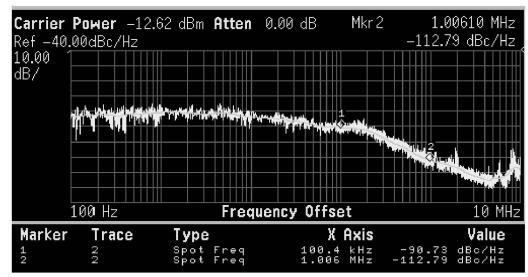

Fig. 8 Measured PLL phase noise

Table 2 Comparison of phase noise with other GPS receivers

Reference	In-band /(dBc/Hz)	100k offset /(dBc/Hz)	1M offset /(dBc/Hz)
[1]	−80	−92	−112
[2]	−80	−80	−109
[3]	—	−88	—
[4]	−80	−90	−113
This work	−82	−90	−112

Figure 8 and Table 2 show the experimental results of the phase-noise spectrum and the comparison of the phase noise with other GPS receivers, respectively.

4 Conclusion

A wide-band CMOS frequency synthesizer for a dual-band GPS receiver, which has been fabricated in a standard 0.18μm CMOS process, is proposed. The frequency synthesizer has the advantages of extremely low power consumption, better phase noise performance, wide tuning range, and fast lock-in, which is suitably integrated into a high performance dual-band GPS receiver.

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一种用于双波段 GPS 接收机的低功耗宽带 CMOS 频率合成器

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摘要：提出了一种用于双波段 GPS 接收机的宽带 CMOS 频率合成器.该 GPS 接收机芯片已经在标准 0.18μm 射频 CMOS 工艺线上流片成功，并通过整体功能测试.其中压控振荡器可调振荡频率的覆盖范围设计为 2～3.6GHz，覆盖了 L1，L2 波段的两倍频的频率点，并留有足够的裕量以确保在工艺角和温度变化较大时能覆盖所需频率.芯片测试结果显示，该频率综合器在 L1 波段正常工作时的功耗仅为 5.6mW，此时的带内相位噪声小于－82dBc/Hz，带外相位噪声在距离 3.142G 载波 1M 频偏处约为－112dBc/Hz，这些指标很好地满足了 GPS 接收芯片的性能要求.

关键词：锁相环；全球定位系统；频率合成器；压控振荡器；低功耗；CMOS 射频
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