A Piecewise Curvature-Corrected CMOS Bandgap Reference with Negative Feedback

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Abstract: A piecewise curvature-corrected bandgap reference (BGR) with negative feedback is proposed. It features employing a temperature-dependent resistor ratio technique to get a piecewise corrected current, which corrects the nonlinear temperature dependence of the first-order BGR. The piecewise corrected current generator also forms negative feedback to improve the line regulation and power supply rejection (PSR). Measurement results show the proposed BGR achieves a maximum temperature coefficient (TC) of 21.2ppm/℃ without trimming in the temperature range of −50～125℃ and a PSR of −60dB at 2.6V supply voltage. The line regulation is 0.8mV/V in the supply range of 2.6～5.6V. It is successfully implemented in an SMIC 0.35μm 5V n-well digital CMOS process with the effective chip area of 0.04mm^2 and power consumption of 0.18mW. The reference is applied in a 3,5V optical receiver trans-impedance amplifier.

Key words: piecewise curvature-corrected; bandgap reference; line regulation; PSR; temperature coefficient
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1 Introduction

Bandgap references (BGRs) are essential components in most purely analog, mixed-signal, and digital processing systems, and generate voltage reference with low temperature coefficient (TC) in a large temperature range (TR). To achieve this goal, many curvature-corrected BGR architectures have been proposed. Most of these architectures are designed in bipolar or BiCMOS processes[1～3]. BGR with low temperature drift in a CMOS process is needed to achieve low cost and to be integrated into a digital processing system. In 1983, Song and Gray proposed a curvature-compensation BGR in a 6μm standard digital CMOS process, which achieves TC of 25.6ppm/℃ after trimming over the TR of −55～125℃[4]. The BGR covered 3.5mm^2 chip area and dissipated 12mW power consumption with a ±5V supply voltage, which limites its application in integrated digital processing systems. A matched nonlinear correction (MNC) CMOS BGR was introduced in Ref. [5]. A TC of 16.7ppm/℃ was achieved without trimming. However the TR was only 85℃, which is not suitable for most industrial applications. Another CMOS curvature-compensated BGR employing temperature-dependent resistor ratio technique was presented in Ref. [6], but little attention was paid to improving its line regulation and PSR. A pre-regulated curvature-corrected BGR with high line regulation and a TC of less than 20ppm℃ after trimming was proposed, which generates a piecewise-linear corrected current to improve its TC in a 2μm MOSIS process[7]. The piecewise-linear corrected current is zero in the lower TR and is linearly dependent on temperature in the higher TR, which is not effective for the correction of the nonlinear temperature dependence of first-order BGR.

2 First-order BGR

Figure 1 shows the schematic of the first-order BGR. The output voltage of the BGR consists of the

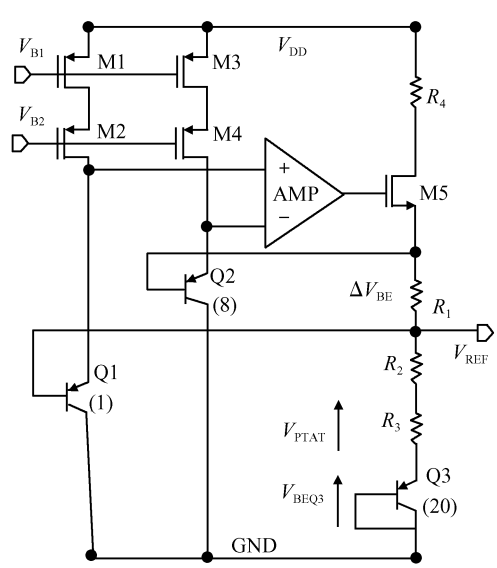

Fig. 1 Implementation of the first-order BGR

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base-emitter voltage of a bipolar transistor with a TC of approximately -2.2mV/℃ and a voltage proportional to the absolute temperature (PTAT). Typically, the base-emitter voltage is expressed as

$$V_{BE}(T) = V_{G0} - [V_{G0} - V_{BE}(T_R)] \times \frac{T}{T_R} - V_T(\eta - \alpha)\ln\frac{T}{T_R} \quad (1)$$

where V_{G0} is the diode voltage at 0K, V_T is the thermal voltage, T_R is the reference temperature, and η and α are the temperature dependent parameters of silicon mobility and of the collector current, respectively. As shown in Eq. (1), the first term of V_{BE} is independent of temperature, while the second term and the third term are linearly and nonlinearly dependent on temperature, respectively. A first-order BGR is achieved by compensating the linear temperature dependence in Eq. (1) with a PTAT voltage. The bias voltage V_{B1} and V_{B2} in Fig. 1 come from a high-swing self-biasing circuit. The AMP ensures the emitter voltage of Q1 and Q2 is equal, the voltage difference of base-emitter (ΔV_{BE}) for Q1 and Q2 is added across resistor R_1, which is a PTAT voltage. Then a PTAT current through resistor R_1 is achieved, which is

$$I_{PTAT} = \frac{V_T \ln n}{R_1} \quad (2)$$

where $n = 8$ is the emitter area ratio between Q2 and Q1. The PTAT current flows through $R_2 + R_3$, and the output voltage (V_{REF}) is expressed as

$$V_{REF} = V_{BEQ3} + V_T \ln(n)(R_2 + R_3)/R_1 \quad (3)$$

Adjusting the resistor ratio of $(R_2 + R_3)/R_1$, the linear temperature dependence of V_{BE} is compensated to get a first-order BGR, which leaves the nonlinear temperature dependence uncompensated. The output voltage of the first-order BGR can be expressed as

$$V_{REF} = V_{G0} - V_T(\eta - \alpha)\ln\frac{T}{T_R} \quad (4)$$

The simulated variation of V_{REF} with temperature is 5.5mV in the TR of $-50 \sim 125$℃. The TC is 22.5ppm/℃, which is typical for a first-order BGR. In order to reduce the TC further, a curvature-corrected BGR is necessary.

3 Proposed curvature-corrected method

3.1 Operation

The proposed curvature-corrected BGR is based on the addition of a piecewise corrected current to the first-order BGR, which corrects the second term in Eq. (4).

Figure 2 illustrates the schematic of the piecewise corrected current generator. It consists of a PTAT current given in Eq. (2), a resistor R_4, and a transistor M6. The temperature-dependent resistor ratio technique in Ref. [6] is used to achieve a PTAT^2 voltage. As a result, the TC of R_4 must be higher than that of R_1. The output voltage at node 'A' is given as

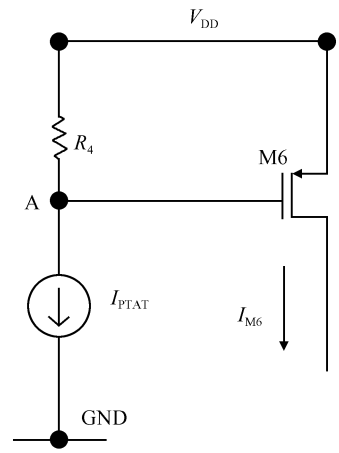

Fig. 2　Piecewise corrected current generator

$$V_A = V_{DD} - \frac{R_4 V_T \ln n}{R_1} \quad (5)$$

Due to the positive TC of R_4/R_1, a PTAT^2 voltage is achieved at the gate-source voltage of transistor M6, which is

$$V_{SG\_M6} = \frac{R_4 V_T \ln n}{R_1} \propto T^2 \quad (6)$$

When V_{SG_M6} is much lower than its threshold V_{th}, there will be no current through M6. When V_{SG_M6} is closing and still lower than its threshold, M6 operates in weak inversion. But due to the strong temperature dependence of V_{SG_M6} and nearly -2mV/℃ TC of V_{th}, the TR for M6 working in weak inversion is narrow. So the state where M6 works in weak inversion is neglected here. When V_{SG_M6} is higher than its threshold, the current through M6 is given as

$$I_{M6} = \frac{1}{2}\mu_p C_{OX}\frac{W}{L}\left(\frac{R_4 V_T \ln n}{R_1} - |V_{thp}|\right)^2 \quad (7)$$

where C_{OX}, W, and L are independent of temperature. The temperature dependence of electron mobility is approximately expressed as $\mu_p \propto T^{-2}$[8]. Extending Eq. (7) with respect to temperature, we get

$$I_{M6} = AT^{-2}(BT^2 + CT)^2 = AB^2T^2 + 2ABCT + AC^2 \quad (8)$$

where A, B, and C are constants independent of temperature. Considering the higher-order temperature dependence and neglecting the lower one in Eq. (8), the approximate TC of $I_{M6} \propto T^2$ is achieved. Figure 3 shows the simulated temperature dependence of I_{M6} in the TR of $-50 \sim 125$℃, which is outlined as

$$I_{M6} = \begin{cases} 0, & V_{SG\_M6} \leqslant |V_{thp}| \\ \propto T^2, & V_{SG\_M6} > |V_{thp}| \end{cases} \quad (9)$$

Here, the value of R_4 is set low so that M6 will conduct nearly zero current in the TR of $-50 \sim 10$℃. When the temperature is higher than 10℃, I_{M6} shows

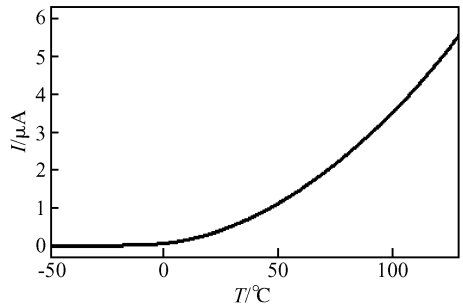

Fig. 3 Piecewise corrected current versus Kelvin degree

its high temperature dependence. To achieve a proper current for the correction of the nonlinear temperature dependence in Eq. (4), the W/L of M6 is set as 1.5μm/5μm. The temperature dependence of I_{M6} is like the corrected current in the piecewise-linear current-mode technique[7], but more effective at correcting the nonlinear term of the first-order BGR in the higher TR.

3.2 Circuit implementation

The circuit implementation of the proposed BGR is shown in Fig. 4. It consists of the proposed piecewise curvature-corrected BGR, the high-swing self-biasing circuit, and the startup circuit. The high-swing self-biasing circuit is formed by transistors M7～M20 and resistor R_5, which provides a supply-insensitive bias voltage for the proposed BGR. The startup circuit helps to avoid the zero-current state of the self-biasing circuit when supply is provided. When the self-biasing circuit reaches the desired operating point, the startup circuit turns off, which will not interfere with the normal operation of the self-biasing circuit. The proposed piecewise curvature-corrected BGR is achieved by adding a transistor M6 to the first-order BGR. Its output voltage is the sum of the base-emitter voltage of Q3, the PTAT voltage, and the corrected voltage, which is

$$V_{REF} = V_{BEQ3} + \frac{V_T \ln(n)(R_2 + R_3)}{R_1} + I_{M6} R_3 \tag{10}$$

Another advantage of the proposed BGR is its improvement in line regulation and PSR, which is achieved by a negative feedback loop formed by the piecewise current generator. Suppose a ΔV is generated at the output node V_{REF}, then the variation of node 'A' is given as

$$\Delta V_A = \Delta V \frac{R_4}{R_4 + R_1 + r_{ds5}} \tag{11}$$

where r_{ds5} is the output resistance of M5. The current variation of transistor M6 is expressed as

$$\Delta I_{M6} = - g_{m6} \Delta V \frac{R_4}{R_4 + R_1 + r_{ds5}} \tag{12}$$

where g_{m6} is the transconductance of M6, then the variation of BGR's output voltage is approximately

$$\Delta V_{REF} = \left(1 - g_{m6} \frac{R_4}{R_4 + R_1 + r_{ds5}} R_3\right) \Delta V \tag{13}$$

As shown in Eq. (13), the variation of reference is reduced by the negative feedback loop.

3.3 Operational amplifier

The schematic of the AMP is illustrated in Fig. 5. The V_{REF} voltage at room temperature is nearly 1.2V. The voltage of the emitter for Q1 and Q2 is

$$V_{inn} \approx V_{inp} = V_{REF} + V_{BE}(T_R) \tag{14}$$

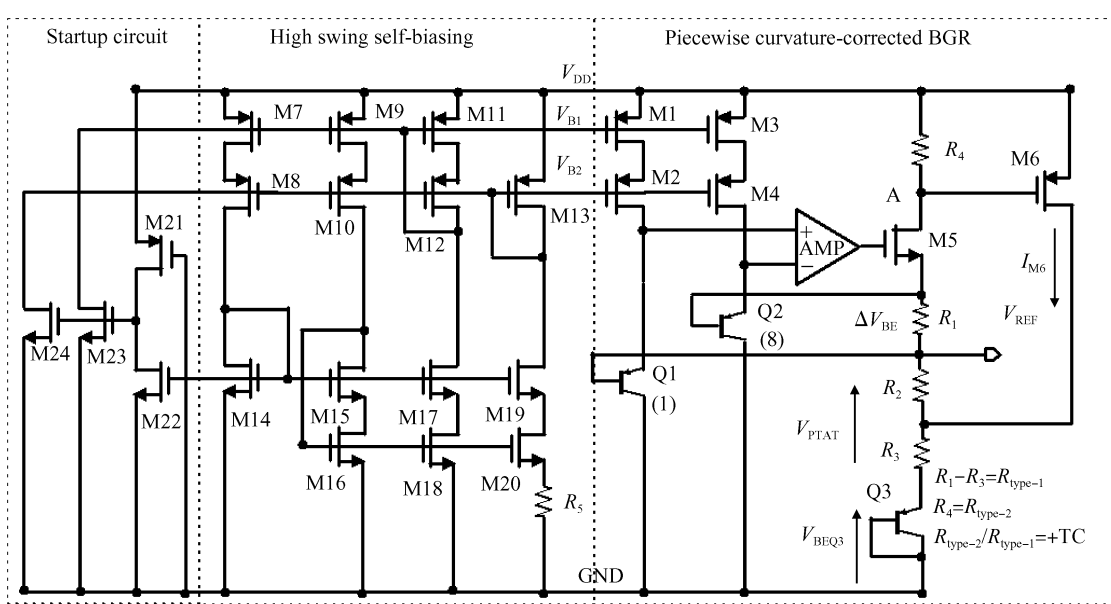

Fig. 4 Circuit implementation of the proposed BGR

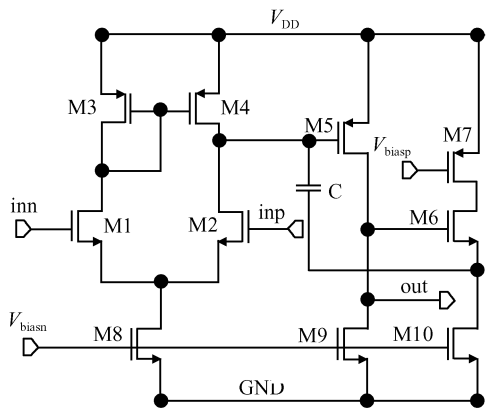

Fig. 5　Circuit of the AMP

Table 1　Simulated performance of the AMP

Parameter	Value
Supply	2.6V
DC gain	71dB
Unity bandwidth	8.4MHz
Phase margin	80°

So the AMP uses a two stage operational amplifier with nMOS transistors M1 and M2 as input transistors. M5 and M9 form the second gain stage. To achieve a proper phase margin for the AMP, a source follower M6 and capacitor C are designed to cancel the zero in the right half plane. This AMP includes a zero in the left half plane, which is used to cancel the output pole. The bias voltage for the nMOS and pMOS transistor comes from the high swing self-biasing circuit. The simulated performances of the AMP are listed in Table 1.

4　Verification

To evaluate the feasibility of the proposed BGR, the schematic is fabricated in an SMIC 0.35μm 5V n-well digital CMOS process. The threshold of this technology is $V_{thn} \approx 0.8$V and $V_{thp} \approx -1.0$V at 0℃. In this design, $R_1 \sim R_3$ are made of n-diffusion with the TC of 1.6×10^{-3} and sheet resistance of 81Ω/□. R_4 is made of n-well with the TC of 4.6×10^{-3} and the sheet resistance of 1160Ω/□. Figure 6 shows the die microphotograph, including the proposed BGR. The effective chip area of the BGR including the self-biasing and startup circuit is 0.04mm^2.

Table 2　Simulated performance list of resistor variation

	TR/℃	TC/(ppm/℃)	PSR/dB
Res_tt	−50～125	3.9	−76.5
Res_ff	−55～105	5	−61
Res_ss	−30～130	5	−64.8

In order to ensure the stability of the proposed BGR's performance with variation of sheet resistance, the worst cases for the resistors are simulated. The maximum variation of sheet resistance for n-diffusion and n-well in this technology are ±15 and ±290 Ω/□, respectively. The simulated results are listed in Table 2. As is given in Eqs. (5)～(7), the improvement in TC is mainly dependent on the ratio of TC of different resistors in the effective TR. So the simulated TC in different cases is nearly stable, as given in Table 2. The variation of the resistor ratio will affect the feedback factor given in Eq. (11) and the PSR of the proposed BGR. In all, a TC of less than 5ppm/℃ in the TR of 160℃ and a PSR of −61dB are achieved in the worst cases.

The temperature dependencies of the first-order and proposed BGR are measured with the operating temperature varying from −50 to 125℃. The measured temperature dependence at 2.6V supply voltage is shown in Fig. 7. The TC of the first-order BGR is 51.4ppm/℃. The output voltage variation of the proposed BGR is 4.5mV, which amounts to a TC of 21.2ppm/℃. The TC of the proposed BGR improves when the supply voltage increases. The TC at 3 and 5.6V supply are 18.8 and 15ppm/℃, respectively. Figure 8 shows the reference voltage versus supply voltage at room temperature. The variation of the first-order BGR is 21mV in the supply range of 2.6～5.6V, which amounts to line regulation of 7mV/V. The variation of the proposed BGR increases linearly from 1.2147 to 1.2171V in the same supply range. So the line regulation is 0.8mV/V. The PSR is measured by incorporating a sinusoidal ripple on a

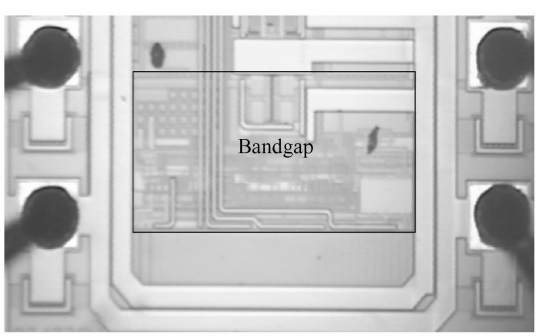

Fig. 6　Chip photograph including the propose BGR

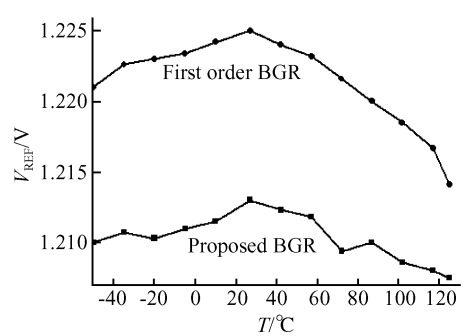

Fig. 7　Measured temperature dependence of the BGR

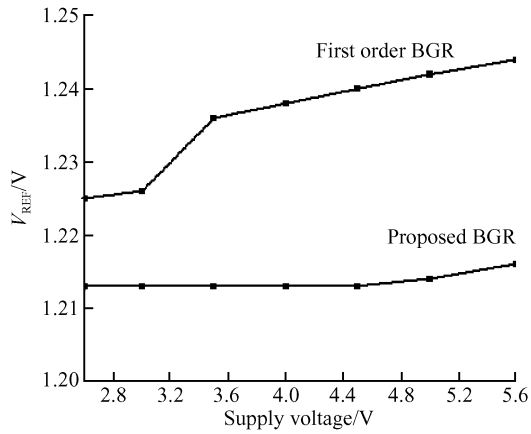

Fig. 8 Measured BGR voltage versus supply voltage

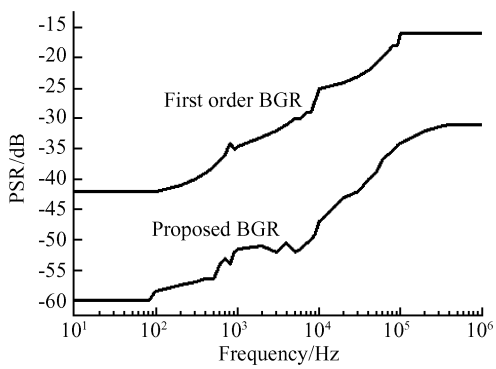

Fig. 9 Measured PSR of the proposed BGR

2.6V DC offset at room temperature without a filter capacitor. The frequency of the ripple is swept from 10Hz to 1MHz. The measured PSR is shown in Fig. 9. The PSR of the proposed BGR and the first-order BGR are −60 and −42dB under low frequency and −30 and −15dB when the frequency is higher than 1MHz. Table 3 lists the measured performance improvement of the proposed BGR over the first-order BGR. The performance improvement for the proposed BGR is obvious. It is achieved by adding only a transistor with the size of 1.5μm/5μm, which requires little extra power consumption and chip area. The total power consumption including the startup circuit and self-biasing circuit is 0.18mW.

Table 3 Performance list of the propiosed and the first-order BGR

	TC /(ppm/℃)	Line regulation /(mV/V)	PSR /dB
First-order BGR	51.4	7	−42
Proposed BGR	21.2	0.8	−60

5 Conclusion

A novel piecewise curvature-corrected BGR with improved performance in line regulation and PSR is proposed. Compared with the temperature-dependent resistor ratio technique in Ref. [6], the resistor with higher TC does not affect the temperature dependence of the proposed BGR in the lower TR (−50～10℃), which helps to extend the TR to −50℃ in the proposed BGR. In the upper TR (10～125℃), the temperature dependence of the piecewise corrected current is higher than that of the piecewise-linear current technique in Ref. [7], which helps to achieve a lower TC in the higher TR. The negative feedback formed by the piecewise current generator improves the line regulation and PSR of the proposed BGR.

Table 4 lists the performance comparison of this work and that of some state-of-art CMOS curvature-corrected BGRs. The TC without trimming, TR, and PSR of the proposed BGR are similar to those in Ref. [4]. But the proposed BGR can operate down to 2.6V supply voltage and occupies less chip area. Compared with Refs. [5～7], the proposed BGR achieves a TC of 21.2ppm/℃ in a larger TR without trimming. The TR for the proposed BGR is 175℃, while the maximum TR for Refs. [5～7] is only 105℃. The TC of 5.3ppm/℃ in Ref. [6] is very competitive, but it is achieved after trimming. In addition, the chip area of this work is much smaller than that in Ref. [5], and

Table 4 Comparison among the curvature-corrected BGRs

	This work	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]
TC /(ppm/℃)	Without trimming, 21.2	After trimming, 25.6	Without trimming, 16.7	After trimming, 5.3	After trimming, <20
TR/℃	−50～125	−55～125	15～100	0～100	−15～90
Technology	0.35μm 5V digital CMOS	6μm digital CMOS	0.35μm CMOS	0.6μm 5V CMOS	2μm MOSIS
Chip area/mm^2	0.04	3.5	0.18	0.057	0.223
Supply voltage /V	2.6	±5	1	2	1.1
PSR/dB	−60	−60	−40	−47	—
Line regulation /(mV/V)	0.8	—	3.5	1.43	0.4

the line regulation and PSR is better than Refs.[5,6] due to the negative feedback loop. The proposed piecewise curvature-correction BGR is implemented in a standard n-well digital CMOS process. It is applied in a 3,5V optical receiver trans-impedance amplifier.

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具有负反馈的分段曲率校正 CMOS 带隙基准源

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摘要：提出了一种新型带有负反馈的分段曲率校正带隙电压基准源，该基准源的主要特色是利用温度相关的电阻比技术获得一个分段曲率校正电流，校正了一阶带隙基准源的非线性温度特性.该分段线性电流产生电路还形成了一个负反馈，以改善带隙基准源的电源抑制和线性调整率.测试结果表明：在 2.6V 电源电压下，该基准源在没有采用校正的条件下，在 -50～125℃ 温度范围内实现了最大 21.2ppm/℃ 温度系数，电源抑制比为 -60dB.在 2.6～5.6V 电源电压下的线性调整率为 0.8mV/V.采用中芯国际(SMIC)0.35μm 5V n 阱数字 CMOS 工艺成功实现，有效芯片面积 0.04mm^2，其总功耗为 0.18mW.该基准源应用于 3,5V 兼容的光纤接收跨阻放大器.

关键词：分段曲率校正；带隙基准源；线性调整率；电源抑制；温度系数

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