

An Enhancement-Mode AlGa_N/Ga_N HEMT with Recessed-Gate*

Wang Chong[†], Zhang Jinfeng, Quan Si, Hao Yue, Zhang Jincheng, and Ma Xiaohua

(Key Laboratory of Wide Band Gap Semiconductor Materials and Devices, Institute of Microelectronics, Xidian University, Xi'an 710071, China)

Abstract: Fabrication of enhancement-mode high electron mobility transistors on AlGa_N/Ga_N heterostructures grown on sapphire substrates is reported. These devices with 1.2 μm gate-length, 4 μm space between source and drain, and 15 nm recessed-gate depth exhibit a maximum drain current of 332 mA/mm at 3 V, a maximum transconductance of 221 mS/mm, a threshold voltage of 0.57 V, f_t of 5.2 GHz, and f_{max} of 9.3 GHz. A dielectric layer formed unintentionally during recessed-gate etching is confirmed by contrasting the Schottky I - V characteristics of pre-etching and post-etching. The frequency characteristics and subthreshold characteristics of the devices are studied in detail.

Key words: high electron mobility transistors; AlGa_N/Ga_N; recessed-gate; threshold voltage

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1 Introduction

AlGa_N/Ga_N heterostructure high electron mobility transistors (HEMTs) have shown advantages in high temperature and high power microwave applications^[1,2]. To date, Ga_N enhancement-mode (E-mode) devices have attracted a great deal of research interest for their use in high-voltage switching and driving of high speed circuits. AlGa_N/Ga_N HEMT is generally depletion-mode (D-mode) because there is two-dimensional electron gas (2DEG) in the heterostructure interface when it is grown. But an E-mode HEMT is required in the domain of digital circuits, and a high-voltage switching for current is only needed when the gate is positively biased. Lanford *et al.* developed an E-mode HEMT with a recessed-gate structure by etching a part of AlGa_N layer of the AlGa_N/Ga_N heterostructure, which realized E-mode HEMT using the depletion effect of a Schottky junction on 2DEG^[3]. Wang *et al.* reported an E-mode HEMT realized by F ion implant doping^[4]. Liu *et al.* demonstrated a non-recessed E-mode device on AlInGa_N/Ga_N^[5]. In this paper, we report a high threshold voltage E-mode AlGa_N/Ga_N HEMT and analyze the correlative factors of current subthreshold characteristics and frequency characteristics of the devices.

2 Device structure and fabrication

The AlGa_N/Ga_N HEMT structure was grown by metal organic chemical vapor deposition (MOCVD)

on (0001) sapphire substrate that was 330 μm thick. The heterostructure consisted of a 3 μm-thick Ga_N channel layer, a 5 nm-thick AlGa_N spacer layer, an n-doped ($2 \times 10^{18} \text{ cm}^{-3}$) 12 nm-thick AlGa_N layer, and a 5 nm-thick AlGa_N cap layer from bottom to top. The AlN mole fraction of the AlGa_N was 27% measured by photoluminescence (PL). Hall measurement results show that the 2DEG electron mobility and concentration are $1267 \text{ cm}^2 / (\text{V} \cdot \text{s})$ and $1.12 \times 10^{13} \text{ cm}^{-2}$ at room temperature, respectively. Figure 1 shows the structure of our E-mode HEMT, which is compatible with D-mode HEMT processing.

The device fabrication started with mesa isolation, which was formed by ICP with the etch-depth of 150 nm and etch-speed of 100 nm/min. Ohmic contacts consisting of Ti/Al/Ni/Au (30 nm/180 nm/40 nm/60 nm) were annealed in nitrogen ambient at 850 °C. The recess area was etched using the ICP process at 0.1 nm/s with depth of 15 nm and etch-bias of

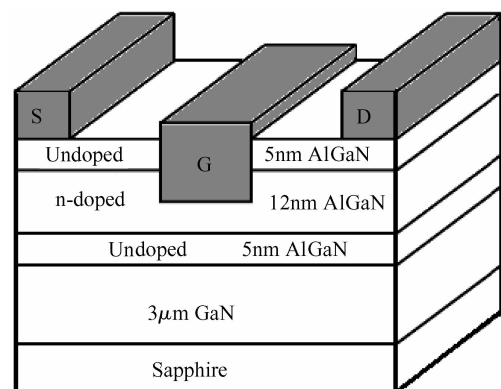


Fig. 1 Cross section of the E-mode AlGa_N/Ga_N HEMT

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[†] Corresponding author. Email: wangchong197810@hotmail.com

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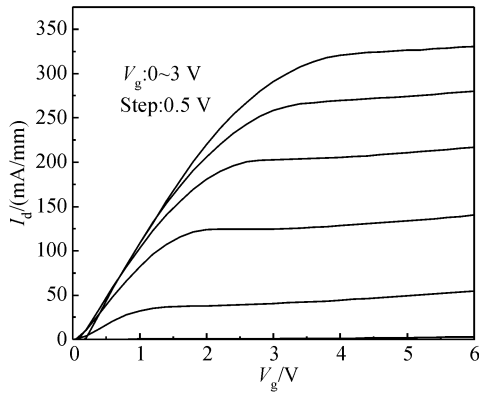


Fig. 2 Output characteristics of the E-mode HEMT

50V, followed by the deposition of Ni/Au (30nm/200nm) in the gate-recess area by electron-beam evaporation. The gate length, gate width, and distance between source and drain are 1.2, 100, and 4 μ m, respectively. Using on-wafer TLM patterns, the contact resistance and specific contact resistance were measured to be 0.63 $\Omega \cdot \text{mm}$ and 1.2 $\times 10^{-5} \Omega \cdot \text{cm}^2$. Direct current characteristics and high frequency characteristics were measured by an HP4156B semiconductor parameter analyzer and an HP8720D network analyzer.

3 Results and discussion

To achieve an E-mode HEMT, the resistance from gate to source and the resistance from gate to drain should be low and the channel resistance under the gate electrode should be high at zero bias, thus different processes should be used for different areas of the channel. By thinning the AlGaIn layer underneath the gate electrode using etching, the 2DEG underneath gate electrode decreases and the 2DEG in the other part of channel remains constant. Further reduction of the 2DEG underneath gate electrode can be implemented by forming a Schottky contact with large barrier height. Then, an E-mode HEMT with on-state only at positive operation voltage can be realized.

The output characteristics of the E-mode HEMT are shown in Fig. 2. The maximum drain current density of approximately 332mA/mm is reached at V_g of 3V. Because the 2DEG is depleted by the Schottky gate at zero bias after recessed-gate etching, the maximum current of the E-mode HEMT decreases compared with the general D-mode HEMT at the same V_g . The DC transfer characteristics measured at V_{ds} of 6V are shown in Fig. 3, and the device exhibits $g_{m\text{-max}}$ of 221mS/mm at V_g of 1.8V and a threshold voltage of 0.57V.

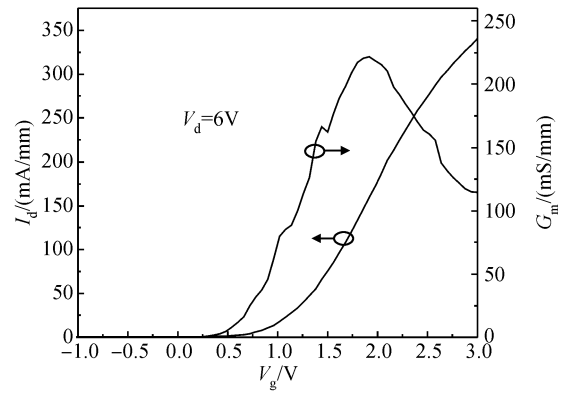


Fig. 3 Transfer characteristics of the E-mode HEMT

$$V_T = \Phi_B - \frac{\Delta E_C}{q} - \frac{qN_D(d - d_i)^2}{2\epsilon_0\epsilon_1} - \frac{\sigma_{\text{pol}}}{\epsilon_0\epsilon_1}d \quad (1)$$

Equation (1) shows the factors that influence the threshold voltage, where σ_{pol} is the polarization charge, q is the electron charge, ϵ_0 is the vacuum permittivity, ϵ_1 is the relative dielectric constant, $q\Phi_B$ is the Schottky barrier height, ΔE_C is the conduction band offset, N_D is the donor density of AlGaIn, d is the total thickness of AlGaIn, and d_i is the thickness of the space layer. Deeper recessed-gate depth and larger Schottky barrier height lead to a more positive threshold voltage.

Conventional D-mode AlGaIn/GaN HEMTs exhibit high gate leakage current when V_g is larger than 2V. Furthermore, the maximum drain current enhances very weakly when V_g is larger than 2V. However, our E-mode HEMT presents MOS gate characteristics with a low gate leakage current at V_g of 3V. Moreover, the drain current of the E-mode HEMT increases by 126mA/mm when the gate voltage increases from 2 to 3V, indicating a high potential to improve the current further.

After the gate etching, the AlGaIn layer was bombarded by ions from the ICP etching and some etching damage such as N vacancies and dislocations generated on the surface of AlGaIn, so the Schottky leakage current of the devices increased^[6]. After analyzing the Schottky I - V characteristics of the E-mode HEMT, as shown in Figs. 4 and 5, we find that the reverse-bias current decreases while the forward turn-on voltage of the Schottky I - V characteristics increases after gate etching. Experimental results show that a dielectric layer is formed unintentionally during gate etching so that the devices exhibit MOS gate characteristics. But the quality of the dielectric layer was not good enough that the decrease of reverse-bias leakage current was less than that of the MOS HEMT. Palacios *et al.* developed an E-mode HEMT that can work at a V_g of 4V^[7]. They thought the device could work at high gate bias because the energy band was affect-

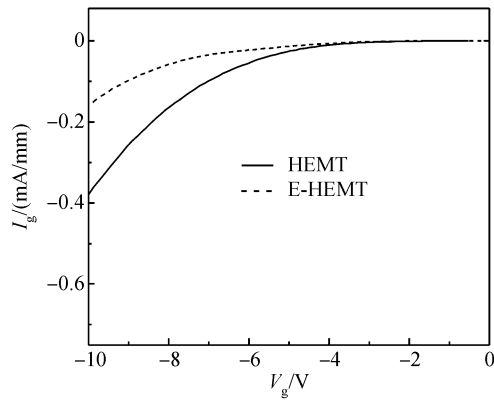


Fig.4 Schottky leakage current of the HEMT and the E-mode HEMT

ed by the fixed charge introduced during gate etching. From our experiment, we find that the MOS gate characteristic of the E-mode HEMT is determined by the unintentionally formed dielectric layer, and the layer's existence depends mainly on the pressure of the ICP chamber. The layer might be formed by a second deposition in the ICP etching when the pressure of the ICP chamber is high. The Si element was found in the dielectric layer by analyzing SEM scatter electrons. The sample is placed on a Si wafer when it is etched, and there is N_2 in the etching gas, so the Si_3N_4 dielectric is unintentionally formed in recessed-gate etching when the pressure of the ICP chamber is high.

The RF characteristics of the E-mode HEMT were measured at V_g of 1.8V and V_{ds} of 6V, and f_t of 5.2GHz and f_{max} of 9.3GHz have been achieved, as shown in Fig.6. During the gate etching, interface states may emerge between the unintentionally formed dielectric layer and the surface of the semiconductor, which will restrain the improvement of the RF characteristics.

Figure 7 shows the transfer characteristics of both the E-HEMT and the D-HEMT in the semilog

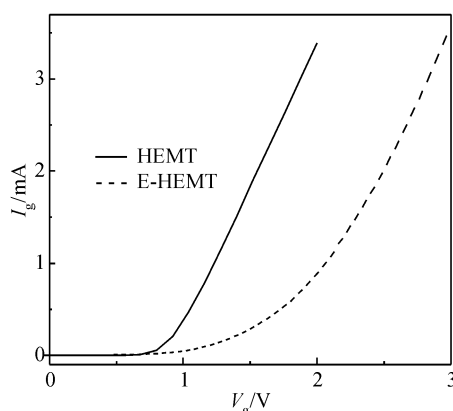


Fig.5 Schottky forward characteristic of the HEMT and the E-mode HEMT

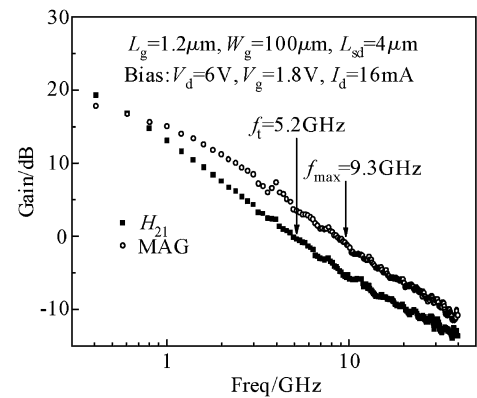


Fig.6 Gain versus frequency of the E-mode HEMT

coordinate. The sub-threshold characteristics of the devices are reflected by the slope of curve of I_d versus V_g near the threshold voltage. The rising of I_d of the E-mode HEMT above the threshold voltage is slower than that of the D-mode HEMT, and the slopes of the sub-threshold characteristics decrease. Experimental results indicate that surface states are produced in the AlGaIn when the area of the recessed-gate is bombed in the ICP etching^[8], then the surface states trap free electrons and affect control ability of the gate on the channel near the threshold voltage. Therefore, the sub-threshold characteristics of the E-mode HEMTs degenerate.

4 Conclusion

We have fabricated recessed-gate AlGaIn/GaN E-mode HEMTs, which exhibit a maximum drain current of 332mA/mm, a maximum transconductance of 221mS/mm, and a threshold voltage of 0.57V. When the gate length is 1.2 μ m, the f_t and f_{max} are 5.2 and 9.3GHz, respectively. The experimental results suggest that a Si_3N_4 dielectric layer unintentionally deposited during recessed-gate etching reduces the gate leakage current and helps the E-mode HEMT to work at higher forward bias. Thus, the device demonstrates

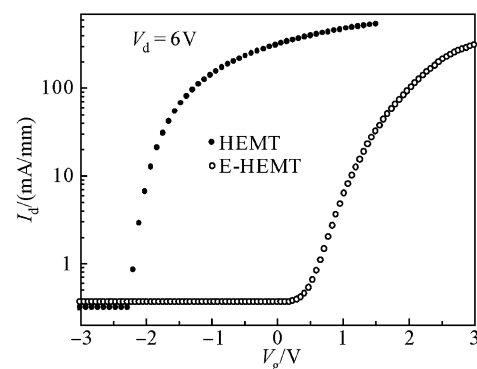


Fig.7 Transfer characteristics of the E-mode and D-mode HEMTs

MOS gate characteristics and the experimental results suggest that we can fabricate an E-mode HEMT with MOS structure. The current sub-threshold characteristics and frequency characteristics are influenced mainly by the surface states introduced in recessed-gate etching.

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增强型 AlGaIn/GaN 槽栅 HEMT*

王 冲[†] 张金凤 全 思 郝 跃 张进城 马晓华

(西安电子科技大学微电子研究所 宽禁带半导体材料与器件重点实验室, 西安 710071)

摘要: 成功研制出蓝宝石衬底的槽栅增强型 AlGaIn/GaN HEMT. 栅长 $1.2\mu\text{m}$, 源漏间距 $4\mu\text{m}$, 槽深 15nm 的器件在 3V 栅压下饱和电流达到 332mA/mm , 最大跨导为 221mS/mm , 阈值电压为 0.57V , f_t 和 f_{max} 分别为 5.2 和 9.3GHz . 比较刻蚀前后的肖特基 $I-V$ 特性, 证实了槽栅刻蚀过程中非有意淀积介质层的存在. 深入研究了增强型器件亚阈特性和频率特性.

关键词: 高电子迁移率晶体管; AlGaIn/GaN; 槽栅; 阈值电压

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[†] 通信作者. Email: wangchong197810@hotmail.com

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