A 5.4mW Low-Noise High-Gain CMOS RF Front-End Circuit for Portable GPS Receivers*

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Abstract: This paper describes a CMOS low noise amplifier (LNA) plus the quadrature mixers intended for use in the front-end of portable global positioning system (GPS) receivers. The LNA makes use of an inductively degenerated input stage and power-constrained simultaneous noise and input matching techniques. The quadrature mixers are based on a Gilbert cell type. The circuits are implemented in a TSMC 0.18μm RF CMOS process. Measurement results show that a voltage conversion gain of 35dB is achieved with a cascade noise figure of 2.4dB, an input 1dB compression point of -22dBm, and an input return loss of -22.3dB. The fully differential circuits only draw 5.4mW from a 1.8V supply.

Key words: CMOS RF IC; GPS; low-noise amplifiers; mixers; receivers; noise figure
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1 Introduction

Radio frequency designs are increasingly taking advantage of technology advances in CMOS. RF building blocks and complete receivers realized in CMOS and showing performance compatible with the most stringent standards have been proven. The use of CMOS technologies for implementation of front end electronics in a GPS system is therefore attractive because of the promise of integrating the whole system on a single chip[1~3].

Global positioning system (GPS) is a satellite broadcast system providing the fundamental physical quantities of the absolute position, velocity, and time information to users. Although GPS was originally developed for military purposes, its civil use has greatly been increased in recent years. There is great enthusiasm in the consumer market for the capabilities of GPS. Manufacturers of cellular telephones, portable computers, and other mobile devices are looking for ways to incorporate GPS into their products. Thus, there is a strong motivation to provide highly integrated solutions at the lowest possible power consumption[4]. So far, there have been no reports on fully CMOS integrated GPS receivers at home. This is the first case in which a radio has been successfully fully integrated in CMOS technology for a portable application.

This paper describes the design and measurement of a fully differential LNA plus quadrature mixers for portable GPS receivers. This solution is intended for a low-IF architecture with an IF of about 4MHz. The LNA is used to amplify the RF signal to reduce the noise contribution from the mixer. The mixer performs frequency conversion using nonlinear elements in time-varying circuits. The two building blocks are very important in the GPS receiver because their performances affect the system performance and the performance requirements of the adjacent building blocks, which include the LO, image-rejection filter, and IF stages. Thus, in the design of circuits, there are several common goals. These include minimizing the noise figure, providing enough gain with sufficient linearity, and providing a stable 50Ω input impedance to achieve good input matching. The additional constraint of low power consumption is even more critical in portable applications[1].

With these goals in mind, an inductively degenerated input stage and a power-constrained simultaneous noise and input matching technique are used in the LNA design. To enhance the gain of the LNA, the output of the first stage is AC-coupled through the capacitance to the second stage. To save power, the current through the second gain stage is reused to supply the core transistors in the first stage. The quadrature mixers follow the LNA directly on-chip and are based on a Gilbert cell type. Figure 1 shows the complete circuit of the differential LNA plus quadrature mixers. Measurement results show that a voltage conver-

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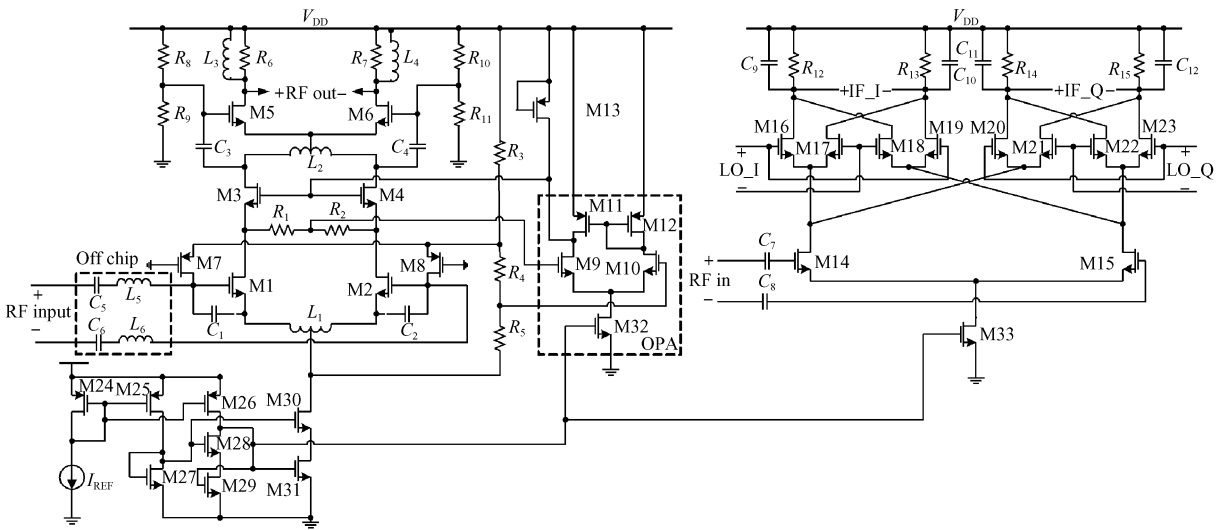

Fig. 1 Complete circuit of the differential LNA plus quadrature mixers

sion gain of 35dB has been achieved with a cascade noise figure of 2.4dB, an input 1dB compression point of −22dBm, and an input return loss of −22.3dB. The fully differential circuits only draw 5.4mW from a 1.8V supply.

2 Circuit design

2.1 LNA design

As shown in Fig. 1, a differential architecture is selected for better rejection of on-chip interference and common-mode disturbances. This consideration is particularly important in GPS applications, where both the supply and substrate voltages may be noisy. To maximize common-mode rejection at high frequencies, it is critically important for the layout to be as symmetrical as possible[5].

The differential pairs can be matched well through careful layout design, but the on-chip spiral inductors are difficult to keep symmetric. Thus, two symmetric inductors with center-tap (See Fig. 2) are chosen to be the source and load inductors, respectively. Under differential mode operation, a DC bias can be applied at the tap of the inductors L_1 and L_2. The

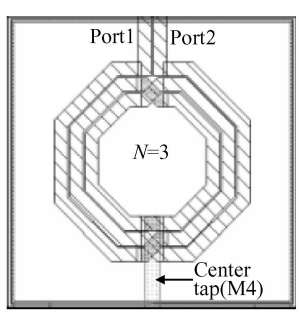

Fig. 2 Symmetric inductor with center-tap

number of the inductors can be reduced from four to two, and the area of the die will be smaller. L_3 through L_6 are off-chip inductors.

The LNA consists of two main parts: the input stage, formed by four core transistors, M1 through M4, and the output stage, formed by transistors M5 and M6. The input stage is cascoded to reduce the influence of the gate-to-drain overlap capacitance G_{gd} on the LNA's input impedance and to mitigate the Miller effect. In addition, the use of cascode improves the LNA's reverse isolation, which is important for suppressing LO feedthrough from the mixers back to the input of LNA and the stability of the LNA by minimizing interactions between the interstage tank and the input matching network. The input matching is performed off-chip.

The output of the first stage is AC-coupled through C_3 and C_4 to M5 and M6 for additional gain. To save power, the current through the output stage is reused to supply the four core transistors M1 through M4, decreasing the power by a factor of two[4]. Hence, the center tap of the output tuning inductor L_2 returns to the common source connection of M5 and M6. The output of LNA is tuned by L_3, L_4 and R_6, R_7 for improved gain and impedance matching with the quadrature mixers. The output network can also reject any low frequency noise.

The LNA biasing current can be chosen to optimize the noise and current consumption performances. In the presented circuits, a high-swing, low-voltage current mirror is used and the low threshold voltage of the process permits four devices to be stacked. To keep the devices M1 and M2 saturated while leaving some room for signal swing, a common mode feedback loop is used to allow the amplifier to operate reliably at low supply voltage (1.8V), despite

Table 1　LNA simulated performances

I/mA	Gain/dB	NF/dB	IIP3/dBm	S_{11}/dB
2	27	0.9	−8	−25

Table 2　Mixers simulated performances

I/mA	Gain/dB	NF/dB	IIP3/dBm
1	15	6.6	−2

supply, temperature, and process variations. Choosing the appropriate $V_{gs} - V_t$ at bias for the desired IIP3[6] leads to a bias current of 1mA per side.

The LNA uses an inductively degenerated input stage and an LC load. This topology achieves minimum noise figure, matched input impedance, and maximum transconductance gain for given current consumption. A problem of this topology is the sensitivity to gate induced current noise, since such noise is enhanced by the Q-factor of the input circuit[7]. To optimize the noise figure of the LNA, it is important to model the induced gate noise of the input devices. The noise source plays an important role as a noise totally dominated by the gate induced current noise. In this topology, at a given frequency, the sum of gate induced and thermal noise will be the minimum for an optimum device size. Because of the strong sensitivity of the gate-induced current noise to the intrinsic gate capacitance (it follows a square law), an improvement can be obtained with additional capacitances C_1 and C_2 in parallel to the intrinsic gate capacitance of transistor M1 and M2. The insertion of the capacitors to decouple Q from C_{gs} adds a degree of freedom when adjusting the reduction of Q for any given value of C_{gs}. Therefore, a new optimum condition, with a lower noise figure near the minimum, can be achieved. This is called the power-constrained simultaneous noise and input matching (PCSNIM) technique[8].

A device modeled in 0.18μm RFCMOS technology is used for simulation. The optimum gate width of the input stage is 100μm, the source inductor L_1 is 1.7nH, and the load inductor L_2 is 10.5nH for high gain. Table 1 reports a summary of the LNA simulated performances.

2.2　Mixer design

The LNA is followed by the I-Q quadrature mixers that are AC-coupled to the LNA and based on the Gilbert cell (Fig. 1). The mixers translate the input signal from RF to an intermediate frequency of 4.092MHz.

Among many proposed active mixers, the widely used double-balanced Gilbert-cell mixer topology is preferred since it can provide both LO and RF rejection at the IF output. Furthermore, spurious products can be suppressed effectively and high intercept points can be achieved. The mixer is required to provide a low noise figure, a high conversion gain, and high linearity. The simultaneous achievement of these requirements is a challenging task in the design.

Figure 1 shows that the quadrature mixers comprise a differential pair driver stage (M14 and M15) and two differential switching quads (M16～M19 and M20～M23). The driver stage amplifies the RF signal to compensate for the attenuation due to the switching process and to reduce the noise contribution from the switching quad[9]. The differential switching quad controlled by local oscillator signal forms a multiplication function that converts the RF signal to an IF signal. The two mixers are resistively loaded and have capacitors in parallel with them to form a low pass network for filtering the high-frequency component. Noise is present in all the transistors making up these functions.

The driver stage can be optimized as the input stage of the LNA to reduce its noise contribution. But for the low-IF GPS receiver, the mixer flicker noise is very important and the switching transistors primarily determine the flicker noise performance. The flicker noise of the switching transistors appears at the mixer output through two dominant mechanisms: the direct and indirect mechanisms[10]. A large LO amplitude lowers the direct mechanism and the indirect mechanism depends on the frequency and the capacitance at the common source node of the switching pair. Improved linearity and reduced flicker noise are achieved by subtracting DC current from the switching pair.

The optimum width of the amplifier transistor and the switching transistor is 80 and 50μm, respectively, and the load resistors are 3.2kΩ. Table 2 summarizes the quadrature mixers simulated performances.

3　Experimental results

The GPS RF front-end has been integrated in a TSMC 0.18μm RF CMOS process with six metal levels. The availability of the triple well allows isolation of the nMOS transistors from the substrate. A die photograph of the chip is shown in Fig. 3. The die area is 2.2mm×2.1mm and the area of LNA plus I-Q mixers is 0.95mm×0.55mm. The experimental setup used for characterization of LNA and quadrature mixers is shown in Fig. 4.

The RF signal is injected into the LNA input via a balun and an input matching network. The balun converts the single-ended signal provided by the RF

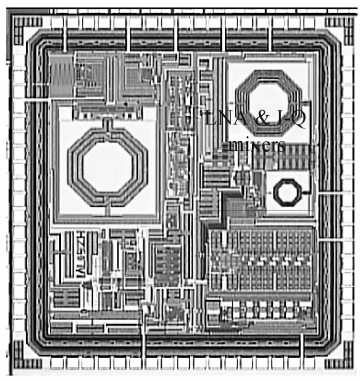

Fig. 3 Die photo

signal generator into a differential signal. Particular surface acoustic wave (SAW) filters naturally provide a differential output, so a balun is not necessary. The matching network provides a real 50Ω impedance to match with the signal source. Figure 5 shows that at 1.57542GHz, the measured S_{11} is less than −22dB. Following the mixer, an IF driver is used to measure the mixer output. The driver is designed so that its linearity does not interfere with the mixer linearity measurement, and its insertion loss will be compensated. In a real chip, an image-reject filter and an AGC amplifier would replace the IF driver. The output IF spectrum is shown in Fig. 6 and the measured 1dB compression point is shown in Fig. 7. The results of experimental measurements are summarized in Table 3 and compared to other designs.

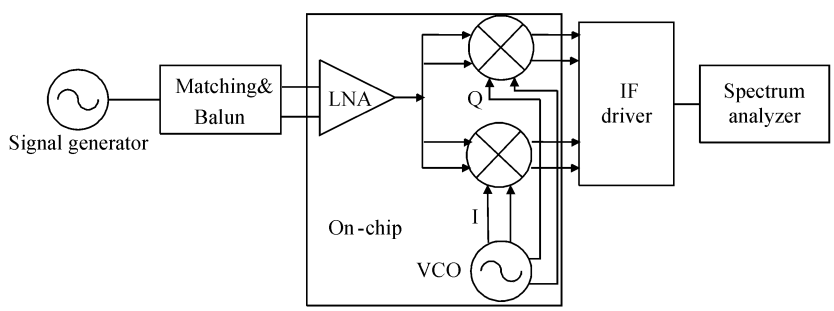

Fig. 4 Measurement setup

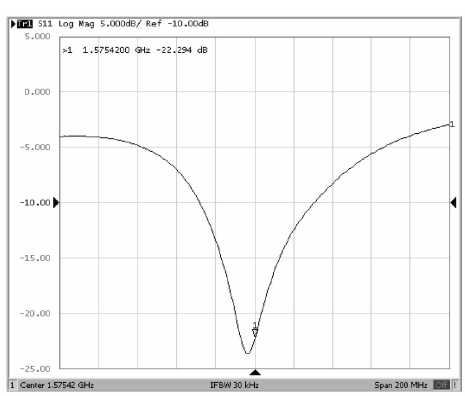

Fig. 5 Measured S_{11}

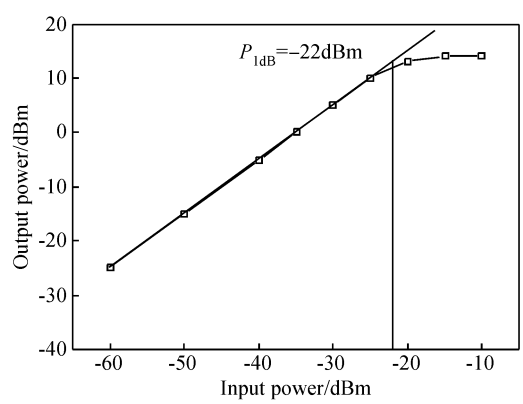

Fig. 7 Measured 1dB compression point

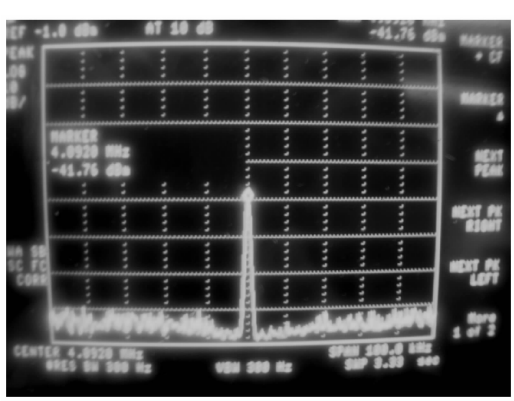

Fig. 6 Measured IF spectrum

Table 3 GPS Front-end performance summary

Parameter	This work	Ref. [4]	Ref. [11]
Technology	0.18μm CMOS	0.35μm CMOS	0.35μm CMOS
Supply voltage/V	1.8	1.5	2.8
LO frequency/MHz	1571.328	1400.42	1435.42
LO leakage to RF port /dBm	−90	——	——
IF frequency/MHz	4.092	175	140
S_{11}/dB	−22.3	−12	−12.3
Cascade noise figure/dB	2.4	4.1	3.8
Total conversion gain/dB	35	13.4	40
1dB compression (input) /dBm	−22	−20	−35.5
Power dissipation/mW	5.4	12	22.4
Die area/mm^2	0.52	0.84	4.2

4 Conclusion

A 5.4mW low-noise, high-gain RF front-end for portable GPS receivers has been presented. The functional LNA/mixer combination has a voltage gain of 35dB, a cascade NF of 2.4dB, an S_{11} of −22.3dB, and a P_{1dB} of −22dBm. This demonstration shows the potential for a fully integrated CMOS RF front-end, even when targeting stringent standards. In particular, low power consumption and a low noise figure are the main features of this realization.

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用于便携式 GPS 接收机中的 5.4mW 低噪声高增益 CMOS 射频前端电路设计*

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摘要： 设计了应用于便携式 GPS 接收机射频前端中的 CMOS 低噪声放大器和正交混频器. 该电路中的低噪声放大器采用带源端电感负反馈的输入级，并引入功耗约束下的噪声和输入同时匹配技术. 正交混频器基于吉尔伯特单元. 电路采用 TSMC 0.18μm RF CMOS 工艺实现，总的电压转换增益为 35dB，级联噪声系数为 2.4dB，输入 1dB 压缩点为 −22dBm，输入匹配良好，输入回损为 −22.3dB，在 1.8V 电压供电下，整个全差分电路功耗为 5.4mW.

关键词： CMOS 射频集成电路；全球定位系统；低噪声放大器；混频器；接收机；噪声系数
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