MOS Model 20 Based RF-SOI LDMOS Large-Signal Modeling*

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Abstract: A novel large-signal equivalent circuit model of RF-SOI LDMOS based on Philips MOS Model 20 (MM20) is presented. The weak avalanche effect and the power dissipation caused by self-heating are described. The RF parasitic elements are extracted directly from measured *S*-parameters with analytical methods. Their final values can be obtained quickly and accurately through the necessary optimization. The model is validated in DC, AC small-signal, and large-signal analyses for an RF-SOI LDMOS of 20-fingers (channel mask length, $L = 1\mu$m, finger width, $W = 50\mu$m) gate with high resistivity substrate and body-contact. Excellent agreement is achieved between simulated and measured results for DC, *S*-parameters (10MHz～20.01GHz), and power characteristics, which shows our model is accurate and reliable. MM20 is improved for RF-SOI LDMOS large-signal applications. This model has been implemented in Verilog-A using the ADS circuit simulator (hpeesofsim).

Key words: RF-SOI LDMOS; large-signal model; MOS Model 20; harmonic power; Verilog-A
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1 Introduction

Today, the rapid growth of wireless communication at radio frequencies (RF) has created a huge demand in high-performance RF components for power amplifiers in base station, consumer, and automotive applications. Due to the high gain, good linearity, and low cost, the laterally diffused MOS (LDMOS) offers a good alternative to GaAs MESFETs and silicon bipolar junction transistors (BJT) for L- and S-band power amplifiers[1]. LDMOS power amplifiers have been developed for WCDMA, GSM, WLAN, and WiMAX applications recently[2～5]. With the scaling down of smart power ICs, silicon-on-insulator (SOI) technology is becoming more attractive because it has many advantages over bulk silicon: SOI offers a better isolation scheme leading to improved circuit density, latchup-free operation, and simplifications in processing[6,7]. Moreover, the implementation of an LDMOS in SOI may allow the integration of the RF power amplifier into a wireless system-on-a-chip, in which all of the digital, analog, and RF circuits of a wireless system are integrated onto a single die. Thus, there has been increasing interest in DC and RF performance of SOI LDMOS[1,6～15].

Optimal designs for RF power amplifiers and other IC-applications require accurate models, especially physics-based models, for circuit simulation which is valid in DC, AC small-signal, and large-signal conditions over a wide range of bias and frequency. Several LDMOS models have been developed[1,6～15]. Yang *et al*. reported an empirical compact LDMOS large-signal model description with thermal node[1]. The main advantage of empirical models lies in their simplicity and numerical efficiency. Drawbacks are their use of limited physics, which reduces overall accuracy and complicates the definition of scaling rules[13]. Previous physical models, such as the BSIM3-SOI[14], have too many parameters and too complex an extraction procedure. Some physical compact models for SOI LDMOS have been reported in the literature with better accuracy[7,9,15], but they are limited to DC and AC small-signal operations. The table-based models have problems with a relatively long simulation time, no capability to include self-heating effects, and less accuracy to predict distortion behavior of power amplifiers due to the limitation of discontinuities in the model elements and nonlinearities in their interpolation for imperfect measurement data[1,16]. Wood *et al*. reported a large-signal LDMOS model for RF power amplifier applications[17]. However, the simulation accuracy still needs to be improved and the model validity is not shown for DC or AC small-signal operation under different biasing conditions. Thus, a fast, accurate, robust, and physics-based LDMOS intrinsic and RF parasitic elements model is still lacking.

Philips MOS Model 20 (MM20) is a new physics-

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based compact LDMOS model. Unlike other MOS models (EKV, BSIM3-SOI and PSP), MM20 was developed specifically for LDMOS devices. This model uses surface-potential-based formulations to calculate the currents and charges of an LDMOS device, giving an accurate physical description of the transition from weak to strong inversion in the channel region, as well as from accumulation to depletion in the drift region. MM20 includes an accurate description of all physical effects important for LDMOS devices, such as: velocity saturation, mobility reduction in the channel and the drift region, conductance effects of the channel region (channel length modulation, DIBL and static feedback), weak avalanche currents in the channel region, and the quasi-saturation effect, which is unique for LDMOS[8,18]. As a result, MM20 gives an accurate description in all regimes of operation, ranging from subthreshold to superthreshold in both the linear and saturation regimes[10]. Though, there is an iteration procedure inside the model used for the calculation of the internal-drain potential, it has been demonstrated that MM20 is robust and sufficiently fast during circuit simulations[11].

This paper reports a detailed simulation study of the DC, AC small-signal, and large-signal behavior of LDMOS devices. From the characterization and analysis, a novel MM20 based analytical RF large-signal model is derived. Excellent agreement is achieved between simulated and measured results of the DC and *S*-parameters (10MHz～20.01GHz). The power performance simulation also shows the proposed model is accurate in reproducing the large-signal characteristics of SOI LDMOS through comparison with the measured results.

2　SOI LDMOS device structure and its RF parasitic components

RF device simulation requires modeling and calibration of the intrinsic device and parasitic components[19]. Figure 1 shows the cross-section of the SOI LDMOS transistor under study with RF parasitic components. It is a body-contact n-channel device with a 20-finger (channel mask length, $L = 1\mu$m, finger width, $W = 50\mu$m, gate-oxide thickness, 30nm) gate. The p-well is diffused under the gate, where the channel is formed. The p^+ well body contact is connected to the source contact. The lightly doped drain (LDD) between the drain contact and the active channel is the drift region, which makes LDMOS devices have a high-voltage handling capacity. The resistance of the drift region is complicated with dependence on the gate and drain biases, leading to the quasi-saturation

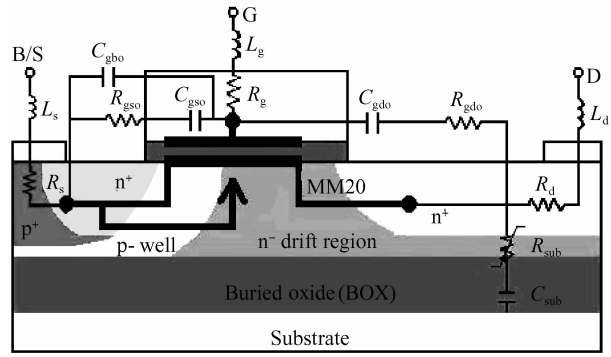

Fig. 1　Cross-section of an RF-SOI LDMOS transistor with equivalent circuit described by MM20 and RF parasitic components

phenomenon that is unique for LDMOS[8,9].

The equivalent circuit described by MM20 and RF parasitic components of this SOI LDMOS transistor is shown in Fig. 1. All the components are physically based. The pad parasitic effects can be removed by de-embedding, so the pad parasitic elements are not shown here. However, the terminal inductive effect caused by the leads cannot be removed easily in this process. So three terminal inductances (L_g, L_d and L_s respectively) still have to be considered[20]. The resistance R_g representing the effective lumped gate resistance consists of both the gate lead-poly contact resistance and the high frequency distributed gate lead resistance. The resistances R_s and R_d stand for effective source and drain resistances, consisting of the n-well, contact, and high frequency distributed lead resistances. C_{gdo} and R_{gdo} represent the gate-drain oxide parasitic capacitance and high frequency parasitic resistance, respectively. C_{gso} and R_{gso} represent the gate-source oxide parasitic capacitance and high frequency parasitic resistance, respectively. C_{gbo} represents the gate-body capacitance. The serial structures R_{sub} and C_{sub} are introduced here to represent the resistance and capacitance at the bottom of the drift region and the BOX region. The intrinsic SOI LDMOS behavior is modeled by MM20.

Figure 2 shows a new common-source RF-SOI LDMOS large-signal equivalent circuit model based on MM20. For large-signal model simulation, the resistor and the capacitor, whose instantaneous values depend on two voltages (i.e. V_{DS} and V_{GS}), should be implemented as a controlled current source and a controlled charge source, respectively[17]. Hence, the intrinsic MM20 components include Q_B, Q_G, Q_S, Q_D and I_{ds}, and all of them can be omitted at zero bias[17,20]. Due to the combination of SOI with thick buried oxide and high-power dissipation, the self-heating of the device is significant. Therefore, a model that accounts for the temperature rise due to self-heating is essential for re-

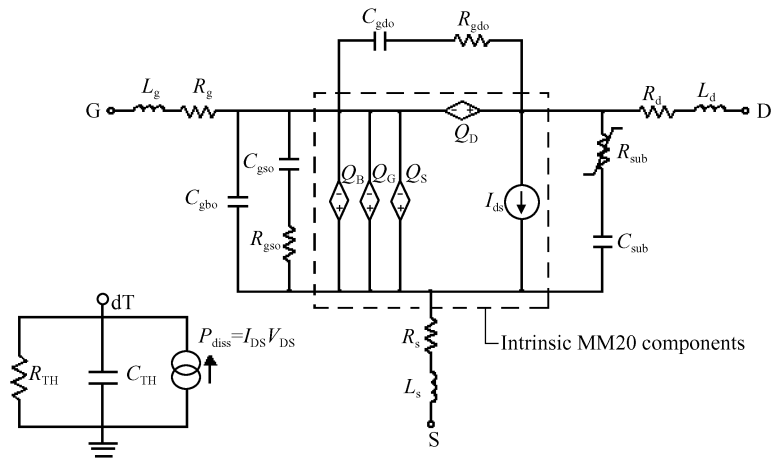

Fig. 2 MM20 based RF-SOI LDMOS large-signal equivalent circuit model with a self-heating network

liable results[6]. So the self-heating network is added to take this into account.

3 Extraction of RF parasitic components

All the measured *S*-parameters are de-embedded, so the pad parasitic effects are not considered in this work. The linear elements L_g, L_d, L_s, R_g, R_d, and R_s can be extracted from the *S*-parameter measurements at zero-bias, i. e. $V_{DS} = 0$V, $V_{GS} = 0$V. At this biasing condition, the intrinsic DC model components shown in Fig. 2 can be canceled according to MM20, and the equivalent circuit can be simplified to that shown in Fig. 3. The method can be found in Ref. [20].

After the extraction of these parasitic elements, the *Y*-parameters of the Π structure network in the dashed line box can be obtained by applying the following mathematical operation:

$$Y = \text{ztoy}\begin{pmatrix} Z_{11} - Z_g - Z_s & Z_{12} - Z_s \\ Z_{21} - Z_s & Z_{22} - Z_d - Z_s \end{pmatrix} \quad (1)$$

where $Z_g = R_g + j\omega L_g$, $Z_d = R_d + j\omega L_d$, $Z_s = R_s + j\omega L_s$. The Π structure network can be divided into three parts: the left part (C_{gbo}, C_{gso} and R_{gso}), the middle part (C_{gdo} and R_{gdo}), and the right part (R_{sub} and C_{sub}). Their *Y*-parameters are respectively given by

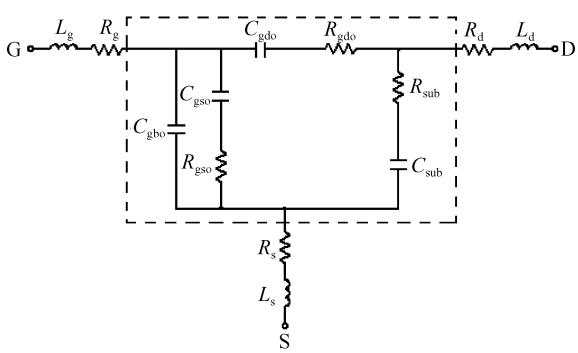

Fig. 3 Simplified small-signal equivalent circuit at $V_{GS} = 0$V, $V_{DS} = 0$V

$$Y_L = Y_{11} + Y_{12} \quad (2)$$

$$Y_M = -Y_{12} = -Y_{21} \quad (3)$$

$$Y_R = Y_{22} + Y_{21} \quad (4)$$

Thus, all the elements in the dashed line box can be extracted analytically following the method mentioned in Ref. [20]. Subsequently, the measured *S*-parameters are set as the numerical optimization targets, and the optimization range of each parameter can be largely narrowed down due to the analytical extraction. Accurate results can be quickly achieved.

The resistance of R_{sub} is strongly influenced by input voltage, from the measured *S*-parameters with certain gate and drain bias, which is significant for simulated S_{22}. Thus R_{sub} is extracted from the measured *S*-parameters with $V_{DS} = 1 \sim 9$V, step size: 2V, $V_{GS} = 0 \sim 7$V, step size: 0.2V, as can be seen in Fig. 4. Thus, R_{sub} is modeled by

if (V_{DS}<vthd)

$$R_{sub} = \text{ud} \cdot \tanh(\text{slope} \cdot V_{GS} - \text{r1}) + V_{DS}^k / s + \text{yo} \quad (5)$$

else begin

if (V_{GS}<vthg)

$$R_{sub} = \text{ud} \cdot \tanh(\text{slope} \cdot V_{GS} - \text{r1}) + V_{DS}^k / s + \text{yo} \quad (6)$$

else

$$R_{sub} = \text{ud} \cdot \tanh(\text{slope} \cdot V_{GS} - \text{r1}) - a \cdot \ln V_{GS} + V_{DS}^k / s + \text{yo} \quad (7)$$

end

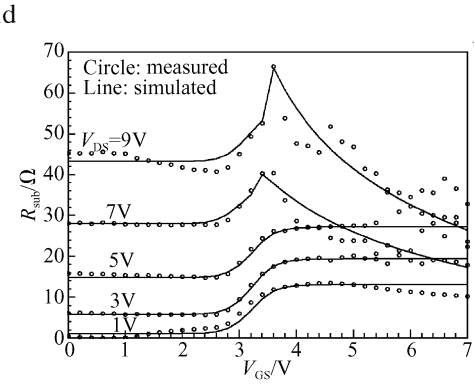

Fig. 4 Extracted and modeled nonlinear resistance results

where vthd, vthg, ud, slope, r1, k, s, a and yo are the fitting parameters.

4 Experimental verification of the model

The proposed direct extraction method was applied to determine the parameters of the test SOI LDMOS, which has 20 fingers with a 1μm gate length and a total gate width of 1mm. The on-wafer LDMOS transistor is tested in a Cascade Microtech summit 1101B RF probe station. The DC characteristics are measured by an Agilent 4156C. The S-parameters are measured in the common source-substrate configuration using an Agilent E8363B vector network analyzer. Parameters are extracted from the measured S-parameters using an Agilent-EEsof IC-CAP2006. In order to be compiled and linked to an Agilent ADS2005A, the source-code of the proposed model is developed in Verilog-A and implemented using the ADS circuit simulator (hpeesofsim).

In order to check the fitting ability of the proposed large-signal model, the RMS error is introduced as follows:

$$\text{RMS\_target} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}[M(i)]^2} \tag{8}$$

$$\text{RMS\_error} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\frac{[S(i)-M(i)]^2}{(\text{RMS\_target})^2}} \tag{9}$$

where N is the total number of data points, and $S(i)$ and $M(i)$ are the ith simulated and measured data points.

DC and S-parameter simulation are implemented to verify the accuracy of the model. In Fig. 5 the drain current I_{DS} and output conductance G_{DS} at various gate voltages are plotted. We can observe that the simulated and measured results achieved excellent agreement. We can observe in Fig. 5 (a), as V_{DS} exceeds 9V, I_{DS} begins to ramp up beyond normal current operating level, which means the device is entering the weak-avalanche region. In order to avoid the breakdown of the device, we stop at 10V in the measurement. The self-heating effect is taken into account in our model and accurately simulated, as well as the weak avalanche effect, as shown in Fig. 5 (a). Thus, the saturation regime is well described by our model. At high gate and drain voltage conditions, where the effect of the gate extending over the drift region is significant, the model also shows good accuracy. Figure 6 shows the measured and simulated I_{DS} and transconductance G_M versus V_{GS}. We observe that the model describes the subthreshold current accurately and in a smooth manner also at the transition from

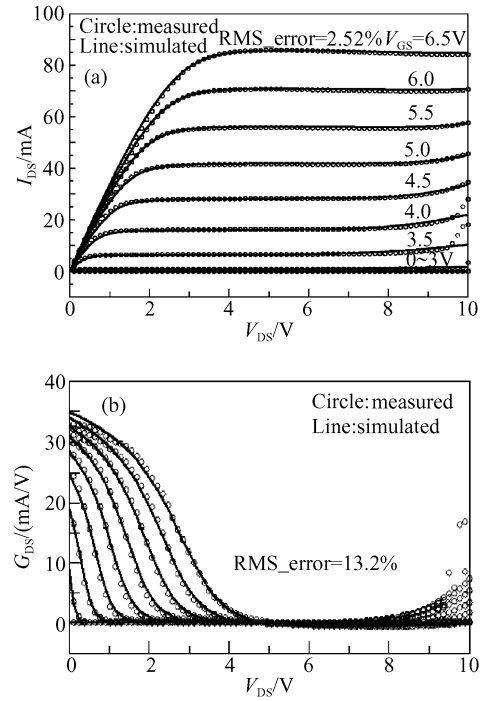

Fig. 5　Comparison of measured and simulated I_{DS} versus V_{DS} (a) and drain-conductance G_{DS} versus V_{DS} (b) characteristics (V_{DS}: 0 to 10V, Step: 0.1V; V_{GS}: 0 to 6.5V, Step: 0.5V; V_S = 0V)

the weak to strong inversion regime. In Fig. 7, ten sets of simulated S-parameters agree well with their measured S-parameters from 10MHz to 20.01GHz. Good agreement verifies that all parameters extracted through our technique are accurate and reliable.

For large-signal models, a common validation method is the comparison between measured and modeled load-pull data[17]. Hence, the power characterizations measurement has been implemented on a focus microwaves multiharmonic passive load-pull bench based on automated tuners. This bench enables the control of the source and load impedances presented to the device at the fundamental frequency, and the second and the third harmonic frequencies, independent from each other. The optimal source and load

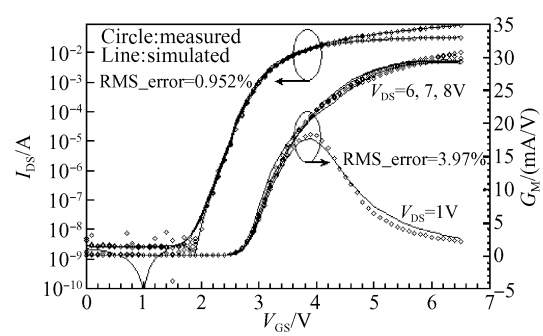

Fig. 6　Comparison of measured and simulated I_{DS} versus V_{GS} and transconductance G_M versus V_{GS} characteristics (V_{DS}: 1, 6, 7, 8V; V_{GS}: 0 to 6.5V, Step: 0.1V; V_S = 0V)

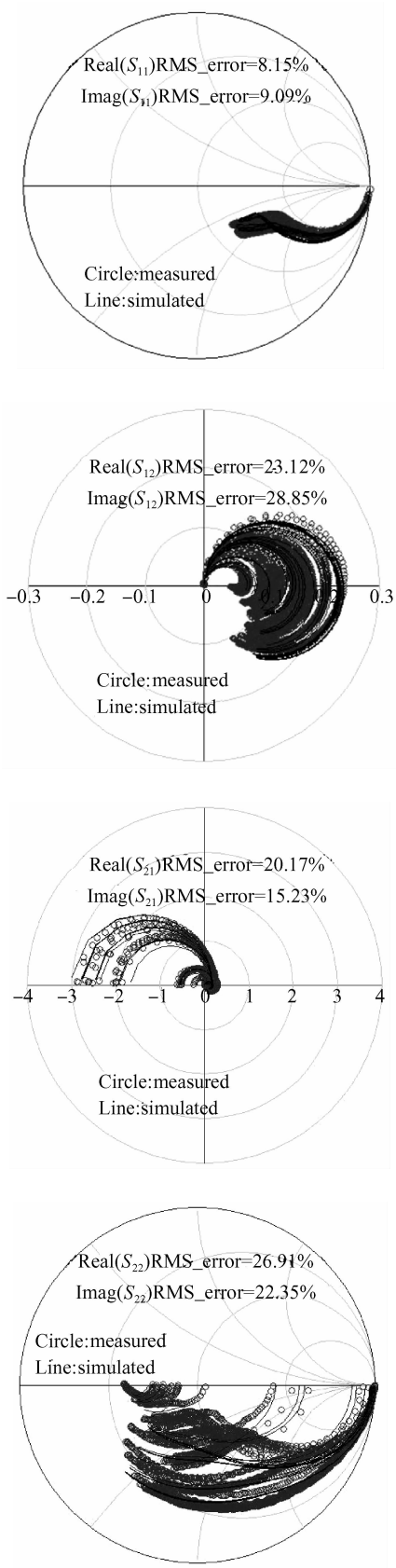

Fig. 7 Comparison of measured and simulated S-parameters (Frequency: 10MHz to 20.01GHz, Step: 100MHz; V_{GS}: 0 to 7V, Step: 1V; V_{DS}: 0 to 8V; Step: 2V; V_S = 0V)

impedances are $Z_S = 70 - j13\Omega$ and $Z_L = 68 - j54\Omega$. The fundamental frequency, gate-source, and drain-source voltage have been set to 900MHz, 5V, and 7V, respectively. The input power swept from −6.25 to 15.2dBm, with steps of 1.01dBm. The input, output, and second and third harmonic powers are measured. As is shown in Fig. 8, the measured and simulated output power and the second harmonic power are in reasonably good agreement. The simulated third harmonic power is matched to measured data in trend, though there is a slight deviation in slope.

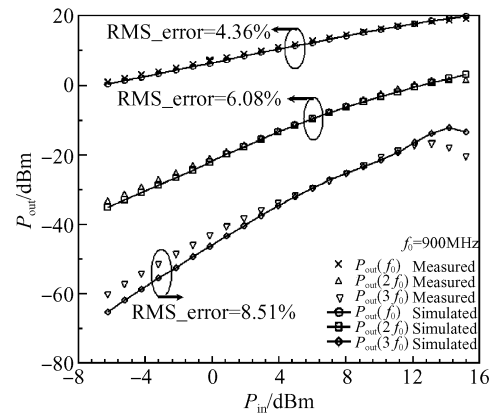

Fig. 8 Measured and simulated fundamental, 2nd and 3rd harmonics power characteristics

5 Conclusion

A novel large-signal equivalent circuit model of RF-SOI LDMOS based on MM20, which is a surface-potential-based physical compact LDMOS model, has been developed. MM20 is improved for RF-SOI LDMOS large-signal applications. MM20 has a much smaller set of parameters (55 for the miniset) due to its physical basis, among which only about 20 parameters have high sensitivity during the fitting process. Thus the intrinsic parameters can be extracted quickly and accurately. All the RF parasitic effects are taken into account. The parasitic elements are analytically extracted from the measured zero-bias S-parameters and quickly determined with necessary optimization steps. A 20-fingers-gate SOI LDMOS is measured to verify the proposed model. Excellent correspondence has been achieved. Self-heating and weak avalanche effects are accurately modeled in the DC condition. The good agreement of measured and simulated small-signal S-parameters for wide bias conditions with frequency range from 10MHz to 20.01GHz shows that the extracted RF parasitic and intrinsic MM20 parameters are accurate and reliable. To verify the new large-signal model, the power characterization measurement has been implemented on a Focus Microwaves multiharmonic passive load-pull bench based on automated tuners. The result shows this model pre-

dicts the fundamental and harmonic power precisely, indicating that our model is well suited for nonlinear RF circuit design with SOI LDMOS. Because MM20 only describes avalanche current empirically and there is no description for the charge in weak avalanche region, the presented model is valid in all operating regimes from the linear to saturation regime, except the weak avalanche region for RF applications. The source-code of the proposed model is developed using the Verilog-A referring to Ref. [18] so as to be compiled and linked to an Agilent ADS2005A and implemented using the circuit simulator hpeesofsim.

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基于 MOS Model 20 的 RF-SOI LDMOS 大信号建模*

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摘要： 提出了一种新的基于 Philips MOS Model 20 (MM20) 的 RF-SOI (radio frequency silicon-on-insulator) LDMOS (laterally diffused MOS) 大信号等效电路模型. 描述了弱雪崩效应以及由热效应引起的功率耗散现象. 射频寄生元件由实验测得的 S 参数解析提取，并通过必要的优化快速准确地获得最终值. 模型的有效性是通过一 20 栅指 (每指栅长 $L=1\mu$m，宽 $W=50\mu$m) 体接触高阻 RF-SOI LDMOS 在直流，交流小信号和大信号条件下的实验数据验证的. 结果表明，直流、S 参数 (10MHz～20.01GHz) 以及功率特性的仿真和实验测得数据能够很好地拟合，说明本文提出的模型具有良好和可靠的精度. 本文完成了对 MM20 在 RF-SOI LDMOS 大信号应用领域的拓展. 模型由 Verilog-A 描述，使用 ADS (hpeesofsim) 电路仿真器.

关键词： RF-SOI LDMOS；大信号模型；MOS Model 20；谐波功率；Verilog-A

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