Nested Miller Active-Capacitor Frequency Compensation for Low-Power Three-Stage Amplifiers

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Abstract: A new frequency compensation technique for low-power, area-efficient multistage amplifiers is introduced. Using nested active capacitors, our scheme achieves better bandwidth-to-power and slew-rate-to-power performances than previous works. Implemented in standard 0.35μm CMOS technology, our three-stage amplifier achieves 105dB DC gain, 3.3M GBW, 68° phase margin, and 2.56V/μs average slew rate under a 150pF capacitive load. All of these are realized with only 40μW power consumption under a 2V power supply, with very small compensation capacitors.

Key words: multistage amplifier; frequency compensation; low power
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1 Introduction

In recent years, the frequency compensation of multi-stage amplifiers for driving large capacitive loads under a low-power condition has been extensively investigated[1~3]. There exist two categories of basic compensation structures, namely NMC-[4~8] (nested-Miller) and RNMC-[9] (reversed-nested-Miller) for three-stage amplifiers (shown in Fig. 1). Among them, TCFC[8] introduced a transconductance with capacitances feedback to the traditional NMC structure such that a left-half-plane zero is generated, resulting in better phase margin. On the other hand, the low-power RAFFC proposed in Ref. [9] also used an active feedback in the conventional RNMC structure. This configuration can have the same effect as in the TCFC structure. Performance improvements with respect to bandwidth-to-power and slew-rate-to-power have been achieved by these modifications. In NMC- and RNMC- based designs, they have achieved their respective best performances.

However, typically the transconductance (bias current) of the third stage of a three stage amplifier is much larger than that of the first and the second stages, especially for driving large capacitive load. RNMC shows inherent bandwidth extension over NMC because the inner compensation capacitor does not load the output node[9]. But it requires the third stage to be non-inverting, which means a two-current-branch implementation (Fig. 2(a)) and higher current consumption than its NMC counterpart (Fig. 2(b)).

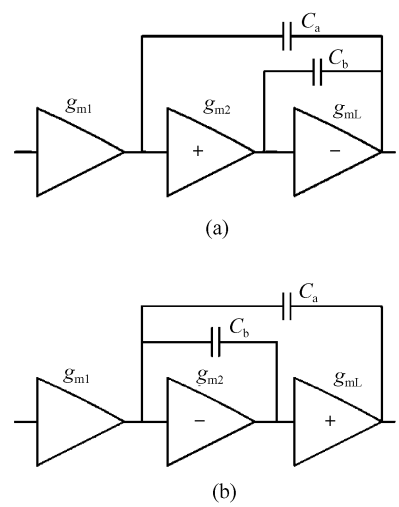

Fig. 1 (a) NMC structure; (b) RNMC structure

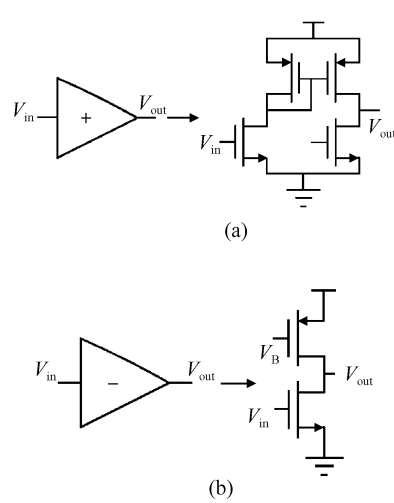

Fig. 2 Transistor level implementation of a non-inverting stage (a) and an inverting stage (b)

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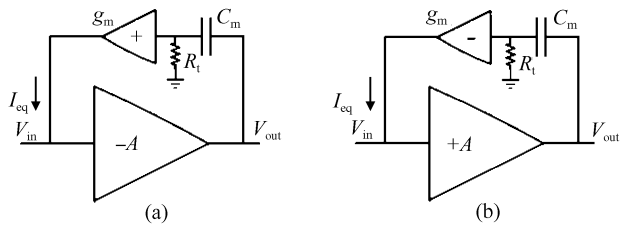

Fig. 3　(a) Current buffer; (b) Proposed active capacitor used between a non-inverting gain stage

In this paper, we develop a new topology that consumes nearly half the current in the third stage while not affecting the performance of the RNMC. By applying active capacitors to construct the reversed nested-Miller structure rather than their passive counterparts, an inverted third stage takes the place of a non-inverted one to realize the Miller effect, thus resulting in a one-branch third-stage instead of a two-branch one. Moreover, our scheme removes the dependence of circuit performance on parasitic parameters, as is unavoidable in most active-feedback based compensation schemes[4~6,8,9]. Meanwhile, the required compensation capacitor size of our scheme is reduced to a great extent. Comparisons with the latest NMC- and RNMC-based approaches reveal the significant performance improvements of our proposal in terms of both bandwidth-to-power and slew-rate-to-power efficiency.

2　Current buffers in Miller compensated circuits

Current buffers (Fig. 3 (a)) have long been used to enhance the performance[4~6,8,9] of three-stage amplifiers and reduce the compensation capacitor size in Miller compensated circuits such as LDOs[11]. An inverting gain stage is required in order to produce the Miller effect. In fact, the current buffer can be designed to be inverted, allowing a non-inverted gain stage to generate the Miller effect. The circuit level implementation of the inverted current buffer is shown in Fig. 4.

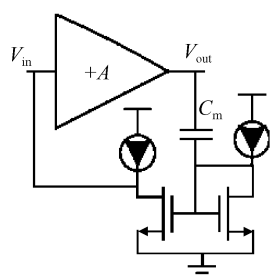

Fig. 4　Circuit level implementation of Fig. 3(b)

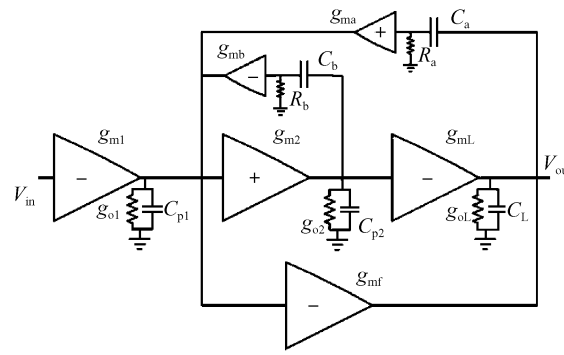

Fig. 5　NMAC structure

3　Proposed compensation technique

The proposed nested Miller active-capacitor frequency compensation (NMAC) structure is shown in Fig. 5. $C_{p1,2}$ represent the parasitic capacitors and C_L is the load capacitor. The two feedback loops are based on the structures depicted in Figs. 3(a) and 3 (b), respectively. A feedforward stage g_{mf} is also introduced to improve the large-signal performance without affecting the small-signal characteristics. By assuming that the gain of each stage is much greater than 1 and C_a, C_b, C_{p1}, and C_{p2} are much smaller than C_L, which is always the case, the transfer function is given by

$$A(s) = \frac{A_{dc}(1 + s/\omega_2)(1 + s/\omega_3)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + \frac{s}{\omega_1} + \frac{s^2}{\omega_1\omega_2}\right)} \tag{1}$$

where

$$A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_{oL}} \tag{2}$$

$$p_{-3dB} = \frac{g_{o1}g_{o2}g_{oL}}{k_a C_a g_{m2} g_{mL}} \tag{3}$$

$$\omega_1 = \frac{k_a C_a}{k_b C_b} \times \frac{g_{mL}}{C_L} \tag{4}$$

$$\omega_2 = \frac{g_{ma}}{C_a} \tag{5}$$

$$\omega_3 = \frac{g_{mb}}{C_b} \tag{6}$$

$$k_a = g_{ma} R_a \tag{7}$$

$$k_b = g_{mb} R_b \tag{8}$$

Unlike some other compensation techniques[4~6,8], no parasitic elements appear in our transfer function, and thus the design is more robust against process variations.

In order to achieve a significant bandwidth extension, $k_a C_a$ is set to be much larger than $k_b C_b$ as indicated in Eq. (4). As explained later, g_{ma} and g_{mb} can be implemented inherently into the circuit. For matching considerations, we set $k_a = k_b$, $g_{ma} = g_{mb}$, so ω_3 is much smaller than ω_2 and will be neglected in the analysis. The transformation function can thus be

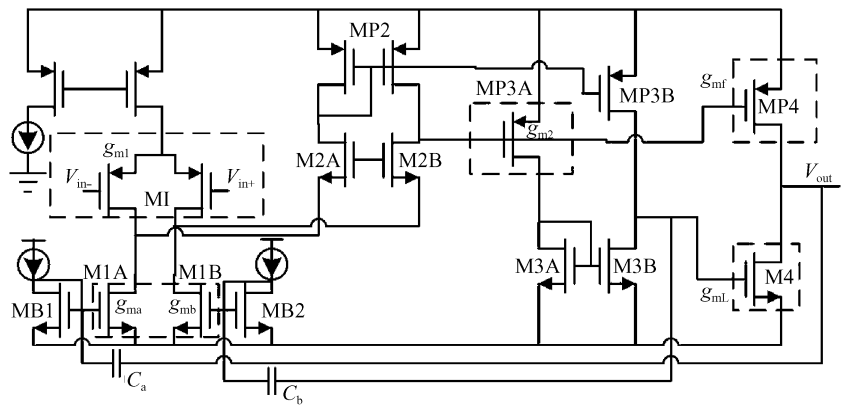

Fig. 6 Circuit level implementation of NMAC structure

approximately expressed as

$$A(s) \approx \frac{1 + s/\omega_2}{\frac{s}{\omega_{UG}}\left(1 + \frac{s}{\omega_1} + \frac{s^2}{\omega_1\omega_2}\right)} \tag{9}$$

where $\omega_{UG} = g_{m1}/k_a C_a$ is the unity-gain bandwidth. Equation (9) indicates that except for the dominant pole, there still exist an LHP zero ω_2 and a pair of conjugate complex left-half-plane (LHP) poles:

$$p_{2,3} = \frac{\omega_2}{2} \pm j\frac{\omega_2}{2}\sqrt{4\frac{\omega_1}{\omega_2} - 1} \tag{10}$$

The phase margin can be expressed as

$$PM = 180^\circ - \arctan\left(\frac{\omega_{UG}}{p_{-3dB}}\right) - \arctan\left\{2\zeta\frac{\omega_{UG}}{|p_{2,3}|}\Big/\left[1 - \left(\frac{\omega_{UG}}{|p_{2,3}|}\right)^2\right]\right\} + \arctan(\omega_{UG}/\omega_3) \tag{11}$$

By choosing

$$\omega_2 = 2\omega_{UG} \tag{12}$$

to avoid additional poles in the passband of the amplifier[5] and for a phase margin of 60°, we have:

$$\omega_2 = 1.72\omega_1 \tag{13}$$

Based on Eqs. (12) and (13) and other specifications such as GBW and load capacitor, the design parameters can be calculated:

$$g_{ma} = \frac{2}{k_a} g_{m1} \tag{14}$$

$$\frac{k_a C_a}{k_b C_b} \times \frac{g_{mL}}{C_L} = 1.72\frac{g_{m1}}{k_a C_a} \tag{15}$$

g_{m2} does not appear in the above equations, so its value is mainly determined by slewing constraints. Thus, the current distributed at this stage can be ultra small.

4 Circuit implementation and performance comparisons

The transistor level implementation of the NMAC circuit is shown in Fig. 6. The two feedback transconductance stages are realized by MB1, MB2 and M1A, M1B, respectively, with C_a and C_b connected to the dio-connected MB1, MB2, which also serve as the bias for M1A, M1B. The aspect ratio between M1 and MB is set to 2 (k_a and k_b equal 2). In the second stage, the gate of MP3B is connected to the gate of MP2. This implementation simplifies the bias for the amplifier and also enhances the slewing performance of the second stage. As shown in Fig. 4, the feedforward stage g_{mf} is realized by MP4.

The proposed amplifier is laid out in CHARTERED 0.35μm mixed-signal CMOS technology (Fig. 7). Common-centroid layout is practiced in order to achieve better matching for the two Miller capacitors since the ratio between them is used to achieve the bandwidth extension, as shown in Eq. (4). Special attention has also been paid to the matching between M1 and MB. The post-layout simulation results of the open-loop frequency response and the step response (200mVpp input) under the unity-gain feedback configuration are shown in Fig. 8. A 150pF capacitive load is used for both configurations.

The performances of the amplifier under two load conditions are summarized in Table 1. In order to perform a fair comparison with the published compensation schemes, two widely accepted figure-of-merits (FOMs) are used[8]:

$$IFOM_S = (GBW \times C_L)/I_{TOT} \tag{16}$$

$$IFOM_L = SR \times C_L/I_{TOT} \tag{17}$$

Equation (16) shows the bandwidth-to-power performance and Equation (17) represents the slew-rate-

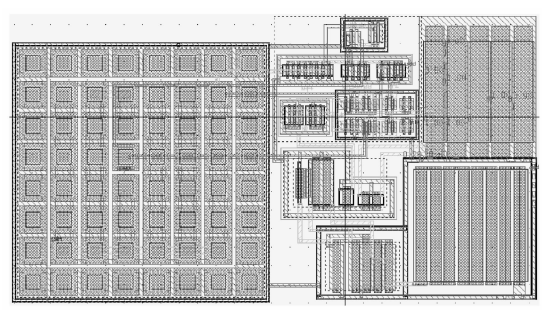

Fig. 7 Layout of the proposed amplifier

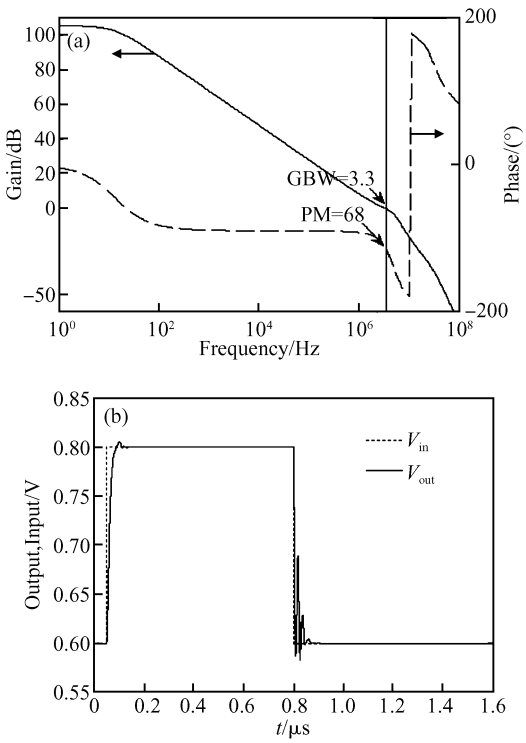

Fig. 8　Post-layout simulation results loaded with a 150pF capacitor　(a) Open-loop frequency response; (b) Step response under unity gain configuration with a 200mVpp input

to-power performance of the amplifier under a given capacitive load condition. The low-power RAFFC[9] and the TCFC structure[8] represent the latest RNMC and NMC based compensation schemes, respectively. The comparisons in Table 1 demonstrate that both the IFOMs and IFOML increase by 2 or 3 times, showing the superior performance of the proposed compensation scheme. Furthermore, the compensation capacitor sizes are also reduced, which means a significant reduction in die area.

Table 1　Performance summary and comparisons

	Year	C_L /pF	I_{TOT} /mA	Average slew rate /(V/μs)	GBW /MHz	Comp. cap. /pF	$IFOM_S$	$IFOM_L$
Low-power RAFFC[9]	2007	500	0.035	1.1	1.1	11 0.35	15714	18429
This work	—	500	0.020	1.84	1.8	0.96 0.02	45000	46000
TCFC[8]	2005	150	0.030	1.035	2.85	1.1 0.92	14250	5175
This work	—	150	0.020	2.56	3.3	0.7 0.02	24750	15360

5　Conclusion

A new frequency compensation technique for low-power operational amplifiers, namely NMAC, is proposed and analyzed. By using active Miller capacitors to compensate the three-stage amplifier in a nested way, the power consumption and the compensation capacitor sizes are significantly reduced while better performances are obtained. The post-layout simulation results verified its effectiveness. Comparisons with up-to-date compensation schemes are also given.

References

[1] Leung K N, Mok P K T. Nested Miller compensation in low-power CMOS design. IEEE Trans Circuits Syst II, 2001, 48(4): 388

[2] Leung K N, Mok P K T. Analysis of multistage amplifier-frequency compensation. IEEE Trans Circuits Syst I, 2001, 48(9): 1041

[3] Leung K N, Mok P K T, Ki W H, et al. Three-stage large capacitive load amplifier with damping-factor-control frequency compensation. IEEE J Solid-State Circuits, 2000, 35(2): 221

[4] Lee H, Mok P K T. Active-feedback frequency-compensation technique for low-power multistage amplifiers. IEEE J Solid-State Circuits, 2003, 38(3): 511

[5] Lee H, Mok P K T. Advances in active-feedback frequency compensation with power optimization and transient improvement. IEEE Trans Circuits Syst I, 2004, 51(9): 1690

[6] Lee H, Leung K N, Mok P K T. A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation. IEEE J Solid-State Circuits, 2003, 38(10): 1739

[7] Peng X, Sansen W. AC boosting compensation scheme for low-power multistage amplifiers. IEEE J Solid-State Circuits, 2004, 39(11): 2074

[8] Peng X, Sansen W. Transconductance with capacitances feed-back compensation for multistage amplifiers. IEEE J Solid-State Circuits, 2005, 40(7): 1515

[9] Grasso A D, Palumbo G, Pennisi S. Advances in reversed nested Miller compensation. IEEE Trans Circuits Syst I, 2007, 54(7): 1459

[10] Fan X, Mishra C, Sanchez-Sinencio E. Single Miller capacitor frequency compensation technique for low-power multistage amplifiers. IEEE J Solid-State Circuits, 2003, 38(10): 1735

[11] Rincon-Mora G A. Active capacitor multiplier in miller-compensated circuits. IEEE J Solid-State Circuits, 2000, 35(1): 26

用于低功耗三级放大器的嵌套式密勒有源电容频率补偿技术

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摘要：提出了一种新的用于低功耗，节省面积的三级放大器频率补偿技术.该技术将有源电容进行嵌套连接从而克服了传统的嵌套式密勒补偿与反嵌套式密勒补偿的缺点.当将这一技术用标准的 0.35μm 工艺设计成电路并负载 150pF 电容时，放大器实现了 105dB 直流增益，3.3M 的增益带宽积，68°相位裕度以及 2.56V/μs 的平均转换速率.而这一切的实现是在 2V 电源电压下仅消耗 40μW 的功耗以及使用了很小的补偿电容.

关键词：多级放大器；频率补偿；低功耗

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