A Double High-Voltage p-LDMOS and Its Compatible Process for PDP Scan-Driver ICs*

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Abstract: A high-voltage p-LDMOS(HV-pMOS) with field-oxide as gate dielectric and a RESURF drain drift region to undertake high gate-source voltage and drain-source voltage for the scan driver chip of plasma display panels (PDP) is purposed based on the epitaxial bipolar-CMOS-DMOS (BCD) process. The key considerations and parameters of the design are discussed: the thickness of gate dielectrics is 1mm and the area of the device is 80μm $\times$80μm. Only 18 photoetching steps are needed in the developed process, which is compatible with standard CMOS, bipolar, and VDMOS devices. The breakdown voltage of the HV-pMOS in the process control module (PCM) is more than 200V. The results are favorable for 170V PDP scan driver chips, which contribute to the competitive cost efficiency.

Key words: PDP; HV-PMOS; BCD process; thick gate-oxide; cost-effective
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1 Introduction

PDP is one of the main display devices and will be competitive in future trends[1~3]. The high-voltage display driver chip of the PDP is always a potential element for lowering its cost and improving its competitiveness. Several different technology routes and their roadmaps have co-occurred in their respective driver chips[4~9]. Silicon epitaxial BCD technology is popular for its balance of performance and cost, which is quite suitable for competitive PDP products. HV-pMOS is usually integrated as the chip level shift part and the power output part, which plays a leading role in the whole chip area with the long-term trends of high definition PDP continuous development, and more power outputs need to be integrated in a single driver chip[8].

The HV-pMOS with field-oxide as gate dielectrics developed in this paper for PDP driver applications is under the following considerations:

(1) It should be adequate for driving the equivalent capacitive load of a specific PDP.

(2) It should have excellent compatibility with other transistors (such as CMOS, bipolar, DMOS, and diode), while having high drain-source voltage (V_{ds}) and gate-source voltage (V_{gs}).

(3) The efforts on the area of the HV-pMOS module in the driver chip and the efforts on the fabricating process complexity should be effective and available.

2 Device and technology

Usually and necessarily, for power integrated circuits with high gate-source voltage application, there is a specific process to form the thick gate-oxide[10] and to undertaking the high gate-source voltage. In this paper, an HV-pMOS with field-oxide as the gate dielectric is purposed so that the specific thick gate-oxide is omitted. Another key point is the epitaxial BCD process developed here, which provides compatibility with different device modules, such as VDMOS[9] and the low voltage BiCMOS (bipolar CMOS) module, is simplified and optimized.

Altogether, the above considerations contribute to the cost efficiency of the whole HV-pMOS module for PDP drivers. Below, we will disclose these design issues.

2.1 Structure

A complete HV-pMOS is shown in Fig. 1, in which an n-type epitaxial layer (n-epi) is deposited on p-type substrate. The n-buried layer connects to the bottom-sinkers of other devices such as VDMOS and npn transistors for reducing on-resistance, and here it

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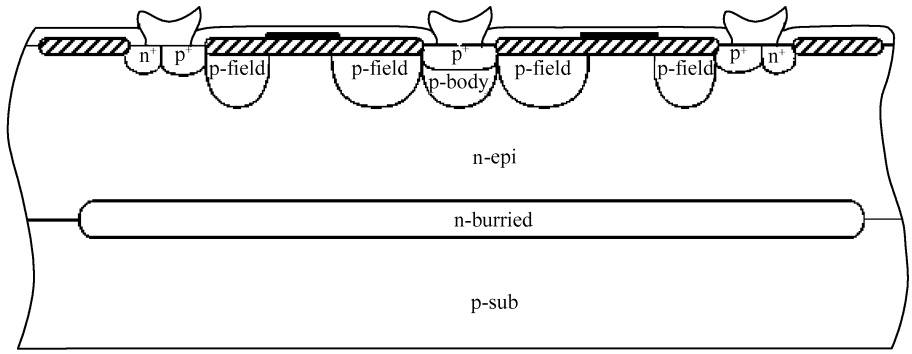
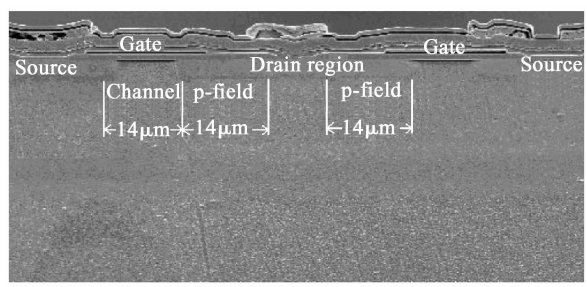
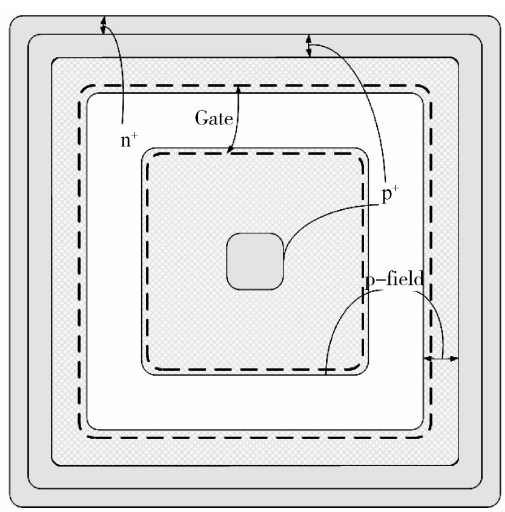


(a)



(b)



(c)

Fig. 1　Structure of the field-oxide HV-pMOS　(a) Schematic structure; (b) Cross-section SEM image; (c) Top view

can improve the electric field distribution of n-epi for the HV-pMOS in the BCD power integration technology. The drain drift region of the device is formed by the p-field layer and it is the key region to undertake the horizontal and vertical electric field, satisfying the RESURF principle. The poly-gate covers the channel on the top of the thick field-oxide, which is capable of high gate-source voltage of about 170V. The p-field layer also forms the source region as the connection between p^+ in the active region and channel because of the thick dielectric under edge of the poly-gate near the source active region. The drain region, the channel region, and the source region provide the main body of the *I-V* characteristics of the device. p-body p^+ and n^+ diffusion are fabricated by self-aligned technology in the drain and source active region; p^+ diffusion forms the source electrode, butting connected with n^+ diffusion in the source active region, and n^+ diffusion also provides electric potential of n-epi; p-body is to increase the radius of the cylinder curvature of p^+ in the drain active region to reduce the electric field intensity of the p^+ shallow junction. The cross sectional SEM image of actual HV-pMOS in PDP scan-driver chip is shown in Fig. 1(b).

The corresponding layout of the device is shown in Fig. 1(c). The drain region is located at the center of the device, surrounded by a closed channel and source region, so that the high voltage drain is isolated

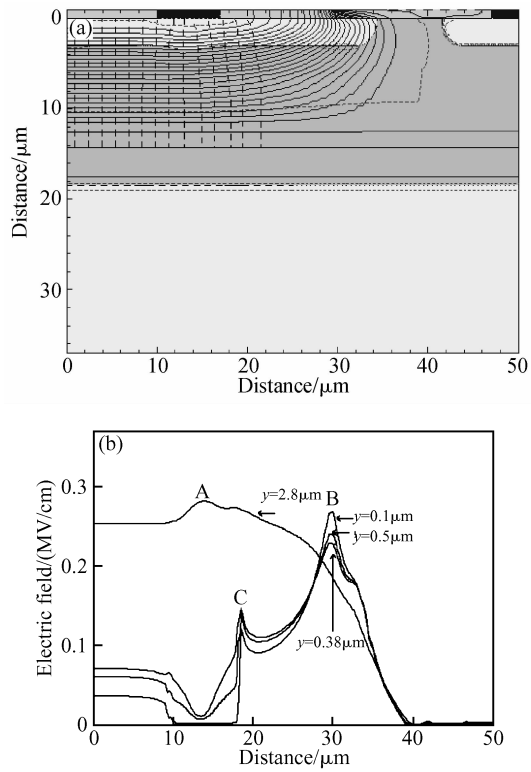


Fig. 2 Electronic solutions for the structure in Fig. 1 (a) Electrical potential distribution; (b) Electric field intensity

to the outside. In this racetrack layout, the parameters should be designed carefully, which is essential to *I-V* characteristics, parasitic effects, and safe operating area, such as secondary breakdown and the Kirk effect[11].

Figure 2 (a) shows the electrical potential distribution of the structure in Fig. 1 under the condition of $V_{ds} = -243$V, $V_{gs} = 0$V. It selects the typical right part of the 2D cross-section to reduce the calculation amount. The equipotent-lines, as shown in Fig. 2, distribute in the p-n junction of the drain drift region and the lines under the drain region are almost horizontal under the effects of the horizontal electrical potential of the n-buried layer. The p-field layer for the drain drift is depleted completely and the lines there are almost vertical under the effects of the lateral electrical potential.

Figure 2(b) gives the distribution of electric field intensity at typical vertical locations, corresponding to the solution of Fig. 2(a). It shows the following design considerations and methods:

(1) The maximum value of the electric field intensity in Fig. 3 occurs at $x = 13.7\mu$m, $y = 2.8\mu$m, corresponding to the internal cylinder region of the p-body, as can be observed in Fig. 2. Thus, the most possible breakdown location is inside the device.

(2) The height of the two electric field peaks "A" and "B" are almost equal, showing an optimized

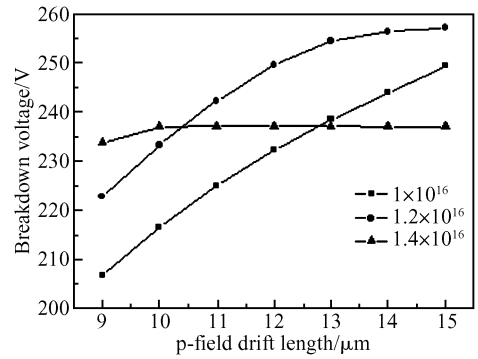


Fig. 3 V_{br} versus L_{dt} $L_{ch} = 14\mu$m, $J_{dt} = 14\mu$m

result between internal and surface electric field, which contributes to entire performance and area.

(3) The surface electric field at $y = 0.1\mu$m has two peaks; one is at the edge of the gate, and the other is at the right edge of p^+. The area under the two peaks is almost equal to the maximum voltage, showing that the surface electric field is optimized by the RESURF principle.

2.2 Key optimization

The p-field drift in drain region and the thickness of dielectric under the gate, which is formed by field-oxide, are both essential for high V_{ds} and V_{gs} HV-pMOS. Figures 3～5 give the tendencies and optimizations of the key parameters. For convenience, the following voltage magnitudes are presented as absolute values.

First, the relation between breakdown voltage (V_{br}) and drift length (L_{dt}) of drain region is shown in Fig. 3. Supposing that the channel length is 14μm, i.e., $L_{ch} = 14\mu$m, and that the junction depth of the drift is 3μm, $J_{dt} = 14\mu$m, and the three curves correspond to different drift concentrations. When the drift is depleted completely by the vertical and lateral electric field, the V_{br} increases as the drift length increases, corresponding to the curves of 1×10^{16} and 1.2×10^{16} cm^{-3}. This shows that the sharing electric charge of drift does not satisfy the requirement[12]. When the drift is depleted partially, the peak electric field occurs near the surface of the drift boundary and the V_{br} is almost unchanged with the drift concentration, corresponding to the curve of 1.4×10^{16}cm^{-3}.

Second, for the design of the HV-pMOS in the framework of the proposed structure, the concentration of the drift (C_{dt}) and the junction depth of the drift (J_{dt}) are quite important for improving surface field at the device terminal, which is depleted and agrees with the RESURF principle in the optimized design. The parameters of the channel are also quite important for the punch-through of the devices, which

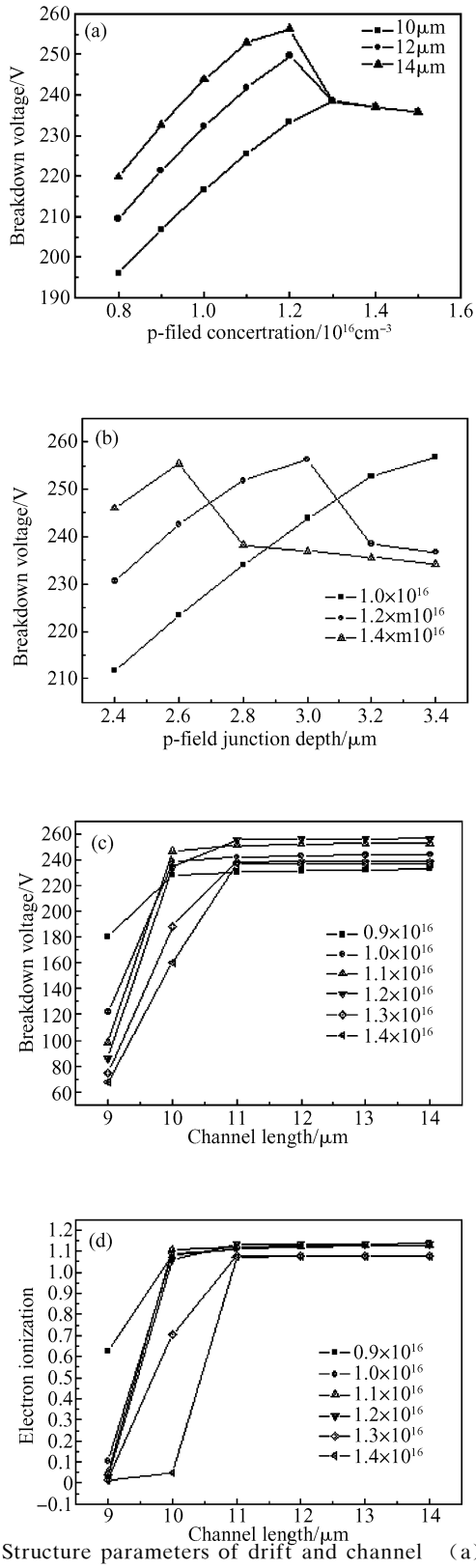


Fig. 4　Structure parameters of drift and channel　(a) Breakdown voltage V_{br} versus drift concentration C_{dt}; (b) V_{br} versus drift junction depth J_{dt}; (c) V_{br} versus channel length L_{ch}; (d) Electron ionization $\int \alpha_e$ versus L_{ch}

is charged for the safe operation range. Figure 4 shows the curve of the optimized parameters and corresponding results. For 170V gate-source dielectric

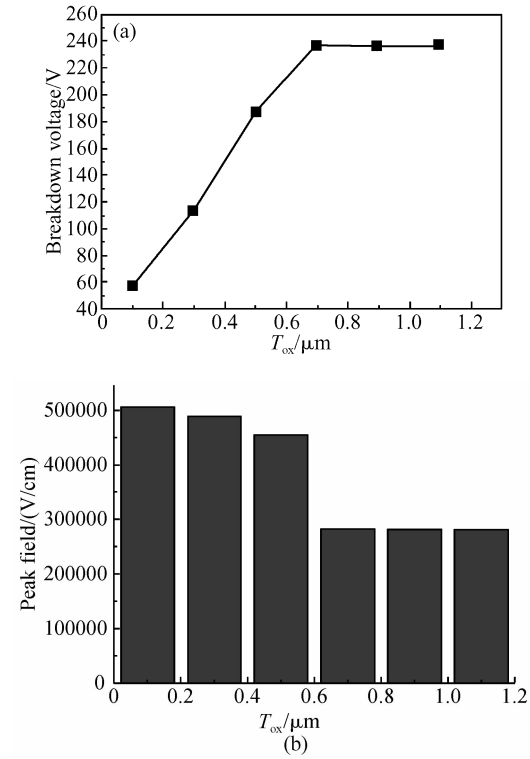


Fig. 5　Influence of field-oxide thickness (T_{ox}) on the device (a) V_{br} versus T_{ox}; (b) E_m versus T_{ox}

breakdown voltage, the thickness of 200nm for the oxide dielectric is enough. However, the thickness is also important for the breakdown voltage inside device, such as the drain-source breakdown voltage. Figure 5 shows the influence of field-oxide thickness on the breakdown voltage and surface peak electric field of the device. As a field plant on the other hand, the gate electrode strongly affects the surface electrical potential distribution and electric field intensity in a certain range of the thickness of the field oxide. Here the lower limit could reach the breakdown of the device.

2.3　Process

The process is based on BCD compatible technology, adopting epitaxial silicon material. The process flow is shown in Fig. 6, and only a few more layers are included than in the common BiCMOS process, as Table 1 shows.

3　Results

We now give the design results of the proposed HV-pMOS, which apply to the PDP scan driver chip. Figure 7 (a) is an HV-pMOS testing structure in the process control module (PCM), and the area is 80μm ×80μm. We obtain the average values of the testing results on eight pieces of wafer (#13, #14, #16,

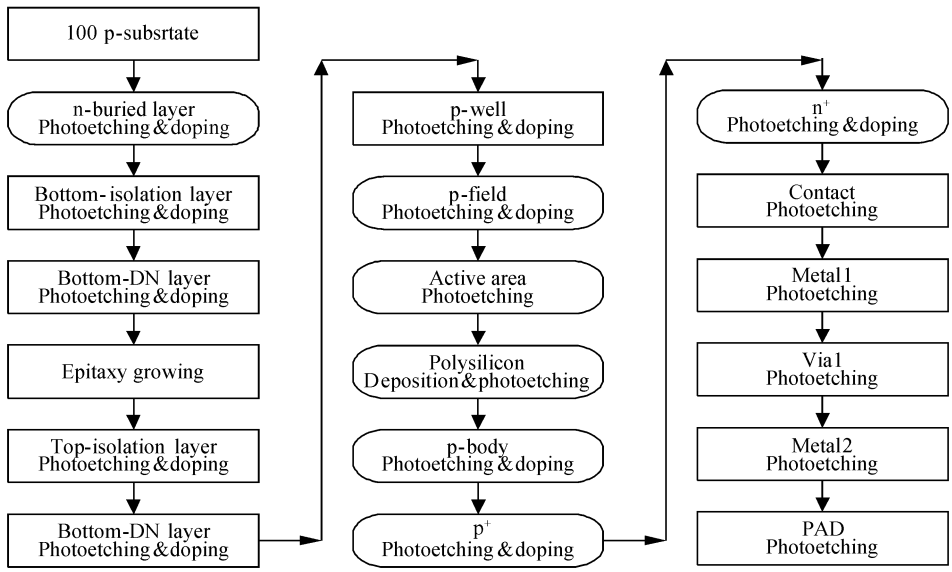


Fig. 6 Process flow of HVPMOS

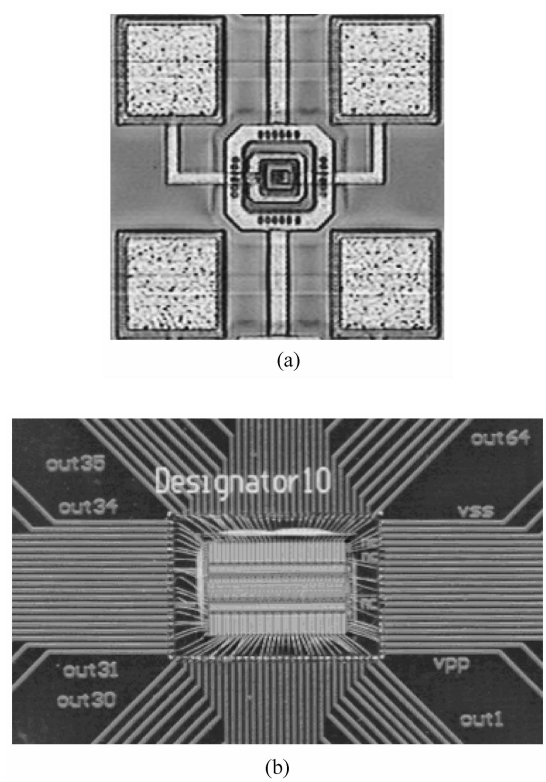
Table 1 Flow of BiCMOS versus compatibility BCD process developed suitable for the HV-pMOS proposed

	BiCMOS	BCD
1	p-sub	p-sub
2	n^+ bury layer	n^+ bury layer
3	isolation and drain	isolation and drain
4	pwell	pwell
5	active	active
6	/	p-field and n-field
7	gate	gate
8	/	p-body
9	p^+ and n^+	p^+ and n^+
10	contact	contact
11	metallization	metallization
12	pad	pad

＃18，＃20，＃21，＃22，＃24) as shown in Table 2 and all of the breakdown voltages are more than 200V for the power output transistors and level shift part. The HV-pMOS is integrated in the PDP scan driver chip. Figure 7(b) is the chip by PCB bonding.

4 Summary

We developed a cost-effective HV-pMOS based on silicon epitaxial BCD technology，which is compatible with 5V low voltage CMOS，5V bipolar transistors，high voltage VDMOS，and avalanche diodes for gate protection of power DMOS in the PDP driver chip. The breakdown voltage (V_{br}) of the HV-pMOS is more than 200V，online testing of the PDP LG-model-42v6 agrees with the design targets，and the design result also could be developed for other power integration circuits with consideration of the application requirements and corresponding parameter adjustment.



(a) (b)

Fig. 7 HV-pMOS test and application results (a) One of the HV-pMOS in PCM modules module；(b) Chip on the function testing by PCB bonding with proposed HV-pMOS

Table 2 Average values of testing results for the PCM in different wafers

Parameter	Average value
Threshold	5.5V
Transconductance	1.445μS
Saturated drain current	709.5μA
Leakage current	−26.2pA
On-resistance	646Ω

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用于 PDP 扫描驱动的双高压 p-LDMOS 及其兼容工艺*

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摘要：报道了基于硅外延 BCD 工艺的高栅源、高漏源电压的功率 pMOS 的设计. 采用 1μm 厚的场氧化层作为栅氧介质及 RESURF 原理优化的漏极漂移区，器件面积为 80μm×80μm，工艺上简化为 18 次光刻，兼容标准 CMOS、双极管和高压 VDMOS. 测试管耐压超过 200V，集成于 64 路 170V PDP 扫描驱动芯片，通过了上机测试.

关键词：PDP；HV-PMOS；BCD 工艺；厚栅氧；低成本
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