A Planar InGaAs/InP Geiger Mode Avalanche Photodiode with Cascade Edge Breakdown Suppression

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Abstract: A Geiger mode planar InGaAs/InP avalanche photodiode (APD) with a cascade peripheral junction structure to suppress edge breakdowns is designed by finite-element analysis. The photodiode breakdown voltage is reduced to 54.3V by controlling the central junction depth, while the electric field distribution along the device central axis is controlled by adjusting doping level and thickness of the InP field control layer. Using a cascade junction structure at the periphery of the active area, premature edge breakdowns are effectively suppressed. The simulations show that the quadra-cascade structure is a good trade-off between suppression performance and fabrication complexity, with a reduced peak electric field of 5.2×10^5 kV/cm and a maximum hole ionization integral of 1.201. Work presented in this paper provides an effective way to design high performance photon counting InGaAs/InP avalanche photodiodes.

Key words: Geiger mode APD; edge breakdown; cascade junction; breakdown voltage
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1 Introduction

Avalanche photodiodes (APDs) are very sensitive optical detectors, which find broad applications in quantum information, biomolecule detection, and astronomical research[1]. Among all device structures, the InGaAs/InP APD with separate absorption and multiplication areas (SAM) is widely accepted to detect infrared radiations (with wavelengths longer than 1μm), owing to the relatively narrow bandgap of InGaAs material. An important application of the APD is to detect single photons, when the photodiode is biased in the Geiger mode (i.e., above its breakdown voltage) and can amplify the single photon-induced current to a macroscopically detectable level[2]. Some results, e.g., large area single-photon APD at room temperature, or APD arrays, have been reported in recent years[3,4]. However, the rules for designing high performance planar InGaAs/InP Geiger mode APDs still require investigation.

A typical planar InGaAs/InP SAM APD and its electric field distribution along the central axis when the APD is biased close to the breakdown voltage are shown in Fig. 1. A 2.2μm-thick intrinsic InGaAs absorption layer is grown on InP substrate, where incident light is absorbed and initial electron-hole pairs are generated. The thickness of the n-type field control layer is 0.4μm with an impurity concentration of 7.0×10^{16} cm^{-3}. This layer is used to modulate the electric field profile along the central axis of the device. The upper 3μm thick lightly n-doped InP layer forms a pn junction together with the top p^+ InP layer doped by diffusion or ion-implantation, where an avalanche of carriers by impact ionization occurs. Between the absorption and multiplication layers, there is a very thin n-type InGaAsP grading layer used to smooth the valance band discontinuity between the InGaAs and InP materials and avoid "pile-up" of holes[5].

A critical position within the device is the InGaAs/InP hetero-interface, marked by K1 in Fig. 1. When photon-generated holes pile-up at the interface and recombine before jumping across the step by thermo-ionic emission, the APD detection efficiency could degrade. An InGaAsP grading layer is introduced to

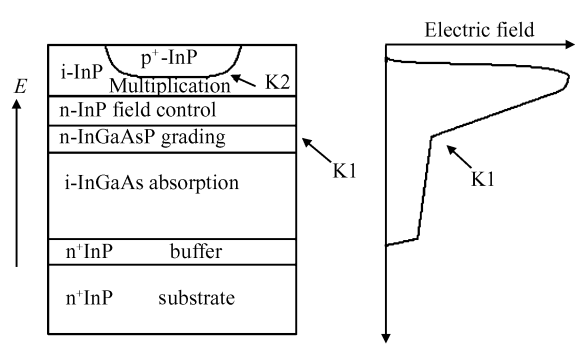

Fig. 1 A planar InGaAs/InP SAM APD and the electric field profile along its central axis

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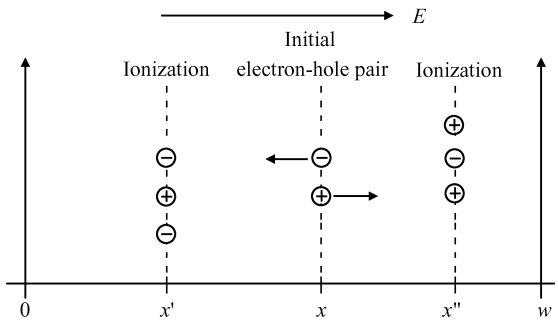

Fig. 2　Schematic of the ionization integral calculation

relieve this effect. The electric field E_{hi} at the hetero-interface should be greater than 80kV/cm. On the other hand, a high E_{hi} can increase the probability of tunneling effects and subsequently increase the dark counting rate. Therefore, the electric field at the hetero-interface should be kept below 200kV/cm[6]. Another key position is at the edge of the pn junction in the InP multiplication layer, marked by K2 in Fig. 1. Edge breakdown can occur prior to central breakdown because of the curvature effect[7]. Measures such as the guard ring structure[8] have been proposed to accomplish this.

When designing Geiger mode APDs, it is crucial to control the device breakdown voltage and monitor the electric field distribution throughout the device structure. With the above concerns in mind, in this paper, the design and simulation of a planar InGaAs/InP SAM APD structure is presented.

2　Device design and simulation

Cylindrical coordinates are used in the simulation. Because the structure is symmetrical along its central axis, only half of the mesh structure is necessary in calculation. Denser meshes are applied to regions with stronger electric fields, such as the multiplication layer and the junction edge region.

Ionization integrals are employed to analyze the breakdown characteristics of the APD. Figure 2 is a schematic picture of the ionization integral calculation.

The width of the depletion region is w. An initial electron-hole pair is generated at position x. When the free carriers travel a distance of $\mathrm{d}x$, impact ionized electrons and holes of $\alpha\mathrm{d}x$ and $\beta\mathrm{d}x$ will be generated, where α and β are the electron and hole ionization coefficients[9]. The total number of electron-hole pairs generated in the depletion layer at position x is[10]:

$$M(x) = 1 + \int_0^x \alpha(x')M(x')\mathrm{d}x' + \int_x^w \beta(x')M(x')\mathrm{d}x' \quad (1)$$

$M(x)$ is the multiplication factor of carriers, and can be solved from Eq. (1):

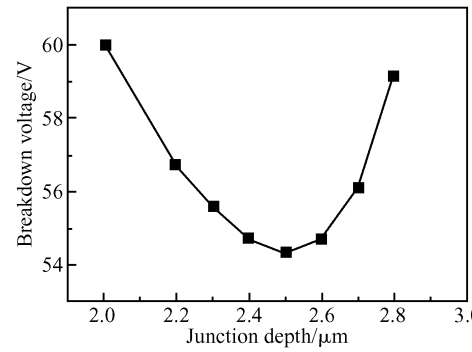

Fig. 3　Relation between the breakdown voltage and the junction depth

$$M(x) = \frac{\exp\left[-\int_x^w(\alpha-\beta)\mathrm{d}x'\right]}{1-\int_0^w \alpha\exp\left[-\int_x^w(\alpha-\beta)\mathrm{d}x'\right]\mathrm{d}x} = \frac{\exp\left[-\int_0^x(\beta-\alpha)\mathrm{d}x'\right]}{1-\int_0^w \beta\exp\left[-\int_0^x(\beta-\alpha)\mathrm{d}x'\right]\mathrm{d}x} \quad (2)$$

When the denominator is zero, $M(x)$ approaches infinity, which means breakdown occurs. Thus ionization integrals can be defined as[11]:

$$I_n = \int \alpha\exp\left[-\int_x^w(\alpha-\beta)\mathrm{d}x'\right]\mathrm{d}x \quad (3)$$

$$I_p = \int \beta\exp\left[-\int_0^x(\beta-\alpha)\mathrm{d}x'\right]\mathrm{d}x \quad (4)$$

The reverse bias at which either I_n or I_p equals unity is the breakdown voltage. The larger I_n or I_p is, the greater opportunity that breakdowns are triggered. Hence I_n and I_p are viewed as the monitoring indices for avalanche breakdowns[12].

The ionization integrals (I_n and I_p) calculated along each potential gradient path are commonly different from one another. In the simulation, the simulator calculates ionization integrals along every potential gradient path that passes at least one node of the simulation mesh within the device. By this mean, breakdown voltages in different regions of the device can be determined and the electric field distribution throughout the device can be obtained.

2.1　Breakdown voltage and electric field distribution control

As stated in section 1, in the planar APD structure shown in Fig. 1, the multiplication layer is formed by diffusion or ion-implantation. The breakdown voltage is a function of the pn junction depth, which can be adjusted in the fabrication process. Choosing a critical junction depth can reduce the breakdown voltage to the minimum, e.g., a 2.5μm junction depth yields a minimum breakdown voltage of 54.3V, as Figure 3 shows.

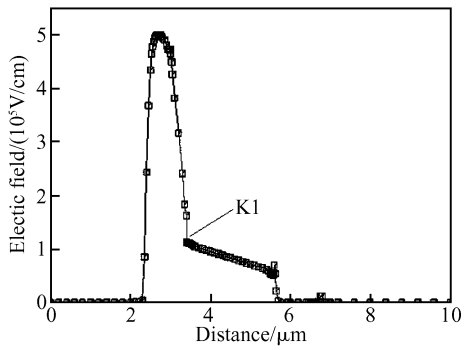

Fig. 4 Electric field profile along the central axis at the minimum breakdown voltage

The electric field distribution along the APD central axis is calculated and shown in Fig. 4. The doping level and thickness of the InP field control layer are also key parameters in controlling the electric field, and therefore should be selected carefully to meet the design criterion. In this simulation work, the doping level of the InP field control layer is set to 6×10^{16} cm^{-3} and the thickness is 0.4μm. As Figure 4 shows, when the APD is biased at that breakdown voltage, the electric field at the hetero-interface is approximately 110kV/cm, falling between 80 and 200kV/cm. This configuration is beneficial for both higher detection efficiency and lower probability of tunneling effects.

2.2 Edge breakdown suppression using a cascade structure

Figure 5 (a) shows the fundamental APD structure with no edge breakdown-suppressing measures. Its three-dimensional electric field distribution is shown in Fig. 5 (d). Compared to the central electric field of 5×10^5kV/cm, an extremely high level of peak electric field (E_{peak}) at 6.7×10^5kV/cm appears at the edge region. The hole ionization integral (I_p) can also be used to estimate the edge breakdown probability. They should be kept as small as possible in the peripheral region. The maximal I_p for the fundamental APD is 2.236, leading to a substantially greater probability that edge breakdowns will happen prior to central breakdowns when the photodiode is working in the Geiger mode.

A conventional way to suppress edge breakdown is to introduce one or more floating guard rings (FGRs) around the active area. Figure 5 (b) shows its structure. The spacing between the device central region and the guard ring is 3μm and the width of the ring is 4μm; the guard ring junction depth is 0.4μm shallower than the central junction. The corresponding electric field distribution is shown in Fig. 5 (e). Calculation shows that E_{peak} is 6.4×10^5V/cm and the maximum I_p is 1.791. This indicates that, compared to the fundamental device, the FGR reduces the peak electric field and the ionization integral in the edge region.

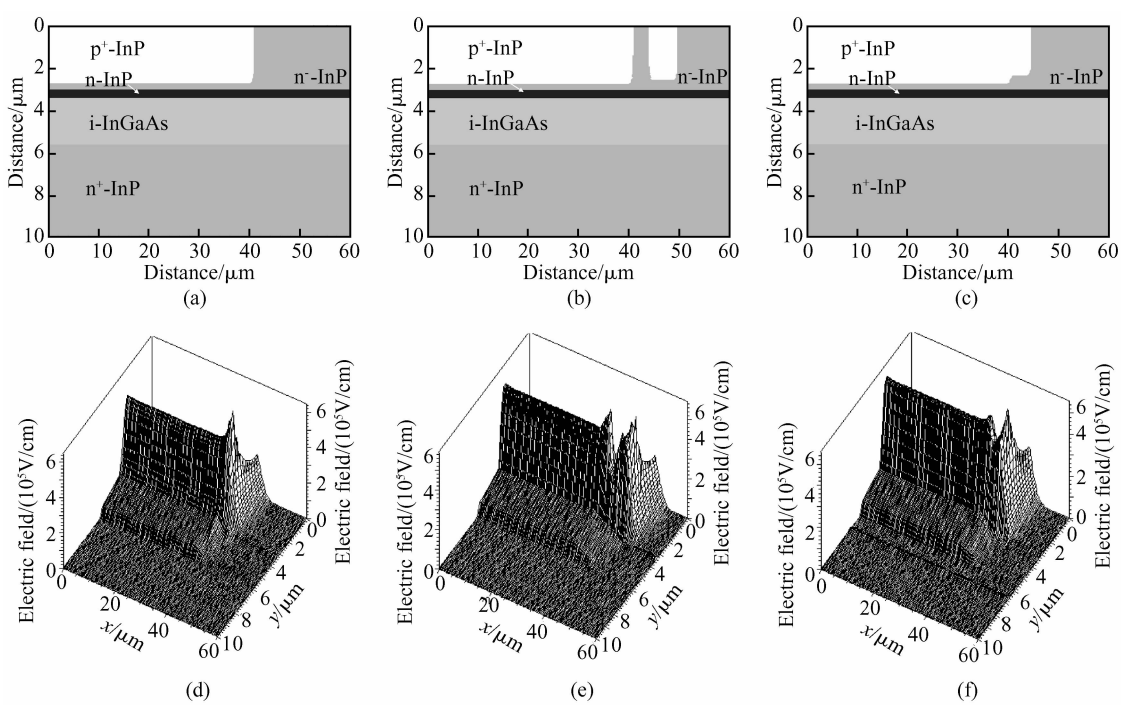

Fig. 5 Different active area edge structures and their electric field distributions (a), (d) Fundamental; (b), (e) Floating guard ring; (c), (f) Double-cascade

Table 1　Peak electric field (E_{peak}) and maximum hole ionization integral (I_p) of different device edge structures

Structure	Central junction edge		Peripheral junction edge	
	E_{peak} /(kV/cm)	Maximum I_p	E_{peak} /(kV/cm)	Maximum I_p
Conventional	6.7×10^5	2.236		
FGR	6.2×10^5	1.791	6.4×10^5	1.665
Double-cascade	5.5×10^5	1.332	5.7×10^5	1.466

In this paper, the cascade junction structure is proposed and its effect is simulated and compared with that of the FGR structure. Figure 5 (c) shows the device structure with two junction cascades. The central junction with a radius of 40μm is surrounded by a shallower junction at its periphery. The peripheral junction is 4μm wide and 0.4μm shallower than the central junction. The three-dimensional electric field distribution of this structure is shown in Fig. 5 (f), which justifies the fact that the outer shallower junction reduces the electric field at the edge of the central junction. This is also verified by the result that the maximal I_p at the edge of the central junction is reduced from the previous FGR value of 1.791 to 1.332, and E_{peak} from 6.4×10^5 to 5.5×10^5 V/cm. These results indicate that the junction cascade structure outperforms the conventional FGR when used for suppressing edge breakdowns. The simulation results are summarized in Table 1.

3　Optimized multi-cascade structure

Figure 6 (a) shows a variation of the above double-cascade structure. The depth difference between the central junction and the peripheral junction is reduced from 0.4 to 0.2μm. Figure 6 (d) shows its electric field distribution. E_{peak} and the maximum I_p at the edge of the central junction are further reduced to 5.3×10^5 kV/cm and 1.197, respectively. However, these values at the edge of the peripheral junction increase to 6.2×10^5 kV/cm and 1.827. Thus, a smaller depth difference between the two cascaded junctions yields a weaker peak electric field and ionization integral at the edge of the central junction at a cost of increased breakdown probability at the edge of the peripheral junction. This phenomenon suggests that by adopting a smaller depth difference between neighboring junction cascades while increasing the number of cascades, the edge breakdown suppression effect can be further enhanced. Figure 6 shows the device edge structure and corresponding electric field distribution with two, three, and four junction cascades. An outer junction is always 0.2μm shallower than its inner neighbors for all these configurations.

The simulation results shown in Table 2 indicate that the electric field and the ionization integral are

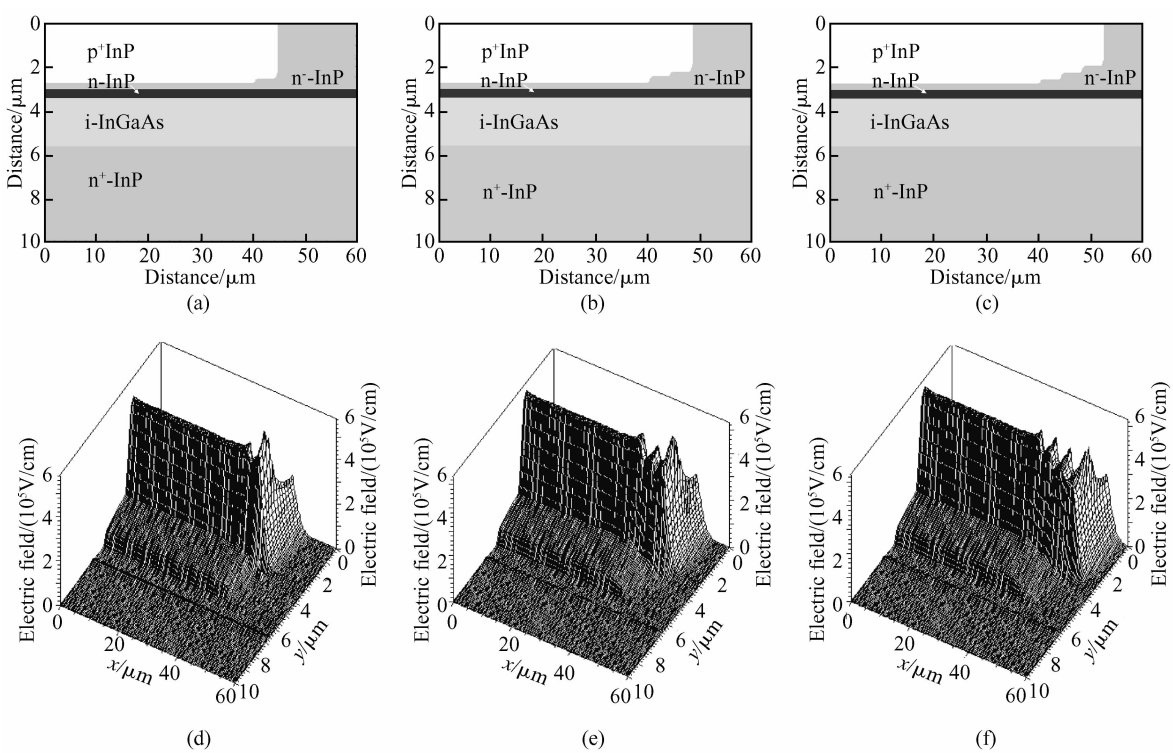

Fig. 6　Different cascade edge junction structures and their corresponding electric field distributions　(a), (d) Double-cascade, structure A; (b), (e) Triple-cascade, structure B; (c), (f) Quadra-cascade, structure C

Table 2 Peak electric field (E_{peak}) and maximum hole ionization integral (I_p) of the central and peripheral junction edges for the double, triple, and quadruple cascade structures

Structure	Central junction edge		Peripheral junction edge	
	E_{peak} /(kV/cm)	Maximum I_p	E_{peak} /(kV/cm)	Maximum I_p
2-cascade	5.3×10^5	1.197	6.2×10^5	1.827
3-cascade	5.4×10^5	1.264	5.6×10^5	1.443
4-cascade	5.3×10^5	1.219	5.2×10^5	1.201

significantly reduced at the peripheral junction edge by the multi-cascade structures. Among them, the quadra-cascade structure with a maximum I_p of 1.22 is regarded as the optimized design with balanced performance between the edge breakdown suppression effect and fabrication complexity.

4 Experiment

Results on the double-cascade structure, or the standoff structure, have already been reported in the literature[6,13]. Fabrication techniques such as multi-step diffusion or ion-implantation can be used to form the edge cascade pn junction. As adopted in this paper, a convenient way is to etch the InP surface to form the cascade recess before doping.

Figure 7 shows the simplified fabrication steps to form the cascade junction. A SiO_2 mask is deposited on the top surface of the InP substrate, then a window for etching is opened by photolithography (a). A certain depth of the surface InP, which is exactly the value of the cascade step, is removed by either dry etching or wet etching (b). A similar process occurs in the following steps with the only exception that the etching window is larger than the first one and forms a second cascade (c, d). Either Zn diffusion or Be ion-implantation can now be employed to form the p^+ region, using the deposited SiO_2 film as a doping mask (e). The cascade edge pn junction forms according to the surface structure. The above steps can be repeated to form multi-cascade structures if required.

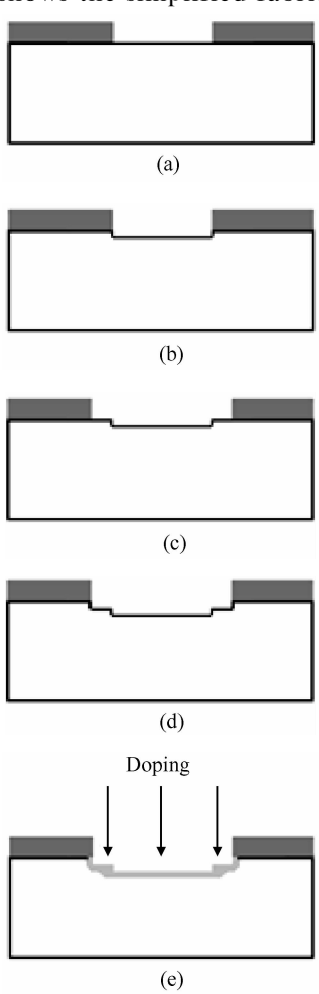

Fig. 7 Multi-cascade structure fabrication procedure

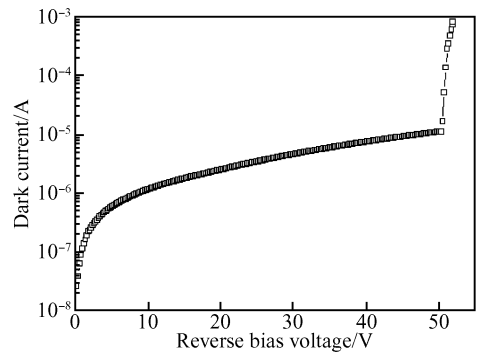

Fig. 8 Dark current at room temperature of the typical 3-cascade structure APDs with the junction depth of 2.5μm

The dark current of the typical 3-cascade structure APDs at room temperature is shown in Fig. 8. These devices all have a junction depth of 2.5μm and show very uniform breakdown characteristics. If the criterion of the dark current level for breakdown is set to be 10^{-3}A, the devices show breakdown voltages of 53V approximately, quite close to the predicted value of 54.3V in Fig. 3. This result also justifies the fact that uniform central breakdown occurs at the breakdown voltage in the cascade structure APD, and premature edge breakdown is suppressed. Better results are expected in the APDs with more cascade steps.

5 Conclusion

A novel planar InGaAs/InP avalanche photodiodes structure is presented and simulated. The central junction depth is carefully chosen to reduce the breakdown voltage, while the electric field at the hetero-interface falls in the ideal range between 80 and 200kV/cm. Furthermore, a cascade junction structure is proposed at the edge of the central junction to maintain a uniform breakdown voltage across the active area. The cascade junction structure outperforms the conventional floating guard ring structures in controlling

the edge electric field distribution. In future development, it is worthwhile to research combining the conventional floating guard ring with the multi-cascade structure. Better results in terms of edge breakdown suppression are predicted but have yet to be verified. Combining all the above considerations, it is guaranteed that Geiger mode APDs for the detection of infrared single photons can be developed using a planar fabrication process and characterized with high detection efficiency and low edge breakdown probability.

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具有抑制边缘击穿的层叠结结构的平面型 InGaAs/InP 盖革雪崩光电二极管的设计

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摘要： 通过有限元分析设计了具有抑制边缘击穿的层叠边缘结结构的平面型 InGaAs/InP 盖革雪崩光电二极管. 通过仔细地控制中央区域结的深度，光电二极管的击穿电压降至 54.3V；同时通过调整 InP 倍增层的掺杂浓度和厚度，沿器件中轴的电场分布也得到了控制. 在有源区的边缘采用层叠 pn 结结构有效地抑制了过早边缘击穿现象. 仿真模拟显示四层层叠结构是边缘击穿抑制效果和制造工艺复杂度的一个好的折衷方案，该结构中峰值电场强度为 5.2×10^5 kV/cm，空穴离化积分最大值为 1.201. 本文提供了一种设计高性能的 InGaAs/InP 光子计数雪崩光电二极管的有效方法.

关键词： 盖革 APD；边缘击穿；层叠结；击穿电压

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