# Layout and process hot carrier optimization of HV-nLEDMOS transistor*

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**Abstract:** Two layout and process key parameters for improving high voltage nLEDMOS (n-type lateral extended drain MOS) transistor hot carrier performance have been identified. Increasing the space between Hv-pwell and n-drift region and reducing the n-drift implant dose can dramatically reduce the device hot carrier degradations, for the maximum impact ionization rate near the Bird Beak decreases or its location moves away from the $Si/SiO_2$ interface. This conclusion has been analyzed in detail by using the MEDICI simulator and it is also confirmed by the test results.

**Key words:** nLEDMOS; hot carrier degradation; layout; process
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## 1. Introduction

For many smart-power applications, such as PDP drivers[1, 2], lateral DMOS transistors are the devices of choice as they are compatible with the standard CMOS process and can be easily integrated[3, 4]. A severe drawback, however, is that the current is flowing close to the $Si/SiO_2$ interface and because of the large drain voltages applied (above 100 V) the devices are vulnerable to hot carrier injection and trapping. The hot carrier degradation mechanism of 12–40 V nLDMOS[3−7] has been well investigated. However, the hot carrier improved method of the nLEDMOS, whose breakdown voltage is above 100 V especially, is less documented.

In this paper, several layout and process key parameters for improving 100 V nLEDMOS transistor hot carrier performance have been identified. The space between Hv-pwell and n-drift region and their doping concentration can significantly impact device HC (hot carrier) performance and need to be optimized. Increasing the space between Hv-pwell and n-drift region and reducing the n-drift implant dose can dramatically reduce the device hot carrier degradations, for the maximum impact ionization rate near the Bird's Beak decreases or its location moves away from the $Si/SiO_2$ interface. However, the former method will affect the turn-on voltage stability, while the latter method will affect the device electric safe operation area. The relationship between these parameters and device HC performance has been investigated by using the MEDICI simulator, which well supports the experimental findings.

## 2. Device structure

The devices investigated in this paper are high voltage nLEDMOS compatible with bulk-silicon standard CMOS processing, shown in Fig. 1. The n-drift and channel length of the nLEDMOS are about 7 and 4 $\mu$m, respectively. The threshold voltage and the maximal turn-off breakdown voltage of the nLEDMOS are 1.5 and 120 V, respectively. The most important layout parameters (i.e., the space between Hv-pwell and n-drift $A$, the channel length $B$) are also indicated in Fig. 1. Since the channel length correlates with the device $I_{on}$ requirement strongly, the channel length $B$ of all the devices investigated in this paper is 4 $\mu$m constantly. The detailed structure and technology parameters can be seen in Table 1.

## 3. Measurement and discussion

It was identified that one-dimensional device layout parameter $A$ and the n-drift implant dose can strongly impact HV-nLDMOS HC performance. Figure 2(a) displays the measured specific on-resistor ($R_{on}$) degradation as a function of the stress time versus Hv-pwell to n-drift space $A$, showing that as $A$ increases $R_{on}$ degradation can be greatly reduced. Figure 2(b) shows that as the n-drift implant dose changed from

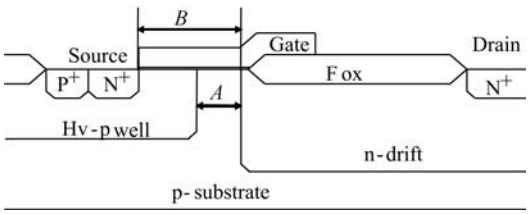


Fig. 1. Cross section (not to scale) of the nLEDMOS showing the main geometrical parameters of the device.

Table 1. Detailed structure and technology parameters of the proposed device.

| Item | Value | Unit |
|---|---|---|
| Hv-pwell boron implant dose | $3.5\times10^{13}$ | atom/cm$^2$ |
| p-sub doping concentration | $7\times10^{14}$ | atom/cm$^3$ |
| n-drift phosphor implant dose | $4.1\times10^{12}$ | atom/cm$^2$ |
| Vt adjustment implant dose ($BF_2$) | $0.9\times10^{12}$ | atom/cm$^2$ |
| Gate oxide thickness | 200 | Å |
| Field oxide thickness | 4400 | Å |
| Poly thickness | 0.55 | $\mu$m |
| Aluminum thickness | 0.8 | $\mu$m |

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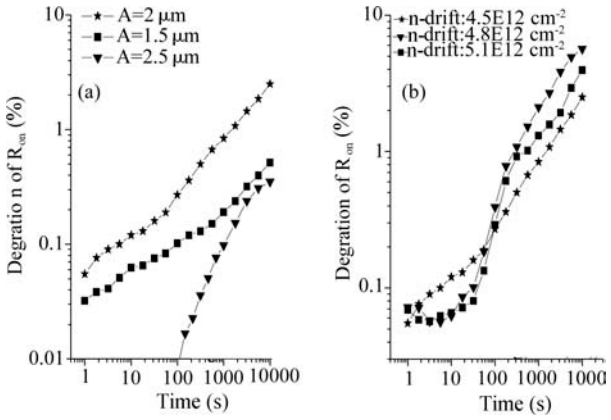


Fig. 2. Measured $R_{on}$ degradation as a function of the stress time versus Hv-pwell to (a) n-drift spacing $A$ and (b) n-drift implant dose. Measured at $V_{gs}$ = 3 V,$V_{ds}$ = 90 V.

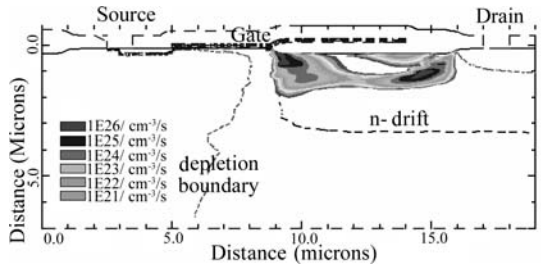


Fig. 3. Simulated nLEDMOS impact ionization rate at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V.

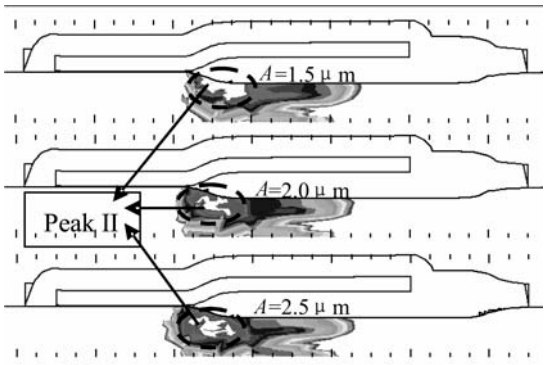


Fig. 4. Simulations demonstrate that as the parameter $A$ increases, the maximum impact ionization rate point location gradually moves away from Si/$SiO_2$ interface around the BB region at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V.

$5.1 \times 10^{12}$ to $4.5 \times 10^{12}$ cm$^{-2}$, $R_{on}$ degradation is also reduced after a stress time of about 100 s. The n-drift implant dose and the parameter $A$ of the devices under investigation in Figs. 2(a) and 2(b) are $4.5 \times 10^{12}$ cm$^{-2}$ and 2 $\mu$m, respectively.

To understand Figs. 2(a) and 2(b), detailed 2-D TCAD simulations are performed to gain insight into the physical mechanisms ruling the device degradation. Figure 3 clearly shows there are two peak impact ionization rate points along the flow lines under a typical operation condition. One point is near the BB (bird's beak) region and the other near the drain, both of which generate a mass of hot carriers. The obvious difference between the two points is that the first one is very close to the Si/$SiO_2$ interface, which means the impact ionization rate and the location of this point dominate the device degradation magnitude.

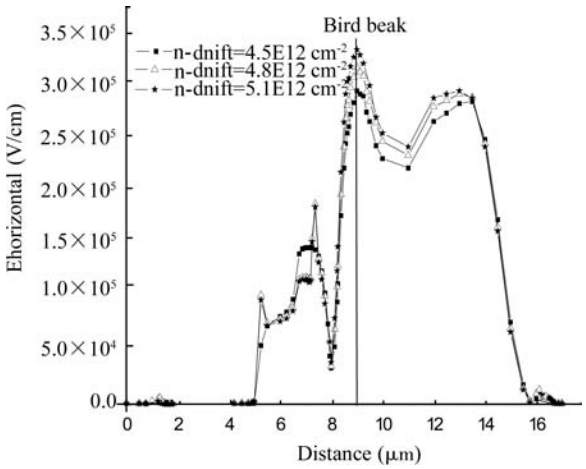


Fig. 5. Simulations demonstrate that as the n-drift implant dose decreases from $5.1 \times 10^{12}$ to $4.5 \times 10^{12}$ cm$^{-2}$, the magnitude of the peak electric field close to the BB region decreases too at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V.

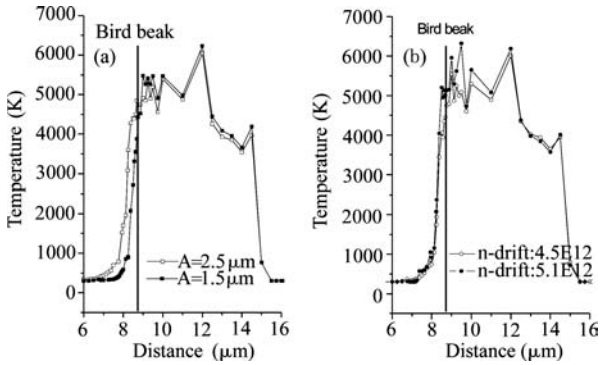


Fig. 6. Electron temperature along the Si/$SiO_2$ interface of the nLEDMOS at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V versus (a) parameter $A$ and (b) n-drift dose.

Figure 4 shows the relationships between the maximum II rate point location and the device parameter $A$ near the BB region at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V. The simulations demonstrate that as the parameter $A$ increases from 1.5 to 2.5 $\mu$m, the maximum impact ionization rate point location gradually moves away from Si/$SiO_2$ interface, reducing the amount of the $D_{it}$ formation and hot carriers injection near the BB region[5–8].

Figure 5 shows the magnitude of the horizontal electric field along the Si/$SiO_2$ interface at $V_{gs}$ = 3 V, $V_{ds}$ = 100 V. As can be seen from Fig. 5, when the n-drift implant dose decreases, the magnitude of the peak electric field close to the BB region also decreases rapidly. As the impact ionization rate of this region decreases, the device degradation is reduced.

It can be seen clearly from Figs. 6(a) and 6(b) that as the parameter $A$ increases or the n-drift implant dose decreases, the electron temperature along the Si/$SiO_2$ interface of the nLEDMOS decreases close to 1000 K near the BB region. A similar conclusion can also been drawn for the hole temperature along the Si/$SiO_2$ interface.

Figures 7(a) and 7(b) show the probability per unit length that a carrier is injected into the oxide along Si/$SiO_2$ interface at $V_{gs}$ = 3.3 V, $V_{ds}$ = 100 V versus n-drift implant dose and parameter $A$, respectively. The simulation results indicate that as the n-drift implant dose decreases and the $A$

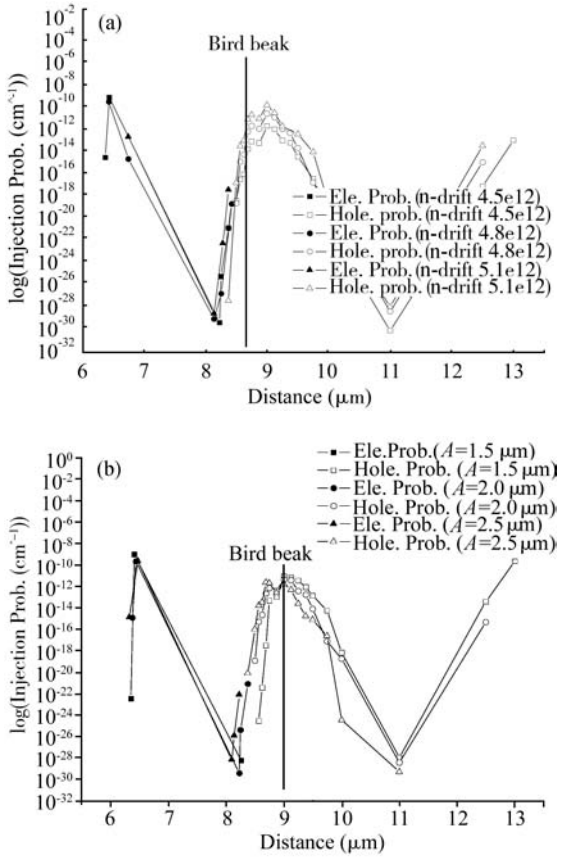


Fig. 7. Probability per unit length that a carrier is injected into the oxide along $Si/SiO_2$ interface at $V_{gs}$ = 3.3 V, $V_{ds}$ = 100 V versus (a) n-drift implant dose and (b) parameter $A$.

increases the probability per unit length that a carrier is injected into the oxide along $Si/SiO_2$ interface decreases, which agrees well with the experiment results.

Because of the photolithgraphy alignment error, the device turn-on voltage relative drift gradually rises as the parameter $A$ decreases. And due to the Kirk effect[9], reducing the n-drift implant dose causes the nLEDMOS safe operating area (SOA) to shrink under typical gate bias condition ($V_{gs}$ = 5 V). Thus these two layout and process key parameters need to be compromised alongside the device turn-on voltage stability, E-SOA (electric safe operating area) and HC-SOA (hot carrier safe operating area).

## 4. Conclusion

In this paper, the layout and process optimization for hot carrier of nLEDMOS transistor have been experimentally investigated. Increasing the space between Hv-pwell and n-drift region and reducing the n-drift implant dose can dramatically reduce the device hot carrier degradations, for the maximum impact ionization rate decreases or its location moves away from the $Si/SiO_2$ interface. This conclusion has been analyzed by using the MEDICI simulator and it is also confirmed by the testing results. The fab productivity of PDP data driver IC chip with the proposed device is 90%，which is a satisfactory result considering its large edge loss due to the big chip size (8 × 1.4 mm$^2$). Because the former method may affect the turn-on voltage stability, while the latter method may affect device electric SOA area, due to the photolithgraphy alignment error and Kirk effect, respectively, these two parameters need to be compromised to some extent for a high reliability device.

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