Simulation and Experiment on a Buried-Oxide Trench-Gate Bipolar-Mode JFET*

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Abstract: A buried-oxide trench-gate bipolar-mode JFET (BTB-JFET) with an oxide layer buried under the gate region to reduce the gate-drain capacitance C_{gd} is proposed. Simulations with a resistive load circuit for power loss comparison at high frequency application are performed with 20V-rated power switching devices, including a BTB-JFET, a trench MOSFET (T-MOSFET) generally applied in present industry, and a conventional trench-gate bipolar-mode JFET (TB-JFET) without buried oxide, for the first time. The simulation results indicate that the switching power loss of the normally-on BTB-JFET is improved by 37% and 14% at 1MHz compared to the T-MOSFET and the normally-on TB-JFET, respectively. In order to demonstrate the validity of the simulation, the normally-on TB-JFET and BTB-JFET have been fabricated successfully for the first time, where the buried oxide structure is realized by thermal oxidation. The experimental results show that the C_{gd} of the BTB-JFET is decreased by 45% from that of the TB-JFET at zero source-drain bias. Compared to the TB-JFET, the switching time and switching power loss of the BTB-JFET decrease approximately by 7.4% and 11% at 1MHz, respectively. Therefore, the normally-on BTB-JFET could be pointing to a new direction for the R&D of low voltage and high frequency switching devices.

Key words: TB-JFET; BTB-JFET; buried oxide; gate-drain capacitance; switching power loss
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1 Introduction

Nowadays, DC/DC Buck converters are used in power management for CPUs, chipsets, peripherals, etc, and are one of the most important applications for low-voltage high-current power switching devices to be researched and developed. Low-voltage power transistors, especially used as control transistors (high side transistors), have been developed recently to meet the high frequency (reaching 1MHz and above) and low switching power loss requirements. While presently power MOSFETs dominate in this area, their dimensions have been scaled to a submicron level and their fabrication processes have become more and more complicated and seem to be approaching the technological limits. Therefore, globally, some attempts continue to resort to trench-gate bipolar-mode power JFETs (TB-JFETs)[1~3].

In this paper, a buried-oxide trench-gate bipolar-mode JFET (BTB-JFET) with an oxide layer buried under the gate region to reduce the gate-drain capacitance C_{gd} is proposed. To evaluate the prospects of this kind of device, simulations for power loss comparison are performed with a BTB-JFET, a trench MOSFET (T-MOSFET) generally applied in present industry, and a conventional TB-JFET without buried oxide[1] for the first time. Furthermore, the normally-on TB-JFET and BTB-JFET have been successfully fabricated for the first time, and the experimental results agree well with the simulation.

2 Structures for simulations

The three structures mentioned above are shown in Fig. 1, which are half cells for simulations. Three devices are vertical, ensuring their application in high current field as power devices. The first two are typical models of state-of-the-art structures with $BV_{ds} \geqslant 20V$ for a T-MOSFET (Fig. 1(a)) and a conventional TB-JFET (Fig. 1(b)), respectively. A BTB-JFET (Fig. 1(c)) is almost identical to the second except for a buried oxide (BOX) layer under the gate region or bottom of the trench, which can be achieved through thermal oxidation[2,4] or deposition[5]. The structure and dimensions of the T-MOSFET are set according to Ref. [6], and simulation results show that the structure with a thick gate oxide at the bottom shown in Fig. 1(a) has a switching power loss reduction by 30% over that in Ref. [6] without changing $R_{DS(on)}$, which ensures the former has the better performance. Key parameters used in the simulations

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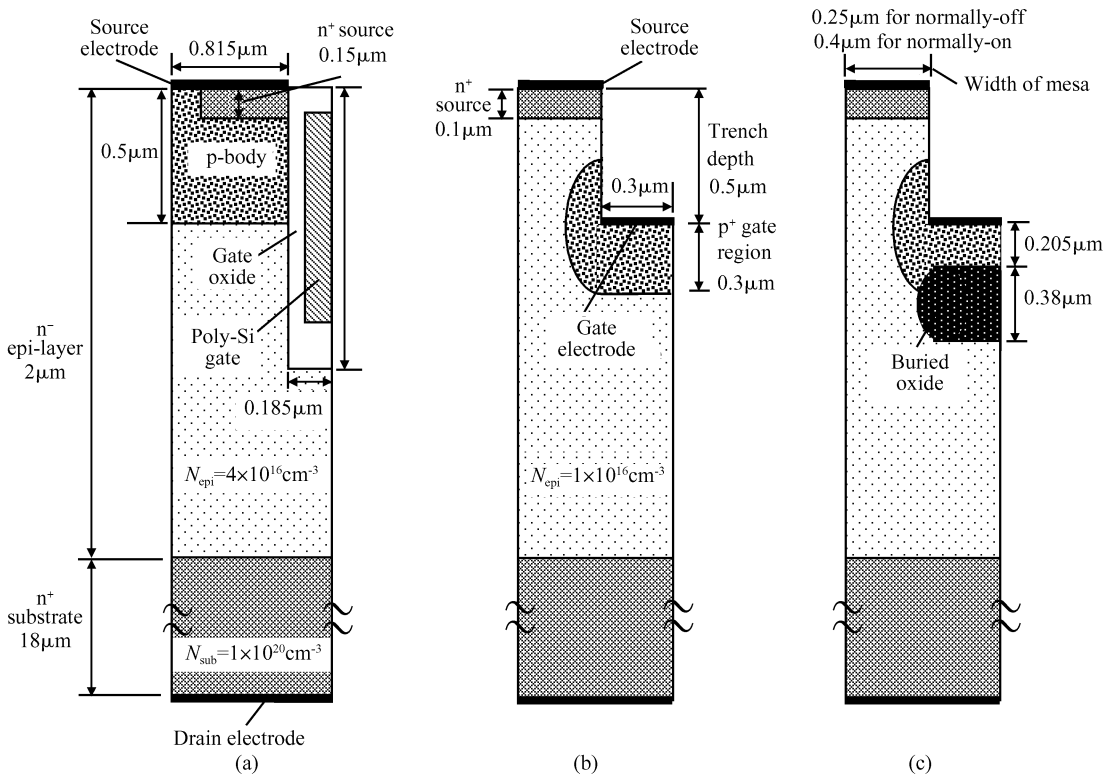

Fig. 1　Schematic structures for simulations　(a) T-MOSFET; (b) TB-JFET; (c) BTB-JFET

are labeled in the figure and omitted when they are identical to those already given on the left. The critical dimensions of all the structures are in submicron.

The MOSFET is a normally-off device. However, the JFET can be either normally-off or normally-on depending on the width of mesa, i.e., whether depletion layers of P-gates overlap at zero gate-source bias. Gate capacitance, especially C_{gd}, is a key parameter in high speed switching applications. In the structure of the BTB-JFET, a large area of pn junction under the gate region is replaced by buried oxide, reducing C_{gd} remarkably and improving the switching performance of the device.

3　Simulation results

For the purpose of estimation, power loss simulations are performed on a basic resistive switching circuit, with V_{DD} = 12V, $I_{D(on)} \approx$16A (through a chip area of 3mm^2), R_G = 2Ω, and V_G pulse set to 0/10V for the T-MOSFET, the normally-off JFETs or set to −8/+2V (−8V offset from the former) for the normally-on JFETs. Figure 2 gives the typical switching waveforms for these devices. The waveforms of v_{GS} and i_G for the TB-JFET (those for the BTB-JFET are quite similar) are remarkably different from those for the T-MOSFET.

Switching power loss $P_{sw} = P_{on} + P_{off}$, where relevant energies are integrated from the onset of V_G pulse to the instant when i_D rises to 90% of $I_{D(on)}$ (to produce E_{on}) and from the ending of V_G pulse to the instant when i_D falls to 10% of $I_{D(on)}$ (to produce E_{off}). Since the P_{sw} is dependent on the working frequency, to calculate the power loss the relative energies are multiplied by the frequency.

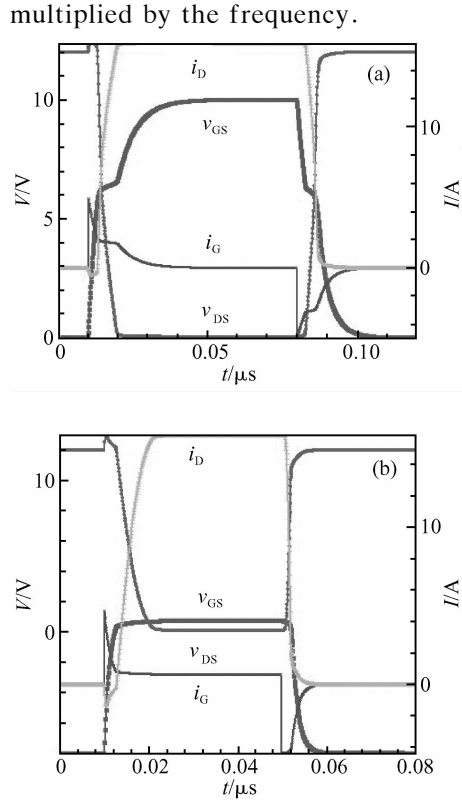

Fig. 2　Typical switching waveforms for T-MOSFET (a) and TB-JFET (same as BTB-JFET) (b)

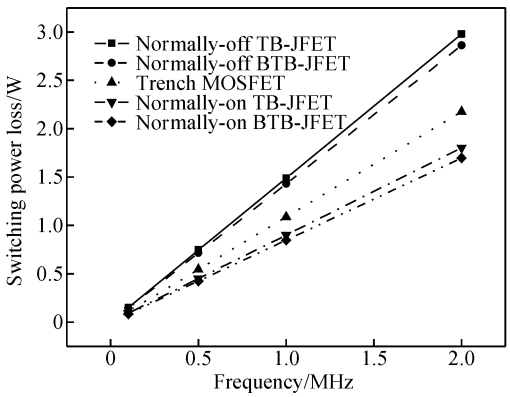

Fig. 3 Comparison for switching power losses of different devices at various frequencies

Figure 3 shows the final calculation results of switching power losses varying with frequency for the three devices. This figure shows that under the circuit condition mentioned above, the normally-on BTB-JFET produces the lowest switching power loss at different frequencies of the five devices, and the improvement is up to 37% and 14% at 1MHz compared to the T-MOSFET and the normally-on TB-JFET, respectively. The trend in the figure implies that the normally-on TB-JFET and normally-on BTB-JFET will be superior to the T-MOSFET at high frequencies and the normally-on BTB-JFET is the most competitive candidates to replace power MOSFETs as the high side power transistor, the switching performance of which is much more emphasized in low-voltage DC/DC Buck converters. On the other hand, the normally-off JFETs always perform worse than the T-MOSFET at different frequencies[7].

4 Experimental results

In order to validate the above simulation results, the normally-on BTB-JFET has been successfully fabricated for the first time, and its buried oxide is realized by thermal oxidation. At the same time, for comparing the performance of the BTB-JFET with the TB-JFET, sample transistors of the normally-on TB-JFET with the same physical structure and dimensions but without the buried oxide has also been fabricated and measured. These two kinds of normally-on JFETs show similar breakdown voltage and current level with BV_{ds} = 21V at V_{GS} = −3V, and both of them have a threshold voltage of about 0.7V. Their R_{dson} are 100mΩ (TB-JFET) and 112mΩ (BTB-JFET), respectively, with 0.25mm^2 of active area.

The measured C_{gd}-V_{DS} curves of the fabricated TB-JFET and BTB-JFET at V_{GS} = −3V are shown in Fig. 4. The gate-drain capacitance C_{gd} of the BTB-JFET is reduced by 45% at zero source-drain bias over

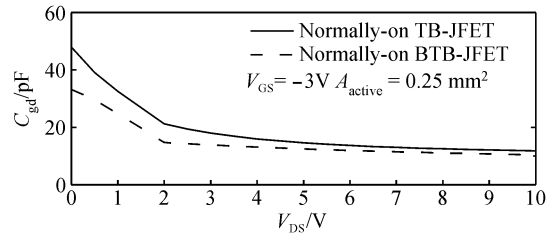

Fig. 4 Experimental plots of C_{gd} versus V_{DS} for normally-on TB-JFET and BTB-JFET

that of the conventional TB-JFET.

The lower C_{gd} reduces the switching time and the power loss of the device during the switching state. The switching parameters of the fabricated TB-JFET and BTB-JFET devices are also tested with a clamped resistive load circuit the same as that used in simulation and under the same measurement conditions. Table 1 gives the measurement conditions and results, where the turn-on time is defined as the time between the events when V_G rises to 10% of the final value (different from the simulation due to the ramping delay of the input pulse) and i_D rises to 90% of the $I_{D(on)}$ value (the same as that in simulation). The turn-off time is defined as the time between when V_G falls to 90% of the initial value and i_D falls to 10% of the $I_{D(on)}$ value. Under the above conditions, the turn-on times of TB-JFET and BTB-JFET are measured as approximately 12.3 and 11.8ns, and the turn-off times are approximately 13.9 and 12.5ns, respectively. These results in switching power losses are approximately 3.205 and 2.858mW for both JFETs at 1MHz, respectively. Compared to the TB-JFET, the switching time and switching power loss of the BTB-JFET are decreased by approximately 7.4% and 11%, respectively. These results agree well with those given by the simulation.

5 Conclusion

A BTB-JFET with an oxide layer buried under the gate region to reduce the gate-drain capacitance C_{gd} is proposed. A power loss comparison of 20V-rated power switching devices, including a BTB-

Table 1 Switching time and power losses of TB-JFET and BTB-JFET

V_{DD} = 10V, V_G = −8～+2V, active area = 0.25mm^2, frequency = 1MHz

Device	Switching state	Switching time /ns	Switching power loss/mW
TB-JFET	Turn-on	12.3	3.205
	Turn-off	13.9	
BTB-JFET	Turn-on	11.8	2.858
	Turn-off	12.5	

JFET, a T-MOSFET, and a conventional TB-JFET, is made by means of simulation with a resistive switching circuit. Simulation results show a great significance and indicate that the normally-on BTB-JFET produces the lowest switching power loss of the five kinds of devices at high frequency applications and its improvement is remarkable. On the other hand, the normally-on TB-JFET and BTB-JFET sample transistors are successfully fabricated. Measurement results show that the normally-on BTB-JFET has a greatly reduced C_{gd} and improved switching power losses over the TB-JFET, which agrees with the simulation results. Thus, we conclude that simulation and experiment have verified the feasibility of the normally-on BTB-JFET as a competitive candidate to replace power MOSFET as the high side power transistor for high frequency and low-power-loss DC/DC converter applications in the coming high frequency era. The normally-on BTB-JFET could be pointing to a new direction for low voltage high frequency switching device research.

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埋氧沟槽栅双极模式 JFET 的仿真与实验*

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摘要：提出了埋氧沟槽栅双极模式 JFET(BTB-JFET)，其在栅极区域下面添加埋氧以减小栅漏电容 C_{gd}. 首次通过仿真对包括 BTB-JFET、常规的无埋氧层的沟槽栅双极模式 JFET(TB-JFET)和现在正在广泛应用的 Trench-MOSFET(T-MOSFET)等 20V 级的功率开关器件在高频应用时的功率损耗进行了比较，得到有重要意义的结论. 采用阻性负载电路. 仿真结果表明，与 T-MOSFET 和常开型 TB-JFET 相比，常开型 BTB-JFET 在 1MHz 时开关功耗分别降低了 37% 和 14%. 进行实验以证明仿真工作的合理性，首次成功地制造出常开型 BTB-JFET 和 TB-JFET，其中埋氧结构是通过热氧化的方法实现的. 实验结果表明，与 TB-JFET 相比，在源漏零偏压时，BTB-JFET 的 C_{gd} 减小了 45%；在 1MHz 时，其开关时间与开关功耗分别降低了约 7.4% 和 11%. 因此常开型 BTB-JFET 应是今后低压高频功率开关器件的研究发展方向.

关键词：沟槽栅双极模式 JFET；埋氧沟槽栅双极模式 JFET；埋氧；栅漏电容；开关功率损耗

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