# Growth of High-Quality InP-on-GaAs Quasi-Substrates Using Double Low-Temperature Buffers and Strained Layer Surperlattices by MOCVD\*

Zhou Jing<sup>†</sup>, Ren Xiaomin, Huang Yongqing, and Wang Qi

(Key Laboratory of Optical Communication & Lightwave Technologies, Ministry of Education, Beijing University of Posts and Telecommunications, Beijing 100876, China)

Abstract: We investigate the growth of InP-on-GaAs combined with the advantages of double low-temperature (LT) buffers and strained layer surperlattices (SLSs). It is found that LT-InP/LT-GaAs double LT buffers are more effective for strain accommodation than a LT-InP single buffer in InP-on-GaAs. On the other hand, there is an optimal thickness for LT-GaAs for a given thickness of the LT-InP layer, at which the double LT buffers can reach the best state for strain adjustment. Furthermore, the position of insertion of SLSs should be carefully designed because the distance above the InP/ buffer interface plays an important role in threading dislocation interactions for dislocation reduction. As a result, the density of threading dislocations in the InP epilayer is markedly reduced. X-ray diffraction measurements show that the full width at half maximum of the  $\omega/2\theta$  rocking curve for the  $2\mu$ m-thick InP epilayer is less than 200<sup>°</sup>.

Key words:InP-on-GaAs;double low-temperature buffers;InGaP/InP SLSs;MOCVDEEACC:0520CLC number:O782Document code:AArticle ID:0253-4177(2008)10-1855-05

### **1** Introduction

High-quality relaxed InP layers grown on GaAs substrates, which are used as "quasi-substrates" for the growth of InP-related optical devices with GaAs electronic devices on a GaAs substrate to realize high-performance optoelectronic integrated circuits (OEICs), have attracted considerable attention<sup>[1~3]</sup>. However, the success of such a monolithic integration depends on if the material problems, such as high defect density and large misfit strain, can be understood and solved. So far, many studies have been carried out to solve the problems<sup>[4,5]</sup>, but from the view of practical interest, most methods used to reduce the number of the defects are too complicated to be widely used in device fabrication.

The overall quality of the heteroepitaxial layer is controlled by the initial layer deposited at low temperature (under  $450^{\circ}$ C); thus, the low-temperature buffer corresponding to the initial growth layer should be carefully studied and designed in order to gain a better quality heteroepitaxial layer. Moreover, among various growth techniques designed to reduce threading dislocations (with strained interlayer, thermal cycling, and patterned growth), inserting InGaP/ InP SLSs into the InP epilayer as defect filtering layers has shown such possibilities<sup>[6]</sup>. However, only a few studies of InGaP/InP SLSs designed for InP-on-GaAs have been reported.

In this study, the effect of LT-InP/LT-GaAs double buffers on InP-on-GaAs is first examined. Simultaneously, we compare the X-ray diffraction profiles of the two samples grown with two types of buffer layers: a LT-InP single buffer and LT-InP/LT-GaAs double buffers, which induce research interest in the mechanism responsible for the defect reduction. Next, 15-period  $In_{1-x} Ga_x P/InP$  ( $x \approx 0.12$ ) SLSs as defect filtering layers in InP-on-GaAs were optimized by varying their insertion positions while fixing the total thickness of the InP epilayer. The quality and the characteristic of grown structures are assessed by double-crystal X-ray diffraction and cross-sectional transmission electron microscopy.

### 2 Experiment

All the samples were grown in a  $3 \times 50$ mm CCS low pressure MOCVD system with the fixed reactor pressure of 100Torr and the total flow rate of 12000 sccm. Pure arsine (AsH<sub>3</sub>), phosphine (PH<sub>3</sub>), trimethylindium (TMIn) and trimethylgallium (TMGa) were used as precursor materials. Pd-cell purified hydrogen (H<sub>2</sub>) served as the carrier gas. After loading into the

<sup>\*</sup> Project supported by the State Key Program for Basic Research of China (No. 2003CB314901), the National High Technology Research and Development Program of China (No. 2007AA03Z418), and the 111 Project (No. B07005)

<sup>†</sup> Corresponding author. Email: zhoujing@bupt.edu.cn

Received 24 April 2008, revised manuscript received 22 May 2008



Fig. 1 Schematic of the epitaxial structures (a) With a single LT-InP buffer layer; (b) With LT-InP/LT-GaAs double buffers; (c) Insertion of 15-period (4nm/6nm)  $In_{1-x}Ga_x P/InP$  ( $x \approx 0.12$ ) SLSs based on (b) The insertion position of SLSs was denoted by h. All the LT buffer layers were grown at 450°C and the remnant layers were grown at 685°C.

growth reactor, all the GaAs (100) substrates were first deposited with a 50nm-thick GaAs layer at 685°C to ensure a smooth surface for the following layer growth.

The structures of the samples are schematically shown in Fig. 1: (a) a conventional two-step growth structure with a single LT-InP buffer; (b) a LT-InP layer together with a thin LT-GaAs layer as double LT buffers; and (c) 15-period (4nm/6nm) In<sub>1-x</sub>- $Ga_x P/InP$  ( $x \approx 0.12$ ) SLSs introduced as an intermediate layer for further improving the quality of the top InP layer. The thickness h of the first InP layer indicating the insertion position of SLSs will be discussed in next section. In all cases, InGaP/InP SLSs were grown at 685°C, which were kept the same as that of the InP epilayer in order to remove the influence of switching temperature on the material properties. The growth temperatures of both LT-InP and LT-GaAs were 450°C. The thickness of LT-InP, if not specifically noted, was 15nm. The V/III ratios were 165,270, and 185 for the LT-InP, LT-GaAs, and InP epilayer, respectively.

Following growth, the quality and the characteristic of grown structures were assessed by doublecrystal X-ray diffraction (DCXRD). The improvement of the crystal quality or degradation of the InP layer was measured by the decrease or increase in the full width at half-maximum (FWHM) of X-ray diffraction peaks. The distribution and threading behaviors of dislocations were studied by cross-sectional transmission electron microscopy (TEM) with a JE-OL 2000FX instrument operating at 200keV.

### **3** Results and discussion

#### 3.1 Effect of the double LT buffers

The samples were measured by DCXRD to confirm the crystal quality and residual strain with different buffer schemes, and the results are given in Table 1. From the symmetric (004) rocking curves, the FWHM of the epitaxial layer feature gives an indication of the material quality. To determine the residual strain in the InP epilayer, (004) and a set of (115) diffraction rocking curves with different incident angles were measured.

As shown in Table 1, the InP peak from sample B, with a 15nm/15nm LT-InP/GaAs double buffer, has the smallest FWHM of all the samples, indicating the lowest dislocation density. When further increasing the thickness of the LT-GaAs buffer, especially larger than 50nm, the FWHM is boarded obviously, suggesting that there exists an optimal thickness of the LT-GaAs buffer at which the crystal quality is the best. It was also found that the crystal quality of the samples grown by the double LT buffers (sample B) is much better than that grown by a single LT buffer (sample E) in spite of the same thickness of the total LT-buffer layer.

Table 1 also reports the experimental values of out-of-plane and in-plane lattice constants  $(a_{\perp}, a_{\parallel})$ . In addition, the residual strain  $(\epsilon_{\perp}, \epsilon_{\parallel})$  are also given. The lattice constant ratio  $a_{\perp}/a_{\parallel}$  is calculated by

$$\frac{a_{\perp}}{a_{\parallel}} = \left(\frac{h^2}{k^2 + l^2}\right)^{1/2} \tan\left(\arccos\frac{h}{\sqrt{h^2 + k^2 + l^2}} + \beta\right)$$
(1)

where  $\beta = \frac{1}{2} (\Delta \theta_+^{115} - \Delta \theta_-^{115})$ , and  $\Delta \theta_+^{115}$  and  $\Delta \theta_-^{115}$  are the angular separations between the InP and GaAs reflections from the (115) and (115) planes, respectively, and h = 1, k = 1, l = 5 the relevant reflection plane in-

Table 1 Structural parameters of InP-on-GaAs with LT-InP/ LT-GaAs double buffers  $t_1$  and  $t_2$  are the layer thickness of LT-InP and LT-GaAs, respectively.  $a_{\perp}(\varepsilon_{\perp})$  and  $a_{\parallel}(\varepsilon_{\parallel})$  are the experimental values of out-of-plane and in-plane lattice constants (residual strain) respectively, obtained from XRD symmetric (004) and asymmetric (115) measurements. (004)-FWHM of InP epilayer recorded using the  $\omega/2\theta$  mode, indicating the trends in crystal quality. All the samples had a  $2\mu$ m-thick InP epilayer and other growth conditions were kept the same.

No.	$(t_1/t_2)$	(004)-FWHM	$a_{\perp}$	<i>a</i>	ε_	€∥
	/(nm/nm)	/(~)	/nm	/nm	/ %	/ %
А	15/0	408	0.6012	0.5826	1.576	-1.398
В	15/15	370	0.5927	0.5892	0.3172	-0.2812
С	15/50	389	0.5885	0.5831	0.4851	-0.4310
D	15/80	430	0.5894	0.5780	1.034	-0.9169
Е	30/0	525	0.5877	0.5869	0.07219	-0.06402



Fig. 2 Rocking curves of XRD  $\omega/2\theta$  (004) scans of samples B (a) and E (b) In a, a shoulder tailing to the right of the InP epilayer peak, indicated by the arrow, was associated with a mechanical deformation behavior of LT-buffer.

dices. The in-plane and out-of-plane strains given by

$$\varepsilon_{\parallel} = \frac{a_{\parallel} - a_{\rm epi}}{a_{\rm epi}}, \quad \varepsilon_{\perp} = \frac{a_{\perp} - a_{\rm epi}}{a_{\rm epi}}$$
(2)

with the lattice constant of InP epilayer satisfying the relation of  $a_{epi} = a_{\#} + \frac{1-\nu}{1+\nu}(a_{\perp} - a_{\#})$ .  $\gamma$  is the Poisson's ratio and its value is 0.36 for InP.

Table 1 also shows that there is large difference between values of  $a_{\perp}$  and  $a_{\parallel}$ . On one hand, this difference is caused by the difference in the thermal expansion coefficients between InP and GaAs. On the other hand, the dislocations at the interface and the stacking faults of the samples affect the measured value of  $a_{//}$ , so  $a_{//} = a_{substrate}$  is not true in the partially relaxed structure. We also found that the variation in residual strain is correlated with adding the LT-GaAs layer between the LT-InP layer and the substrate. The strain energy in sample A is larger than other samples grown with LT double buffers (samples B,C,D), as a similar trend in FWHM. Sample E, with a 30nm-thick LT-InP, has the smallest strain energy of all the samples, but has the largest FWHM ( $\approx 525^{\circ}$ ), indicating that strain relaxing is at the cost of the crystal quality. Thus the mechanism of strain relaxation is an important factor in explaining the behavior of LT-InP/ LT-GaAs double buffers.

In order to further understand the behavior of double LT buffers, Figure 2 plots the rocking curves of XRD for samples B and E, corresponding to curves a and b, respectively. In curve b, the presence of a single, symmetric peak indicates that the InP epilayer and the buffer layer had indistinguishable interplanar

distance for the (004) lattice plane; while in curve a, an obvious shoulder tailing to the right of the InP epilayer peak, indicated by the arrow, is assumed to be associated with a mechanical deformation behavior of double LT buffers. This indicates that a thin LT buffer layer can significantly reduce the dislocation density in heteroepitaxy because the imperfect crystalline of the thin buffer/substrate interface behaves mechanically in a manner similar to that of compliant substrates for strain accommodation<sup>[7]</sup>. In this case, it can be understood as follows: (1) the presence of the shoulder indicates the out-of-plane lattice constant of the double-LT-buffer is smaller than that of the InP epilayer, therefore the double-LT-buffer is tensily strained; (2) the tensile strain of the double-LT-buffer partially compensates the compressive strain in the InP epilayer as a result of reducing the mismatch between the epilayer and the double-LT-buffer and substrate. This mechanism is similar to that of compliant substrate sharing the mismatch strain during heteroepitaxy.

Furthermore, Zhang *et al*.<sup>[8]</sup> proposed that the multi-buffer layers would be more effective in strain accommodation than single a buffer layer due to the presence of the muti-interface. Since the strain accommodation process lasted to the end of the growth, it would be triggered by the muti-interface more than once. Therefore, a possible conclusion is that a double-LT-buffer was more "compliant" for strain accommodation than a single one, which contributes to improving the quality of the InP epilayer. However, the detailed mechanism for compliance is complex and our work on this issue is currently under investigation.

#### **3.2** Insertion of $In_{1-x}Ga_xP/$ InP SLSs

Dislocation reduction by the insertion of SLSs results from threading dislocations bending at the interfaces. This bending of threading dislocations is caused by the misfit strain mainly due to the different lattice constants<sup>[8]</sup>. Since dislocation reduction by the insertion of SLSs associated with the different lattice constants depends strongly on its different lattice constants, the Ga composition x is a major parameter in reducing threading dislocations.

The grown structure is schematically demonstrated in Fig. 1 (c). The strain of SLS is defined as:  $f = (a_{InP} - a_{SLS})/a_{InP}$ , where  $a_{InP}$  is the lattice constant of InP without strain and  $a_{SLS}$  is the equivalent lattice constant of  $In_{1-x}Ga_xP$ . In this case, an increase in Ga composition x corresponds to an increased tensile strain f. In particular, for each composition x, there exists a corresponding critical layer thickness of SLS for formation of misfit dislocations. But the required



Fig. 3 Cross-sectional TEM images of the samples without (a) and with (b) InGaP/InP SLSs The numbers 1 and 2 denote two threading dislocations for interactions.

thickness of the SLS to filter dislocations has not been fully optimized because the reduction of dislocations may be due to the interactions between threading dislocations and misfit dislocations. In this experiment, for x = 0.12 ( $f \sim 0.85\%$ ) SLS, the thicknesses were 6 and 4nm for InP and InGaP, respectively, which were within the range of the critical thickness reported in Ref. [9].

Figure 3 shows the cross-section TEM images of two samples without (a), and with (b) SLSs. In Fig. 3 (a), a high density of misfit dislocations ( $\sim 10^6 \text{ cm}^{-1}$ ) is found at the bottom interface, and some of them thread the epilayer toward the free surface. The observed droplets are presumably due to incomplete PH<sub>3</sub> pyrolysis giving too little P at the solid/vapor interface during growth. In Fig. 3(b), there is almost no dislocation threading from the first InP layer to the second InP epilayer and some bent dislocations being driven along the InP/SLSs interface. In particular, two dislocations, denoted as 1 and 2, started at the bottom interface and propagated toward the upper layer till the annihilation reactions occurred. This ob-



Fig. 4 XRD-FWHM of InP peak of samples with InGaP/InP SLSs as a function of the insertion distance h For the detailed growth conditions of the SLSs, refer to Fig. 1(c).

servation indicates a possible way for dislocation reduction: the separated threading dislocations were driven close by the force as a result of the strain accumulated in the SLSs and coalesced or annihilated in the end. The TEM observations in Fig. 3 confirm that a further reduction of threading dislocations can be achieved by insertion of InGaP/InP SLSs

Figure 4 shows the XRD-FWHM of the InP peak of samples with SLSs as a function of the first InP layer thickness h. The minimum value of FWHM 203" is obtained in the sample with SLSs inserted at h =0.  $5\mu$ m. In the samples with h greater than 0.  $5\mu$ m, the FWHM increases as h increases. Since the total thickness of the InP epilayer was fixed as  $2\mu m$ , the increase of the FWHM was caused not by the deterioration of the dislocation reduction ability of the SLSs, but by the smaller thickness and larger strain of the upper InP layer. In contrast, the FWHM in the sample with SLSs inserted close to bottom interface, e. g. h = $0.05\mu m$ , was comparable with the sample without SLSs. Combined with the analysis of Fig. 3(b), we can assume that if h is less than the required length for threading dislocation interactions, the possibility of dislocations directly threading through the SLSs becomes larger, which deteriorates the dislocation reduction ability of the SLSs. This result implies that the first InP layer is necessary to reduce the threading dislocations.

### 4 Conclusion

In this work, we reported the detailed optimization of properties of double LT buffers and InGaP/ InP SLSs for InP-on-GaAs taking into account the strain relaxation mechanism and defect reduction mechanism. LT-InP/LT-GaAs double buffers deposited on the substrate as the initial layers were first examined and compared with the conventional two-step method. We demonstrated that with a proper thickness of the LT-GaAs layer, the double LT buffers were more "compliant" for strain accommodation than a single LT buffer. Then, 15-period (4nm/6nm)  $In_xGa_{1-x}P/InP$  ( $x \approx 0.12$ ) SLSs were introduced as defect filtering layers before the growth of the final InP layer. We investigated the effects of the insertion position of the SLSs on the stress relaxation and the crystal quality of InP top layer using the dependence curve of FWHM-thickness. We think that, in our case, when the total thickness of the InP epilayer was fixed  $2\mu$ m, an effective insertion position is 0.5 $\mu$ m at least above the bottom interface, which is related to a possible way of dislocation interactions for dislocation reduction.

#### References

[1] Chen S, Liu B, Wang B, et al. GaAs-InP heteroepitaxy and GaAs-InP MESFET fabrication by MOVPE.J Cryst Growth, 1997, 170: 433

- [2] Liao C I, Yang K F, Lin C L, et al. Direct growth of high-quality InP layers on GaAs substrates at low temperature by metalorganic vapor phase epitaxy. Jpn J Appl Phys, 2003, 42:4913
- [3] Zhang Y, Whelan C S, Leoni R, et al. 40-Gbit/s OEIC on GaAs substrate through metamorphic buffer technology. IEEE Electron Device Lett, 2003, 52:24
- [4] Ardila A M, Martínez O, Sanz L F, et al. Study of defects in conformal GaAs/Si layers by optical techniques and photoetching. Mater Sci Eng B, 2002, 91, 70
- [5] Nishida T, Akasaka T, Yamauchi Y, et al. Step-free surface and interface by finite area metalorganic vapor phase epitaxy. J Cryst Growth, 1998, 195, 459
- [6] Lazzrini L, Nasi L, Norman C E, et al. Dislocations in medium to highly mismatched III-V epitaxial heterostructures. J Cryst Growth, 1993, 126, 133
- [7] Westwood D, Woolf D. Mechanical behavior of thin buffer layers in InAs/GaAs heteroepitaxy. J Appl Phys, 1993, 73, 1187
- [8] Zhang Z C, Chen Y H, Yang S Y, et al. Threading dislocation reduction in GaAs on Si with a single InGaAs intermediate layer. Semicond Sci Technol, 2003, 18, 955
- [9] Okuno Y, Kawano T. Study of threading dislocation reduction by strained interlayer in InP layers grown on GaAs substrates. J Cryst Growth, 1994, 145, 338

## 利用双低温缓冲层和插入应变超晶格技术制备高质量 InP-on-GaAs 复合衬底的 MOCVD 生长\*

周静†任晓敏 黄永清 王琦

(北京邮电大学光通信与光波技术教育部重点实验室,北京 100876)

**摘要:**提出一种结合双低温缓冲层和应变超晶格优势的高质量 InP-on-GaAs 复合衬底制备技术.研究发现 LT-InP/LT-GaAs 的双低 温缓冲层比单一低温 InP 缓冲层的聚集应变的效果更为显著.并且,双低温缓冲层中的低温 GaAs 层存在一个最优生长厚度.当低温 InP 生长厚度一定,低温 GaAs 层的生长厚度达到优化生长厚度时,LT-InP/LT-GaAs 双低温缓冲层能达到调节应变的最佳状态.最后,通过插入 InGaP/InP 应变超晶格,并且优化其在外延层中的插入位置,得到了高质量的 InP-on-GaAs 的复合衬底,2μm 厚的 InP 外延层 XRD- ω/2θ 扫描的半高宽小于 200″.

关键词: InP-on-GaAs;双低温缓冲层; InGaP/InP 应变超晶格; MOCVD
EEACC: 0520
中图分类号: O782
文献标识码: A
文章编号: 0253-4177(2008)10-1855-05

<sup>\*</sup>国家重点基础研究发展计划(批准号:2003CB314901),国家高技术研究发展计划(批准号:2007AA03Z418)及111项目(批准号:B07005)资助项目

<sup>\*</sup> 通信作者.Email:zhoujing@bupt.edu.cn 2008-04-24 收到,2008-05-22 定稿