A Novel 4T nMOS-Only SRAM Cell in 32nm Technology Node*

Zhang Wancheng† and Wu Nanjian†

(*State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing* 100083, *China*)

Abstract: This paper proposes a novel loadless 4T SRAM cell composed of nMOS transistors. The SRAM cell is based on 32nm silicon-on-insulator (SOI) technology node. It consists of two access transistors and two pull-down transistors. The pull-down transistors have larger channel length than the access transistors. Due to the significant short channel effect of small-size MOS transistors, the access transistors have much larger leakage current than the pull-down transistors, enabling the SRAM cell to maintain logic "1" while in standby. The storage node voltages of the cell are fed back to the back-gates of the access transistors, enabling the stable "read" operation of the cell. The use of back-gate feedback also helps to improve the static noise margin (SNM) of the cell. The proposed SRAM cell has smaller area than conventional bulk 6T SRAM cells and 4T SRAM cells. The speed and power dissipation of the SRAM cell are simulated and discussed. The SRAM cell can operate with a 0.5V supply voltage.

Key words: SRAM cell; SOI; 4T-SRAM; 32nm technology node
EEACC: 1265D
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2008)10-1917-05

1 Introduction

Static-random-access-memory (SRAM) cells are important components in modern VLSI circuits. Previous SRAM cells can be categorized into three types: six-transistor (6T) SRAMs, resistive-load four-transistor (4T) SRAMs, and loadless 4T SRAMs[1]. Both 6T SRAMs and resistive-load 4T SRAMs have relative large area. Moreover, it is not easy to scale down the supply voltage with the transistor size for 6T SRAMs[1]. On the other hand, the loadless 4T SRAMs promise smaller area and good scaling characteristics. A loadless 4T SRAM consists of 2 nMOS pull-down transistors and 2 pMOS access transistors (2n2p)[1]. The access transistors act as resistive loads when the SRAM cell is in the standby state. This is achieved by deliberately changing the pMOS threshold voltage[1], modifying device geometry[2], or using self-body-biased silicon-on-insulator (SOI) transistors[3,4]. All these methods introduce additional steps in the fabrication process. Recently, an SOI loadless 4T SRAM based on both front-gate feedback and back-gate feedback was proposed[5]. The use of back-gate feedback significantly enhances the SRAM cell's static noise margin (SNM) and reduces its static leakage current. However, the 2n2p structure of this cell limits any further reduction of the cell size.

In this paper, we propose a novel loadless 4T SRAM cell that is composed of all nMOS SOI transistors. The cell has two access transistors and two pull-down transistors. The short channel effect of 32nm technology node MOS transistors maintains the storage node voltage of the SRAM cell in the standby state without any process variation. The back-gate feedback method for SOI transistors is used to achieve a robust SRAM cell read operation. The SRAM cell has a smaller area than those previously proposed and it can operate with a 0.5V supply voltage. The SNM of the SRAM cell is 80mV. The read/write operation speeds are higher than 100MHz. In the following sections, we first show the circuit structure of the SRAM cell. Then we study the characteristics of the circuit by HSPICE. Finally, we discuss the SRAM cell performance and make a conclusion.

2 SRAM cell structure and operation principle

Figure 1 shows the schematic of the proposed 4T SRAM cell. It consists of two nMOS access transistors T1, T2, and two nMOS pull-down transistors N1, N2. All four transistors in the SRAM cell are fully-depleted SOI transistors. Each transistor has two gates, i.e., the front-gate and the back-gate. The transistors can be planar or dual-gate FINFETs. In the first case,

* Project supported by the National Natural Science Foundation of China (No. 90607007) and the Special Funds for State Key Development Program for Basic Research of China (No. 2006CB921201)
† Corresponding author. Email: zhangwc@red.semi.ac.cn; nanjian@red.semi.ac.cn
Received 6 May 2008, revised manuscript received 10 June 2008

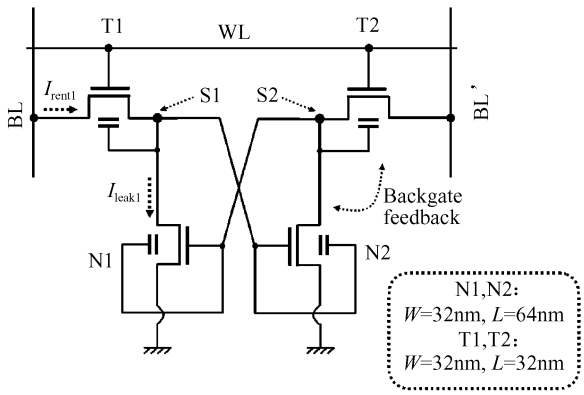

Fig. 1 Schematic of the 4T load-less SRAM cell that consists of word line WL, two bit lines BL and BL', and four transistors

the back-gate voltage is applied through a well contact formed through the BOX layer. The well of the transistors can be separated from each other by shallow trench isolation (STI)[5]. In the second case, the two gates are formed on the two sides of the 'fin'. A typical relationship between the drain current I_d and the front-gate voltage V_{fg} is shown in Fig. 2. The I_d-V_{fg} characteristic is modulated by the back gate voltage V_{bg}. With fixed positive $V_{bg} > 0.5$V, the transistor is always open due to the existence of the back channel. With fixed negative V_{bg}, the threshold voltage of the I_d-V_{fg} characteristic increases. When V_{bg} is same as V_{fg}, the drain current is much larger than the case when V_{bg} is fixed to be 0V.

The SRAM cell value (binary 0/1) and its inversion value are stored as the voltage of the storage node S1 and S2, respectively. S1 is connected to the back-gate of T1, the front-gate of N2, and the back-gate of N2, while S2 is connected to the back-gate of T2, the front-gate of N1, and the back-gate of N1. T1

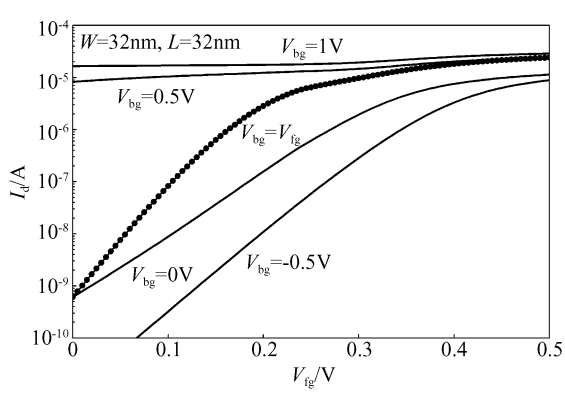

Fig. 2 Relationship between the drain current of the dual-gate SOI nMOS transistor with its front-gate voltage V_{fg}, modulated by various back gate voltages V_{bg} Parameters of the SOI transistor are: W = 32nm, L = 32nm, oxide thickness t_{ox} = t_{box} = 1.5nm, V_{th} = 0.35V. The SOI transistor was simulated by HSPICE using SPICE model of 32nm technology node SOI transistor[6].

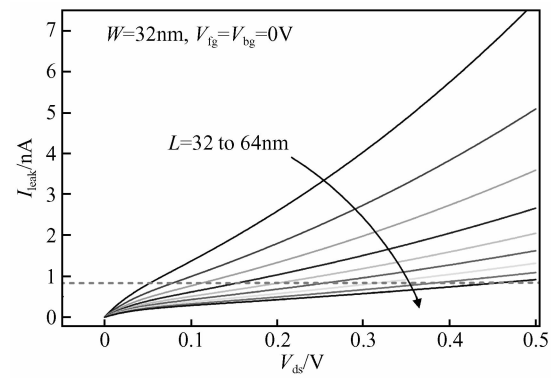

Fig. 3 Static leakage current of the SOI nMOS transistor as a function of drain-source voltage with 32nm channel width and different channel lengths ranging from 32 to 64nm

and T2 have the smallest feature size and largest width-to-length ratio (W/L = 1/1). On the other hand, both N1 and N2 have small width-to-length ratio (W/L = 1/2). In contrast to conventional 6T SRAMs, the two load pMOS transistors are eliminated. Compared to 2n2p structure 4T SRAM, the two pMOS access transistors are replaced by two nMOS access transistors.

The SRAM cell operates as follows. The write process of the SRAM cell is same as the conventional SRAM cell. The word line WL is high, and complementary voltages are applied to two bit lines BL and BL'. After write, the complementary voltages are stored in the storage nodes S1 and S2. In the retention mode, the word line WL is low, and T1 and T2 are closed. The two bit lines BL and BL' are kept high. The complementary voltage of S1 and S2 are feedback to N1 and N2. We assume S1 has a high voltage (near the supply voltage), and S2 has a low voltage (near the ground voltage). During retention, the voltage of S1 is fed back to T1, the equivalent back-gate voltage of T1 is 0, and thus the current through T1 is its static leakage current I_{rent1}. Since the voltage of S2 is fed back to N1, both the front-gate voltage and the back-gate voltage of N1 are 0, and the current through N1 is its static leakage current I_{leak1}. To hold the high voltage of S1, I_{rent1} must be much larger than I_{leak1}. This is achieved using the significant short-channel effect of small dimension MOS transistors. Figure 3 shows the relationship between the leakage current I_{leak} and the drain-source voltage V_{ds} of 32nm channel width nMOS transistors with different channel lengths L. With small channel length, the turn-off characteristic of the transistor deteriorates. Therefore, I_{leak} increases as L decreases. With the same V_{ds}, I_{leak} with L = 32nm is more than 10 times larger than I_{leak} with L = 64nm. Since BL is kept at the supply voltage, the voltage of S1 can remain high (near the

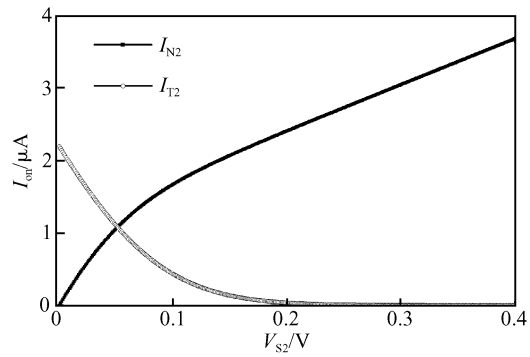

Fig. 4　Relationship of the ON current of N2 and T2 with the node voltage of S2　I_{N2} is much larger than I_{T2} when $V_{S2} > 0.1$V.

supply voltage) during retention. Since the voltages of S1 and S2 are complementary, the voltage of S2 is kept low during retention. Therefore, the retention of the SRAM cell is achieved using only nMOS transistors. On the other hand, with larger dimensions, the short-channel effect of MOS transistors is not so significant. With 65nm technology node, for example, the leakage current of T1 is only 1.4 times larger than the leakage current of N1, and thus the voltage of S1 cannot remain high. Therefore, this SRAM cell design is valid only in technology node below 45nm.

The read process of the SRAM cell is as follow. During read, WL is high and BL and BL' are connected to the sensitive amplifier. Initially, both BL and BL' have high voltages. T2 is opened, and N2 pulls down the bit line BL' to low value. For robust read operation, the ON current I_{N2} through N2 must be much larger than the ON current I_{T2} through T2, so that the voltage of S2 V_{S2} is kept near ground and thus the cell value can not be inverted. This is achieved using the back-gate feedbacks of N2 and T2. During read, both the front-gate voltage and the back-gate voltage of N2 are kept high. On the other hand, the front-gate voltage of T2 is high, but the back-gate voltage of T2 is kept 0. As shown in Fig. 2, when $V_{fg} = V_{bg}$, the drain current is much larger than the case when $V_{bg} = 0$. Therefore, with same drain-source voltage, the current through N2 is much larger than the current through T2, even though N2 has a smaller W/L ratio. Figure 4 shows the relationship between I_{N2} with V_{S2} and I_{T2} with V_{S2}. When V_{S2} is 0.1V, I_{N2} is already much larger than I_{T2}. During reading, the currents through N2 and T2 are the same, so the drain-source voltage of N2 is much smaller than T2. Therefore, during read V_{S2} can be held below 0.1V and thus the cell can sustain its stored value. In summary, the read operation of the SRAM cell is achieved using the back-gate feedback of the pull-down transistors.

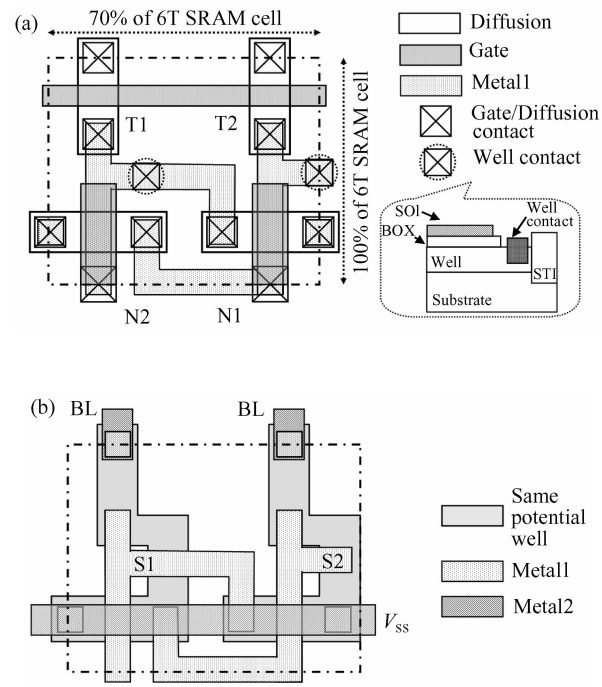

Fig. 5　One possible layout of the 4T all-nMOS SRAM cell (a) Schematic of the gate, diffusion and contact. Back-gate voltage is applied through the well contact, as shown in the inset; (b) Schematic of metal1 and metal2

3　Simulation results and performance

We use the latest predictive technology SPICE models of 32nm technology node SOI MOS transistors[6] to simulate the SRAM cell. The validity of the model has been proved by many works. The simulation SPICE level is BSIM4, which can model the short-channel effect and other quantum effects of MOS transistors below 90nm technology node[7].

Figure 5 shows a possible layout of the SRAM cell, which is composed of planar SOI transistors. The dashed outline indicates one cell. T1 and N2 lie in the left side, since their wells have the same potential. The cell is 70% as wide and 100% as long as the 6T SRAM cell, so it takes up only 70% of the area due to the elimination of pMOS transistors. Using vertical-gate SOI fin-Fet transistors instead of planar ones, the cell area can be further reduced.

Figure 6 shows the SNM butterfly diagram of the SRAM cell. The SNM of the SRAM cell in retention mode is: 80mV with $V_{dd} = 0.5$V; 65mV with $V_{dd} = 0.4$V. This value is nearly same as the SNM of 2n2p SRAM cells[9]. Therefore, the proposed all-nMOS SRAM cell has similar stability performance to the 2n2p SRAM cells. The SNM in retention mode can be improved by decreasing the W/L ratios of N1 and N2, so that the short-channel effects of T1 and T2 are relatively more significant. However, decreasing the

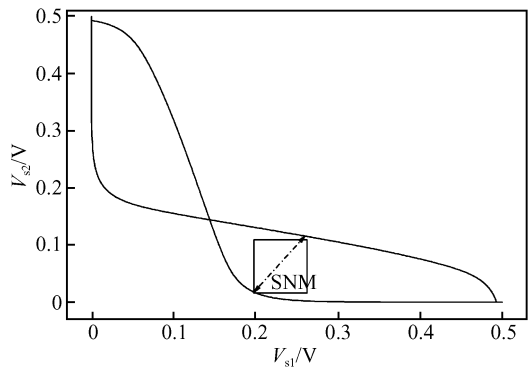

Fig. 6 Static noise margin butterfly diagram of the SRAM cell (The supply voltage is 0.5V.)

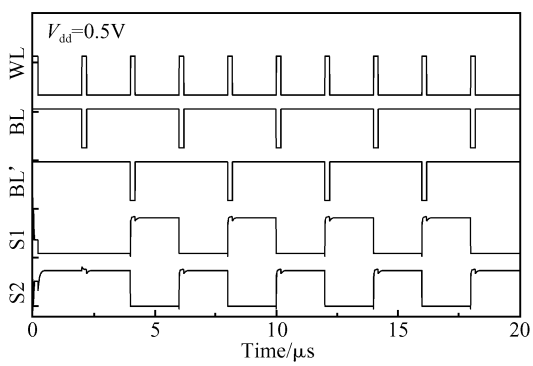

Fig. 7 Simulation result of the write process of the SRAM cell

W/L ratios of N1 and N2 will deteriorate the read operation stability and will increase the cell area.

Figure 7 shows the simulation result of the write process of the SRAM cell with $V_{dd} = 0.5$V. The cell operates correctly. The minimum supply voltage for the correct write/read operation is 0.32V. Lower supply voltage decreases the power dissipation as well as the SNM. Figure 8 shows the write delay and the leakage current as functions of the threshold voltage V_{th} of the nMOS transistors. The write delay increases exponentially as V_{th} increases. The leakage current decreases exponentially as V_{th} increases. Therefore, there is a tradeoff between the operation speed and power dissipation of the SRAM cell. With 0.35V V_{th}, the write delay is 200ps, and the leakage current is 130pA. This corresponds to a maximum 5GHz write speed and a 0.13W/1Gbit static power dissipation.

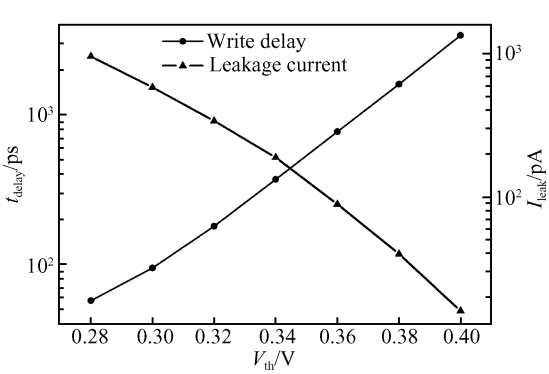

Fig. 8 Write delay and static leakage current as a function of the threshold voltage of the nMOS transistors

4 Conclusion

An all-nMOS four-transistor SRAM cell is proposed. For the first time, the short-channel effect of MOS transistors is used to facilitate the SRAM cell design. The SRAM cell has smaller area than previously proposed 4T cells, and no special fabrication process is required. For large-scale integration, the parameter dispersion of the MOS transistors should be carefully considered, since the leakage current of the access transistor seriously depends on its channel length. Moreover, the tradeoff between the operation speed and power dissipation and the tradeoff between the power dissipation with the SNM should be carefully managed. In conclusion, the proposed SRAM cell is promising for future high-density low-voltage SRAM applications.

References

[1] Noda K, Matsui K, Takeda K, et al. A loadless CMOS four-transistor SRAM cell in a 0.18μm logic technology. IEEE Trans Electron Devices, 2001, 48(12): 2851

[2] Kotabe A, Osada K, Kitai N, et al. A low-power four-transistor SRAM cell with a stacked vertical poly-silicon pMOS and a dual-word-voltage scheme. IEEE J Solid-State Circuits, 2005, 40(4): 870

[3] Terauchi M. A novel 4T SRAM cell using 'self-body-biased' SOI MOSFET structure operating at 0.5volt. IEEE International SOI Conference, 2000: 108

[4] Yu Yang, Zhao Qian, Shao Zhibiao. A low power SRAM/SOI memory cell design. Chinese Journal of Semiconductors, 2006, 27(2): 318

[5] Yamaoka M, Osada K, Tsuchiya R, et al. Low power SRAM menu for SOC application using yin-yang-feedback memory cell technology. IEEE Symposium on VLSl Circuits Digest of Technical Papers, 2004: 288

[6] Zhao W, Cao Y. New generation of predictive technology model for sub-45nm design exploration. Proc ISQED, 2006: 585

[7] Dunga M V, Yang W, Xi X, et al. BSIM4 MOSFET model. http://www-device.eecs.berkeley.edu/bsim3/~bsim4.html

[8] Chappell B, Schuster S E, Sai-Halasz G A. Stability and SER analysis of static RAM cells. IEEE J Solid-State Circuits, 1985, 20(1): 383

[9] Thomas O, Amara A, Vladimirescu A. Stability analysis of a 400mV 4-transistor CMOS-SOI SRAM cell operated in subthreshold. IEEE Conference on Electron Devices and Solid-State Circuits, 2003: 247

一种全 nMOS SOI 晶体管 4 管静态存储器单元*

张万成†　吴南健†

（中国科学院半导体研究所 半导体超晶格国家重点实验室，北京　100083）

摘要：提出了一种新颖的无负载 4 管全部由 nMOS 管组成的随机静态存储器（SRAM）单元.该 SRAM 单元基于 32nm 绝缘体上硅（SOI）工艺结点，它包含有两个存取管和两个下拉管. 存取管的沟道长度小于下拉管的沟道长度.由于小尺寸 MOS 管的短沟道效应，在关闭状态时存取管具有远大于下拉管的漏电流，从而使 SRAM 单元在保持状态下可以维持逻辑“1”.存储节点的电压还被反馈到存取管的背栅上，使 SRAM 单元具有稳定的“读”操作.背栅反馈同时增强了 SRAM 单元的静态噪声容限（SNM）.该单元比传统的 6 管 SRAM 单元和 4 管 SRAM 单元具有更小的面积.对 SRAM 单元的读写速度和功耗做了仿真和讨论.该 SRAM 单元可以工作在 0.5V 电源电压下.

关键词：SRAM 单元；绝缘体上硅；4 管；32nm 工艺结点
EEACC：1265D
中图分类号：TN402　　**文献标识码**：A　　**文章编号**：0253-4177(2008)10-1917-05

* 国家自然科学基金（批准号：90607007）及国家重点基础研究发展规划（批准号：2006CB921201）资助项目
† 通信作者.Email：zhangwc@red.semi.ac.cn；nanjian@red.semi.ac.cn
2008-05-06 收到，2008-06-10 定稿