A 3V 5.88mW 13b 400kHz Sigma-Delta Modulator with 84dB Dynamic Range

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Abstract: This paper introduces a high-revolution, 200kHz signal bandwidth ΣΔ modulator for low-IF GSM receivers that adopts a 2-1 cascaded single-bit structure to achieve high linearity and stability. Our design is realized in a standard 0.18μm CMOS process with an active area of 0.5mm×1.1mm. The ΣΔ modulator is driven by a single 19.2MHz clock signal and dissipates 5.88mW from 3V power supply. The experimental results show that, with an oversampling ratio of 48, the modulator achieves a 84.4dB dynamic range, 73.8dB peak SNDR, and 80dB peak SNR in the signal bandwidth of 200kHz.

Key words: cascaded sigma-delta modulator; analog-digital converter; switched-capacitor circuits; operational amplifiers; CMOS analog integrated circuits

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1 Introduction

As CMOS technology develops, system integration for wireless communication applications has become more popular. In order to reduce the manufacturing costs, the conversion module that changes analog signals to digital ones should be put as close as possible to the antenna, so that the system can primarily process signals in the digital domain. Analog-to-digital converters (ADC), which connect the analog and digital worlds, are the key conversion module and should have high dynamic range and low power consumption. Among all kinds of ADCs, the sigma-delta (ΣΔ) ADC is a good choice for integration design. For over-sampling and noise-shaping techniques, the ΣΔ ADC offers high resolution without complex analog components or excessive matching requirements. In addition, ΣΔ ADCs ease the difficulty in forward anti-aliasing filters design due to high over-sampling ratio. In this paper, the design and measurement of a ΣΔ modulator for low-IF GSM receiver is reported. Implemented in standard 0.18μm CMOS technology, our modulator achieves a 200kHz signal bandwidth with 13bit resolution.

2 2-1 cascaded system design

There are two structures for high-order ΣΔ modulator build-up: single-loop[1] and cascade (MASH)[2]. Compared with cascade structure, single-loop is less sensitive to analog circuit imperfection. However, it might be unstable when the order is higher than two. The instability can be solved by preventing internal signals from overload when low integration gain factors are selected. However, in that case, the SNR would be much worse than the corresponding ideal one. Besides, in order to realize the low gain factors, the single-loop requires large integration capacitances, and those capacitances lead to high parasitic bottom capacitances at the amplifier outputs. According to the above analysis, a 2-1 cascade structure is selected in this paper for its high linearity and stability.

2.1 Implementation approach

First, for a high resolution ΣΔ modulator with minimum power, we should select a proper implementation approach. There are three implementation approaches for ΣΔ modulators: continuous-time[3], switched-current[4], and switched-capacitor[5].

(1) The continuous-time approach has an inherent anti-aliasing effect and can release the requirement of amplifier signal-setting, thus reducing the overall power consumption of the system. However, a continuous-time ΣΔ modulator has difficulties in achieving high dynamic range due to its high sensitivity to non-idealities of the CMOS circuits, such as clock jitters[6], excess loop delay[6], and process variation[7].

(2) The switched-current approach seems appealing because it can use smaller capacitors and lower supply voltage to implement modulators without linear capacitors requirement. However, it is difficult to obtain high linear performance under low supply voltage, and power in this approach is much higher.

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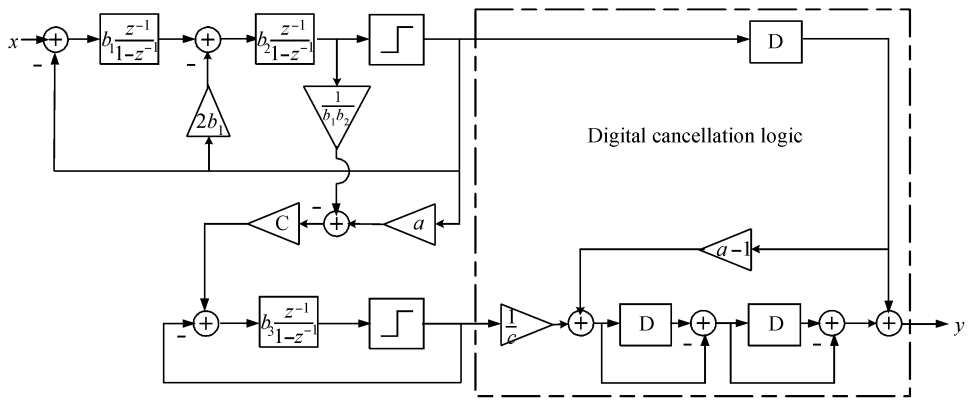

Fig.1　2-1 cascade structure of the ΣΔ modulator

(3) In the switched-capacitor approach, the accuracy is insensitive to the circuit non-idealities mentioned above and a very high resolution can be achieved. Therefore, the system design in this paper adopts the switched-capacitor approach.

2.2　Over-sampling ratio

The ideal dynamic range of a ΣΔ modulator with single-bit quantizer is expressed as[8]

$$\begin{aligned} DR &= \frac{\text{Average Power of Maximal Input Signal}}{\text{Average Power of Noise in Signal Bandwidth}} \\ &= \frac{\frac{1}{2}V_{ref}^{\ 2}}{\frac{\pi^{2L}}{2L+1}\times\frac{1}{M^{2L+1}}\times\frac{V_{ref}^{\ 2}}{3}} \\ &= \frac{3}{2}\times\frac{2L+1}{\pi^{2L}}M^{2L+1} \end{aligned} \tag{1}$$

where L, M, V_{ref} represent the order of modulator, over-sampling rate, and the input reference voltage, respectively.

Equation (1) demonstrates that high resolution could be achieved by increasing M or L. When the order L is determined, Eq. (1) can help us choose a proper over-sampling rate M. However, this equation still encounters some limitations in practice. For instance, it focuses on quantization noise but does not take thermal noise and circuit noise into account. It also neglects the fact that the amplifiers' finite gain and the capacitors' mismatch may cause the quantization noise induced by the first stage to leak into the output, and consequently degrade the SNR. Regarding the above considerations and extra margin for other non-ideal factors, the over-sampling rate is set to be 48, which is bigger than the ideal one.

The 2-1 cascade single-bit structure of the proposed ΣΔ modulator is shown in Fig. 1. The MATLAB simulation results are illustrated in Fig. 2. The peak SNDR is 89dB and the overload level is −3dBFs. By properly selecting the coefficients b_1, b_2, b_3, the output swing of each integrator is controlled to less than ±1.5V when the input signal is overloaded. Meanwhile, a ±1.5V output swing is not difficult to implement in 3V power supply.

2.3　Non-ideal effect

In order to achieve high resolution and linearity, several non-ideal effects should be considered.

2.3.1　Thermal noise

Sampling capacitors selection is critical for saving power and chip area. Besides the quantization noise, thermal noise generated by the sampling process should also be taken into account. For a 2-1 cascaded structure, the total noise power is:

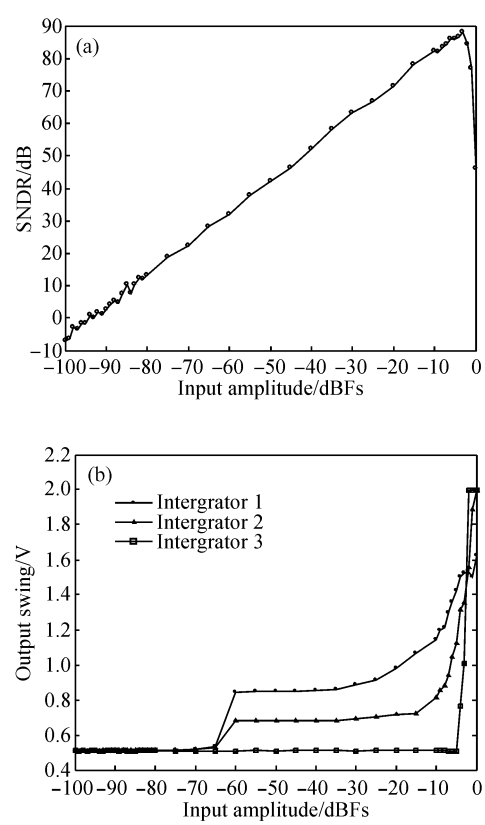

Fig.2　MATLAB simulation results　(a) SNDR versus input amplitude; (b) Output swing of each integrator

$$S_{N_{in}} = \frac{1}{M}S_{N_1} + \frac{1}{b_1^2} \times \frac{\pi^2}{3M^3}S_{N_2} + \frac{1}{b_1^2 b_2^2} \times \frac{\pi^4}{5M^5}S_{N_3}$$

where S_{N_1}, S_{N_2}, S_{N_3} represents the input noise power from the 1st, 2nd, and 3rd integrator, respectively. The coefficient of S_{N_1} and S_{N_2} is smaller than that of S_{N_3}, thus the specification of the last stage's operational amplifier could be released.

The sampling noise power of a differential integrator with sampling capacitor C_s is given by[8]

$$v_{ns}^2 = \frac{4kT}{C_s} \times 2 \tag{2}$$

The sampling capacitor of the first integrator is derived from Eq.(2) to ensure that the thermal noise does not affect the total performance. Because the noise power of the 2nd and 3rd integrator is greatly attenuated relative to that of the 1st integrator, the sampling capacitors in these integrators could be scaled down to save power without performance degradation.

2.3.2 Mismatch

Due to capacitor mismatch in the cascade structure, the factors of the analog part (modulator), a and c will not perfectly match those of the digital part (noise cancellation logic), $\hat{a}$ and $\hat{c}$, which will affect the performance badly. So the capacitor mismatch should be considered at the system level.

Considering the mismatch effect, the total power of quantization noise is presented as

$$S_{ee} = \left[\delta_c^2 \frac{\pi^4}{5M^5} + (-\hat{a}(\delta_a + \delta_c + \delta_a\delta_c) + \delta_c)^2 \frac{\pi^8}{9M^9}\right]\sigma_{Q1}^2 + \frac{1}{\hat{c}^2} \times \frac{\pi^6}{7M^7}\sigma_{Q2}^2 \tag{3}$$

where

$$a = \hat{a}(1 + \delta_a), c = \hat{c}(1 + \delta_c)$$

σ_{Q1} and σ_{Q_2} represent the quantization noise power from the first and second quantizer, respectively.

In order to confine no more than 1dB difference of quantization noise between unmatched and matched situations, the following requirement should be met.

$$\begin{aligned}\delta_c &< \sqrt{\frac{5(10^{0.1} - 1)}{7}} \times \frac{\pi}{\hat{c}M} \\ &< 0.43\frac{\pi}{\hat{c}M} \\ &< 5.6\%\end{aligned}$$

It shows that there is no limitation for δ_a. The matching requirement of δ_c could be met using a large-size unit capacitor, like 200fF, and dummy capacitors to provide a similar process environment.

2.3.3 Operational amplifier open-loop gain

The finite amplifier gain may cause integrator gain error. The MATLAB simulation shows that the first two integrators need a DC gain higher than 80dB, while the last one only needs a DC gain as low as 60dB without degrading SNR. However, considering process and temperature variations as well as margin saving for non-ideal factors, amplifiers need a higher nominal gain to achieve sound noise shaping and linearity.

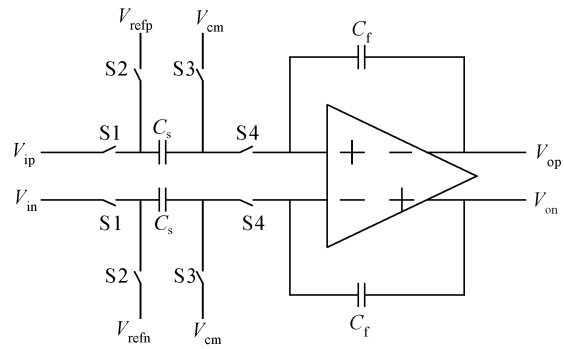

Fig.3 Structure of switched-capacitor integrator

3 Circuit design

3.1 Integrator design

As the basic and essential model in the sigma-delta modulator, a switched capacitor integrator (Fig. 3) is adopted here for its high accuracy and low sensitivity to clock jitter. It samples the reference voltage and input signal by the same capacitor, reducing the load capacitance of the present and former stages, and hence the total power consumption is lowered accordingly. A four-phase clock is used to eliminate the charge injection and clock feed-through effect which may bring harmonic distortion.

There are three kinds of switches adopted in the integrator: CMOS switch (S1, S2), nMOS switch (S3), and an advanced nMOS switch (S4) (Fig. 4). CMOS switches are used to connect input signals and reference voltages that have large variations during operation. The advanced nMOS switches are connected to common-mode voltage, and consist of an nMOS switch and another two nMOS transistors driven by an opposite control voltage. The structure counteracts part of the charge feed-through. The worst consequence of this structure is that when all the charge feeds into one side, the structure has no improvement. However, except for this condition, it will always

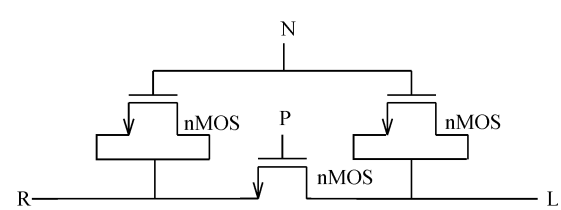

Fig.4 Structure of the advanced nMOS switch

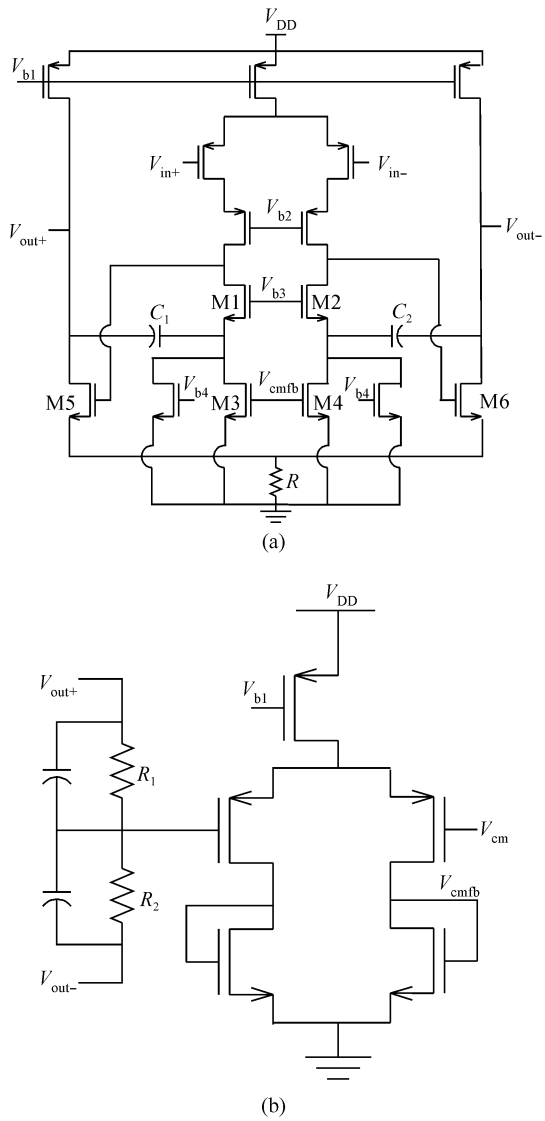

Fig.5　OTA structure　(a) OTA; (b) CMFB circuit

counteract part of the charge feed-through. The best consequence happens when the charge is divided evenly between each side, completely counteracting the charge feed-through of the switch.

3.2　Operational trans-conductance amplifier (OTA) design

The amplifier uses most of the power in the system. Its structure selection is based on the requirements of DC gain, gain bandwidth production (GBW), and output swing. Although an amplifier with a cascode output stage is capable of achieving high DC gain and GBW, it suffers from a limited output swing, which may affect active operation under low voltage. A two-stage with common-source output structure, on the other hand, could meet the requirements of high DC gain and moderate GBW with larger output swing, less power consumption, and lower circuit noise. Therefore, the two-stage with common-source output structure is adopted in this design (Fig. 5).

Table 1　AC simulation results of OTA

Corner	Temperature /℃	Open-loop gain/dB	GBW /MHz	Phase margin /(°)
TT	27	98	158	69
SS	120	99	128	69
FF	0	97	173	69

In this structure, the first stage of the amplifier uses cascode structure to provide high DC gain, while the second stage implemented by common-source structure applies large output swing (for example 1.5V under 3V supply voltage), which is enough for the present system design. The differential pair is made up of pMOS due to its low flicker noise. Because the output resistor of the amplifier is not very large, the output common voltage could be derived from dividing voltage implemented by resistors R_1, R_2 of 100K. It feeds back to the pseudo-transistor by controlling its gate voltage after comparing it with the reference common output voltage. Regarding stability, the pseudo-transistor is divided into two parts, one part offers feedback signal, while the other part supplies current as normal. In order to improve phase margin, Ahuja compensation[9] is adopted because it can achieve good frequency performance with no extra components. This structure has a potential risk that the nMOS transistors M1～M4 may be pressed to the linear region because their source-drain voltage are limited by the M5～M6's gate voltage. As a result, a proper resistor R is added under M5 and M6 to eliminate the limitation, so that the amplifier is working normally under all corners. The simulation results of the OTA are listed in Table 1, where the circuit is verified in 3 different corners.

3.3　Comparator design

Single bit quantizer, a comparator, is shown in Fig. 6. The offset requirement of the comparator in sigma-delta ADC is moderate and easy to meet. In this design, fast regeneration speed (less than one clock period) and low power consumption are the largest concerns. The proposed structure consists of a differential input pair (M01), a top and bottom regeneration loop (M02, M04), and switches (M05, M06). The differential input pair is used to isolate the following digital circuits and reduce the kickback effect to the former integrator. The regeneration loop is adopted to amplify the small signal to full voltage swing. The switches are used to provide a reset signal. The structure is followed by an R-S latch to store the results of the comparator and some series converters cascaded as a buffer to offer enough drive power.

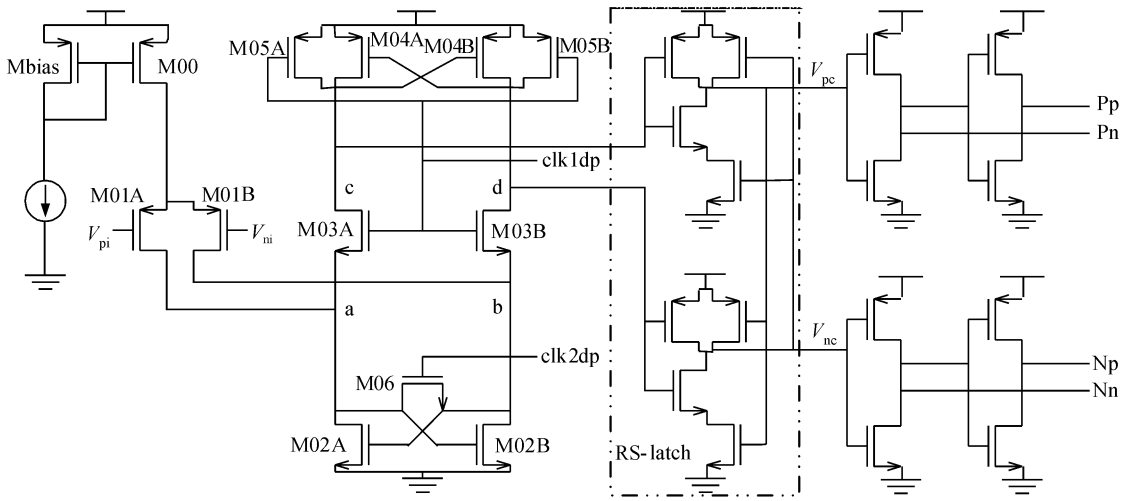

Fig. 6 Comparator schematic

3.4 Layout design

The modulator's layout is shown in Fig. 7. The digital and analog circuit parts are isolated by a protection ground and are connected to digital and analog power supplies, respectively. The sampling and integration capacitors are made of square shape and enclosed by dummy capacitors to achieve high matching requirement. The modulator is designed using standard 0.18μm CMOS technology with a core area of 0.5mm × 1.1mm. The total area including pads is 0.7mm×1.5mm.

4 Experimental results

The measured output spectrum of modulator is illustrated in Fig. 8. MATLAB was used to do FFT for the digital cancellation logic and the decimation filtering during the performance evaluation. The DC output spectrum shows that the noise floor of the modulator is −85.8dBFs. The frequency of input sine signal is selected to be 60kHz to enable the second and third order distortion to fall into the 200kHz baseband, thus making the result more accurate. It shows that the second order distortion is −93.6dB, and the third is −76.7dB. Figure 9 illustrates the measured SNR/SNDR as a function of input amplitude. The peak SNR and SNDR achieves 80 and 73.8dB when input signal is −7dBFs. The dynamic range of the modulator is 84.45dB because the overload level is −1.35dBFs. An abstract of the measured characteristic of modulator is listed in Table 2.

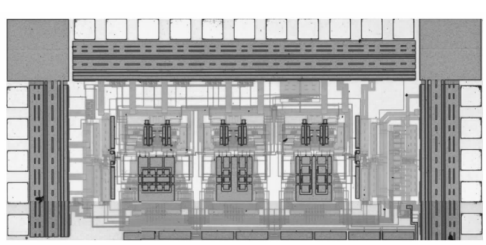

Fig. 7 Microphotography of the modulator

5 Conclusion

This paper presents the design of a 2-1cascaded single-bit sigma-delta modulator for low-IF GSM receiver. The modulator is implemented in 0.18μm

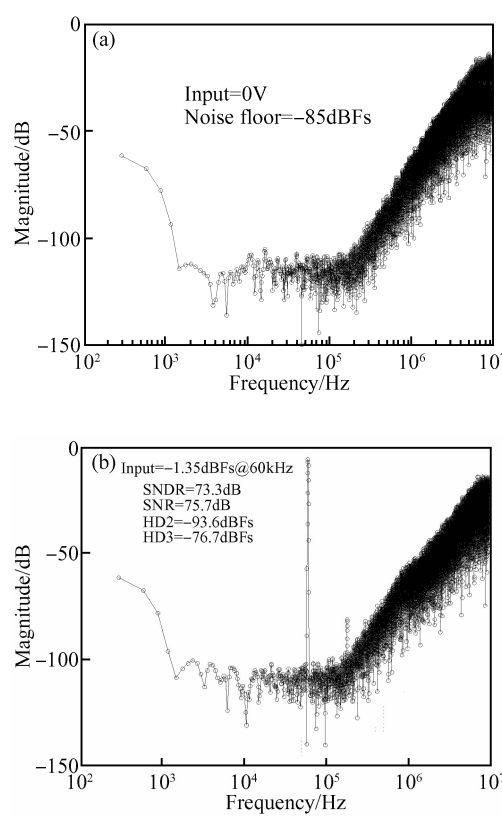

Fig. 8 Measured output spectrum after decimation (a) Noise floor; (b) Output spectrum when −1.35dBFs sinusoidal signal input

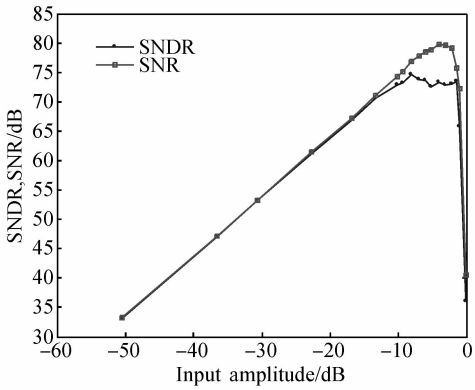

Fig.9　Measured SNR/SNDR as a function of input amplitude

Table 2　Measured characteristics of the modulator

Specification	Measurement result
Power supply	3V
Reference voltage	±1V(diff)
Signal bandwidth	200kHz
Sampling frequency	19.2MHz
Overload level	−1.35dBFs
Dynamic range	84.45dB
Peak SNR	80dB
Peak SNDR	73.8dB
Static power consumption	5.88mW
Active area	0.55mm^2
Technology	0.18μm CMOS

CMOS technology and occupies 0.5mm × 1.1mm area. The experimental results show that the modulator achieves a dynamic range of 84.45dB and a peak SNDR of 73.8dB. The bandwidth is 200kHz and the sampling frequency is 19.6MHz. The modulator dissipates less than 6mW static power from a 3V supply.

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84dB 动态范围 13b/400kHz/3V/5.88mW ΣΔ 模数转换器

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摘要： 介绍了一个 200kHz 信号带宽、用于低中频结构 GSM 射频接收机的高精度 ΣΔ 调制器. 为了达到高线性和稳定性，调制器采用 2-1 级联单比特的结构实现. 电路在 0.18μm CMOS 工艺下流片验证，核心面积为 0.5mm×1.1mm. 调制器工作在 19.2MHz 的采样频率，在 3V 电源电压下功耗为 5.88mW. 测试结果表明，在 200kHz 信号带宽，过采样率为 64 的条件下，调制器达到 84.4dB 动态范围，峰值 SNDR 达到 73.8dB，峰值 SNR 达到 80dB.

关键词： 级联 ΣΔ 调制器；模数转换器；开关电容；运算放大器；CMOS 模拟积分电路

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