A PVT Tolerant Sub-mA PLL for High Speed Links*

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Abstract: A sub-mA phase-locked loop fabricated in a 65nm standard digital CMOS process is presented. The impact of process variation is largely removed by a novel open-loop calibration that is performed only during start-up but is opened during normal operation. This method reduces calibration time significantly compared with its closed-loop counterpart. The dual-loop PLL architecture is adopted to achieve a process-independent damping factor and pole-zero separation. A new phase frequency detector embedded with a level shifter is introduced. Careful power partitioning is explored to minimize the noise coupling. The proposed PLL achieves 3.1ps RMS jitter running at 1.6GHz while consuming only 0.94mA.

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1 Introduction

The bandwidth demands for inter-chip communication are continuously increasing. The higher data rate gives less timing margin for data transfer, so the PLLs that can provide low jitter clocks in a noisy digital environment containing high performance UPS and high density memory are required.

The impact of PVT variation is getting worse with technology scaling. For PLL design, the loop parameters such as damping factor and phase margin change with PVT variations significantly. The higher operating frequency and the continuous shrinking of the supply voltage with process scaling lead to ring oscillators with a very large tuning gain (several GHz/V). The higher sensitivity of the ring oscillators to the temperature makes the situation even worse. Some PVT tolerant PLLs have been developed[1~4]. In this paper, we adopt a dual-loop architecture[1], which provides a tracking mechanism to achieve a process-independent damping factor and pole-zero separation. A novel open-loop calibration is performed only during start-up, so that the impact of process variation on the oscillators is largely removed. The current controlled oscillator (ICO) is supplied by a current source biased from a bandgap current reference to mitigate the effect of temperature variation.

The power supply noise is the dominant contributor for clock jitter in a mixed signal SoC with large digital circuits. In this design, we partition the power supply network carefully to minimize the coupled supply noise. Several kinds of regulators are adopted to trade off between PSRR, noise coupling, and voltage headroom.

2 Architecture

The top level diagram of the dual-loop PLL is shown in Fig. 1. The PLL achieves the stabilizing zero by the proportional path. The s-domain open-loop transfer functions for the integral and proportional path are:

$$H_{\text{int}}(s) = \frac{I_{\text{cpi}}}{2\pi} \times \frac{1}{sC_{\text{int}}} g_{\text{mi}} \tag{1}$$

$$H_{\text{prop}}(s) = \frac{I_{\text{cpp}}}{2\pi} \times \frac{K_{\text{mir}}}{1 + sC_{\text{p}}R_{\text{p}}} \tag{2}$$

Small signal analysis shows the open-loop and closed-loop transfer functions of the PLL are, respectively,

$$H_{\text{OL}}(s) = [H_{\text{int}}(s) + H_{\text{prop}}(s)] \frac{K_{\text{ICO}}}{s} \tag{3}$$

$$H_{\text{CL}}(s) = \frac{NH_{\text{OL}}(s)}{N + H_{\text{OL}}(s)} = \frac{NK_{\text{ICO}}\left[\frac{I_{\text{cpi}}}{2\pi} \times \frac{g_{\text{mi}}}{C_{\text{int}}}(1 + sC_{\text{p}}R_{\text{p}}) + \frac{I_{\text{cpp}}}{2\pi}K_{\text{mir}}s\right]}{Ns^2(1 + sC_{\text{p}}R_{\text{p}}) + K_{\text{ICO}}\left[\frac{I_{\text{cpi}}}{2\pi} \times \frac{g_{\text{mi}}}{C_{\text{int}}}(1 + sC_{\text{p}}R_{\text{p}}) + \frac{I_{\text{cpp}}}{2\pi} \times K_{\text{mir}}s\right]} \tag{4}$$

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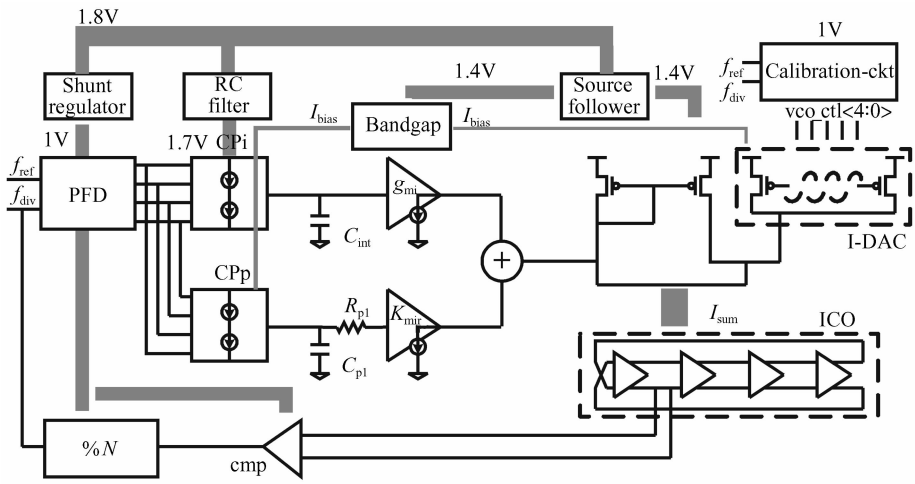

Fig. 1 Top view of the PLL

The main ripple pole $f_p = 1/2\pi R_p C_p$ presents high reference spurs and noise attenuation. This pole is far above the bandwidth of the PLL to ensure the stability of the system, so it can be ignored when we analyze the loop characteristic. Equation (4) can be rewritten as

$$H_{CL}(s) \approx \frac{K_{ICO}\left(\frac{I_{cpi}}{2\pi} \times \frac{g_{mi}}{C_{int}} + \frac{I_{cpp}}{2\pi} K_{mir} s\right)}{s^2 + \frac{K_{ICO}}{N}\left(\frac{I_{cpi}}{2\pi} \times \frac{g_{mi}}{C_{int}} + \frac{I_{cpp}}{2\pi} K_{mir} s\right)} = \frac{N\omega_n^2\left(1 + \frac{s}{\omega_z}\right)}{s^2 + 2\zeta\omega_n + \omega_n^2} \quad (5)$$

From Eq. (5), we can get the following expressions for the loop, the nature frequency (f_n), stabilizing zero (f_z), damping factor (ξ), and pole/zero separation:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_{ICO} I_{cpi}}{N} \times \frac{g_{mi}}{2\pi C_{int}}} \quad (6)$$

$$f_z \cong \frac{I_{cpi} g_{mi}}{I_{cpp} 2\pi K_{mir} C_{int}} \quad (7)$$

$$\xi = \frac{I_{cpp}}{I_{cpi}} \times \frac{K_{mir}}{2}\sqrt{\frac{K_{ICO} I_{cpi}}{N} \times \frac{C_{int}}{2\pi g_{mi}}} \propto \sqrt{\frac{C_{int}}{C_{ICO}} V_{const}} = \text{const.} \quad (8)$$

$$f_p/f_z = \frac{C_{int}}{C_p} \times \frac{I_{cpp}}{I_{cpi}} \times \frac{R_i}{R_p} K_{mir} \quad (9)$$

where I_{cpi} and I_{cpp} are the charge-pump currents of the integral and proportional path, R_i and R_p are the integral and proportional path degeneration resistors, g_{mi} is the integral path transconductance given by the inverse of R_i, K_{ICO} is the gain of the current controlled oscillator, C_{int} and C_p are the integral and proportional path capacitors, C_{ICO} is the load capacitance of the ICO, K_{mir} is the gain of the ICO driving current mirror of the proportional path, N is the frequency divider ratio, and V_{const} is a constant voltage with low process variation as shown in the following section.

These equations show that the pole-zero separation suffers low process variation as it is given by the ratios of currents, capacitors, and resistors. With this architecture, we also get an almost process-independent damping factor, which is important to achieve low jitter. The simulated phase noise of the PLL over PVT variations using a traditional third-order passive filter is shown in Fig. 2. In our simulation, the RMS jitter integrating phase noise from 1kHz to 100MHz offset changes from 2.9 to 6.0ps due to PVT variation when the PLL works at 1.6GHz. The impacts of the PVT variations on the traditional and the proposed PLL are summarized in Table 1.

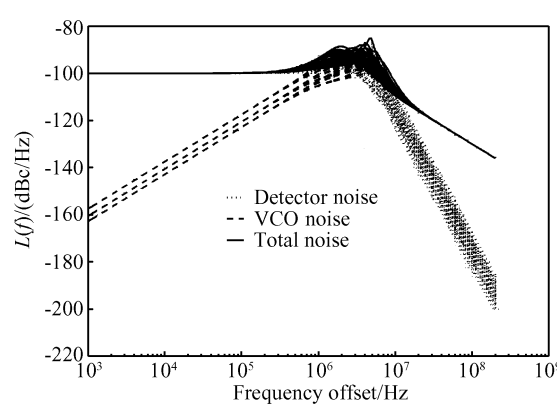

Fig. 2 Simulated phase noise of the traditional PLL under PVT variations

Table 1 Impact of PVT variations

Parameter	Traditional	This work
K_{VCO}	3GHz/V	600MHz/V
f_p/f_z	32±6	32±2
ξ	0.75～1.4	0.95～1.1
J_{RMS}(1kHz～100MHz)	2.9～6.0ps	2.6～3.1ps

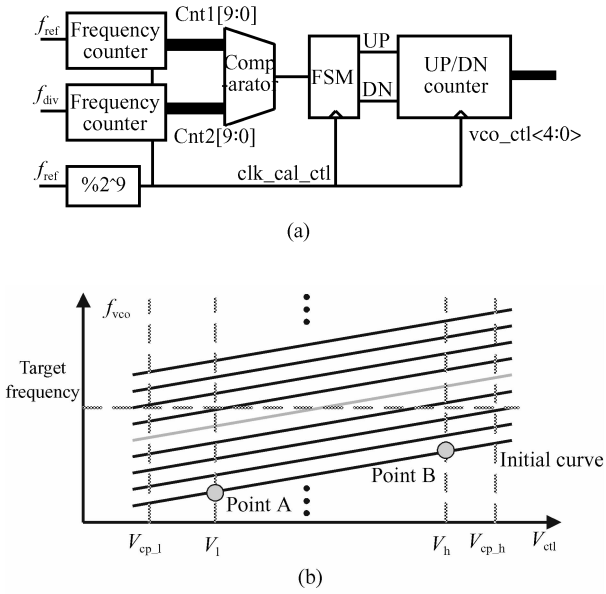

Fig. 3　Calibration block　(a) Calibration block; (b) Multi-range VCO curves

3　Building blocks

3.1　Calibration block

Keeping the oscillator gain small is important for noise performance because the oscillator noise in a PLL is directly proportional to its gain. To ensure that the oscillators work properly under all PVT conditions, multi-range VCOs have been developed[5,6].

In this design, a novel open-loop calibration is proposed that is performed only during PLL start-up. The open-loop operation reduces the calibration time significantly compared with its closed-loop counterpart[5], which is constrained by the settling time of the PLL. Figure 3 explains the principle of the calibration. In Fig. 3(b), $V_{cp\text{-}l}$ and $V_{cp\text{-}h}$ are the limit of the output range of the charge pump; V_l and V_h are the predefined voltages to provide enough margin for the oscillator when it experiences V_T variation after calibration. Because of the low supply voltage, choosing proper V_l and V_h values to reserve enough margin for V_T variations while keeping overlaps in adjacent curves is important. During calibration, we compare the oscillation frequency of the VCO with the reference clock by two frequency counters. If clk_cal_ctl is high, the VCO is biased at point A and the calibration block judges whether the VCO is slower than the target frequency; otherwise, the VCO is biased at point B and judges whether the VCO is faster than the target frequency. The calibration is over when both conditions are satisfied, otherwise, shifting to the upper curve. This calibration can lower the VCO gain several times by removing the impact of process variation on the oscillator. In our case, the VCO gain goes down from 3GHz/V to 600MHz/V.

3.2　Phase frequency detector and charge pump

The proposed phase frequency detector[7] is shown in Fig. 4(a). The inputs go through a series of inverters to generate a capture pulse at each positive edge of the reference and feedback clock. The internal nodes int_up_n and int_dn_n are charged to 1.8V by the reset signal rst and then rst is charged to 1.8V waiting for the capture pulse. Weak keepers are added between the internal nodes int_up_n and int_upb, int_dn_n and int_dnb to overcome the leakage current and charge sharing effect. The dynamic circuit not only improves the operation speed, but also converts 1V input to 1.8V output.

The charge pump is shown in Fig. 4(b). A dynamic current matching feedback loop is implemented by adding an amplifier to drive the gates of the pMOS current mirrors such that the source and sink currents are well matched. The decouple capacitor C_d is used to reduce the ripple on the node pbias and also as a compensation capacitor to stabilize the negative feedback loop. The noise of the current mirror devices is filtered-out using two low corner frequency RC filters (LPF1, LPF2), as shown in Fig. 4(b). The start-up circuit is added to prevent circuits from falling into the cut-off state.

3.3　Current controlled oscillator and bandgap

The diagrams of the ICO and bandgap are shown in Fig. 5. The ICO is supplied by a 5bit current DAC biased through the bandgap reference and the current from the current loop filter. The current DAC uses a cascoded mirror to increase output impedance and improve PSRR. The source degeneration resistor R_d is used to further reduce the noise contribution of the current mirror. In series with an active low pass filter, the current DAC provides at least 50dB PSRR for the ICO over the whole bandwidth.

A current reference[8] with a low temperature coefficient is implemented as the reference of the current DAC. This can reduce the margin requirement of the ICO for V_T variations, lowering the ICO gain. The reference current is given by

$$I_{bg} = (1/R_{bg})(\kappa T/q)\ln N + V_{be}/R_1 \qquad (10)$$

The first contribution is PTAT, while the second decreases with the temperature; by choosing N, R_{bg}, R_1 properly, we can make $dI/dT \approx 0$. A four-stage ring inverter-based oscillator was adopted for its low-voltage operation capability. Cross-coupled inverters are added at the output of each pseudo-differential inverter to improve the waveform symmetry and thus

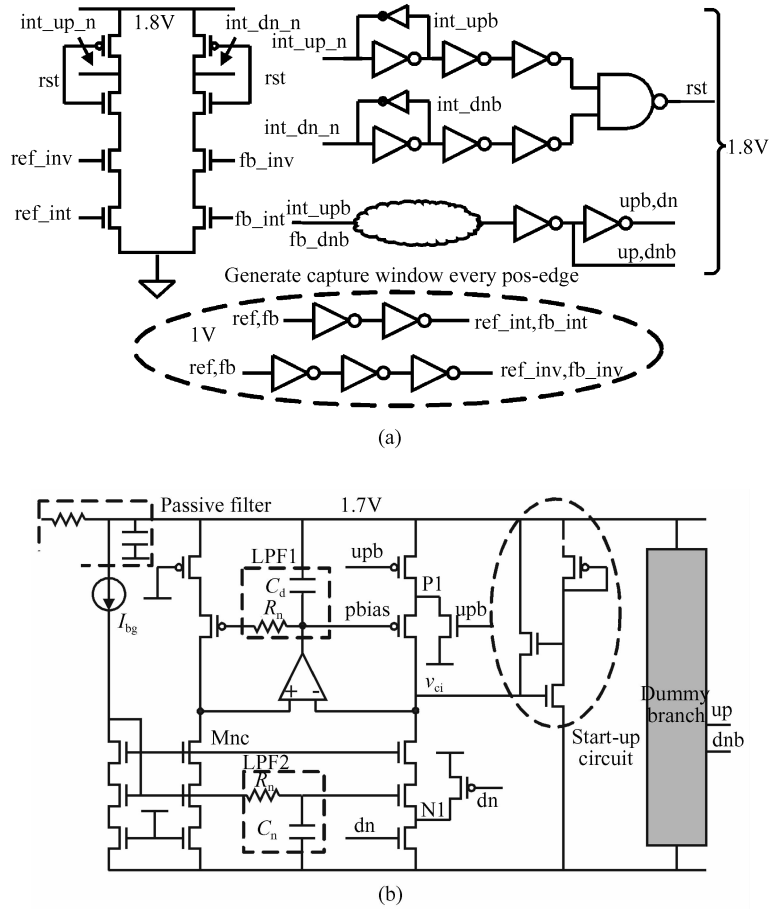

Fig. 4 PFD and charge pump (a) Phase frequency detector; (b) Charge pump

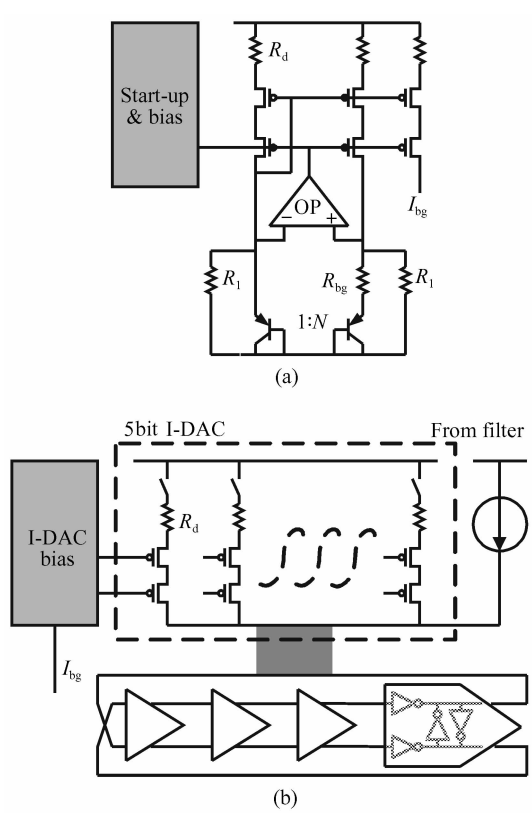

Fig. 5 Bandgap and ICO (a) Current bandgap reference; (b) Current control oscillator

reduce the flicker noise up-conversion.

3.4 Loop filter

This design uses a current-mode loop filter with a feedforward path that leads to a low area of on-chip capacitance and a smaller noise contribution[1]. The integral path transconductance stage is shown in Fig. 6(a). It has a large source degeneration resistor to stabilize its transconductance over a large current range ($g_{mi} = 1/R_i$). The self-biased and cascoded current mirror improves PSRR significantly. The source degeneration resistor (R_d) of the current mirror increases the output impedance and reduces its noise contribution. The proportional path shown in Fig. 6 (b) is realized as a current mirror that magnifies the

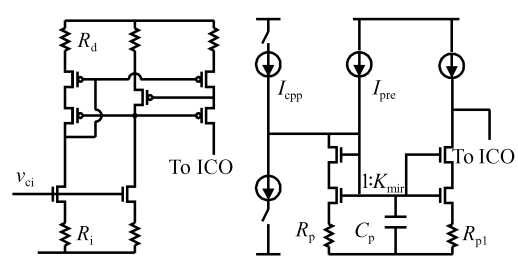

Fig. 6 Loop filter (a) Integral path; (b) Proportional path

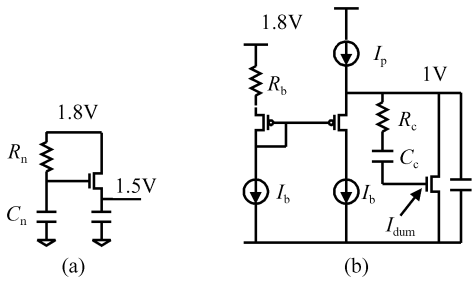

Fig. 7　Regulators　(a) Active filter; (b) Shunt regulator

current injected by the proportional charge pump (I_{cpp}). The current gain (K_{mir}) helps reduce the current switched in the charge pump, increase its speed, and reduce the clock feedthrough and channel charge injection effects. The current mirror is pre-biased with a low value current (I_{pre}) to minimize its turn-on delay, which would significantly degrade the phase margin of the PLL[1].

3.5　Power supply partitioning

Power supply partitioning and distribution are critical for the jitter performance of a PLL. A single 1.8V supply is used for the entire PLL to reduce the number of the package pins in this design, so the situation is even worse. We choose an active low pass filter, shown in Fig. 7(a), whose drop-out is about 0.3V to reject high frequency supply noise for the analog blocks that have enough voltage headroom, such as current DAC, current bandgap reference, and loop filter. The charge pump uses a simple passive RC filter, shown in Fig. 4(b), to maximize its output range, which will help lower the VCO gain. The digital blocks (PFD, divider, clock buffers) are supplied by a high reverse-PSRR shunt regulator[9], as shown in Fig. 7(b). The shunt regulator provides a 1V supply for the digital blocks and keeps constant current from the 1.8V supply to ground. This will minimize the dI/dT noise coupled to the noise sensitive analog blocks.

4　Measurement results

The PLL is fabricated in a 65nm standard digital CMOS process. The photograph of the test chip is shown in Fig. 8. The PLL is measured using Agilent's DSA 80000 oscilloscope. The waveform of the output clock at 1.6GHz is shown in Fig. 9. Measured under room temperature, the RMS jitter is 3.1ps when running at 1.6GHz, and the peak-to-peak jitter is 18.4ps in 10000 hits. The RMS jitters measured with different supply voltages and temperatures are shown in Table 2. The table shows that the proposed PLL achieves stable jitter performance over the PVT variations. The increase of jitter with temperature is mainly due to the thermal noise rising with temperature. It consumes only 0.94mA (excluding the output buffer for measurement) when running at 1.6GHz. The comparisons of this PLL with previous works in terms of jitter, power consumption, and area are summarized in Table 3.

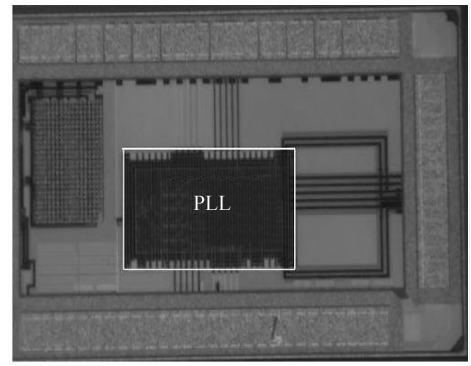

Fig. 8　Photograph of the test chip

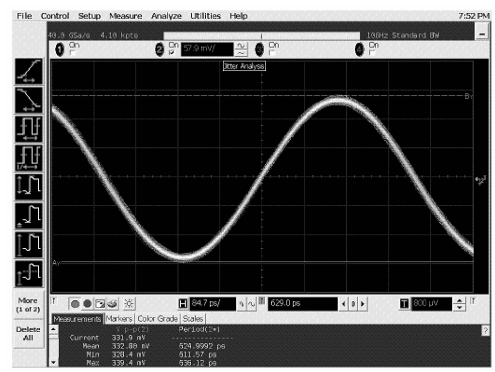

Fig. 9　Waveform of the clock

Table 2　RMS jitters under different supply voltages and temperatures

	V_{DD} = 1.6V	V_{DD} = 1.8V	V_{DD} = 2V
26℃	3.2ps	3.1ps	3.1ps
45℃	3.3ps	3.2ps	3.2ps
82℃	3.6ps	3.5ps	3.5ps

Table 3　Comparisons of this PLL with previous work

	Frequency	Jitter	Power	Area	Technology
This work	1.6GHz	3.1ps RMS 18.4ps p2p	0.94mA	0.04mm^2	65nm CMOS
Ref.[4]	520MHz	<77ps p2p	1.7mA	0.18mm^2	90nm CMOS
Ref.[10]	3.125GHz	1.3ps RMS	15mW	0.064mm^2	130nm CMOS
Ref.[11]	1.25GHz	1.2ps RMS	3mA	0.015mm^2	130nm CMOS
Ref.[12]	1GHz	12.8ps RMS	22mW	0.36 mm^2	0.35μm CMOS
Ref.[13]	1244MHz	6.1ps RMS	12mW	0.22mm^2	0.25μm CMOS

5　Conclusion

A PVT tolerant sub-mA PLL for high speed links is presented in this paper. A novel open-loop calibration is proposed to mitigate the impact of PVT variation. A dual-loop architecture is adopted to achieve

process independent loop characteristics such as damping factor and pole-zero separation. A new phase frequency detector embedded with the level shifter is introduced.

The test chip has been fabricated in a 65nm standard digital CMOS process, and good jitter is achieved with very low power consumption. To our knowledge, this is the first PLL designed with 65nm technology reported in the domestic literature.

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一个用于高速信号传输的对 PVT 变化不敏感的低功耗锁相环*

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摘要： 介绍了一个用于高速信号传输的低功耗锁相环. 提出了一种新的开环校准方法. 该校准通过上电时候进行的开环数字校准很大程度上减轻了工艺变化对电路的影响，相比以前的闭环校准方法，该方法可以显著缩短校准时间. 在这个锁相环中采用了双环路的结构来获得对工艺、温度和环境变化不敏感的环路参数：例如衰减因子、相位裕度等. 还设计了一种新的鉴频鉴相器，它内嵌了电平转换的功能，简化了电路. 该 PLL 的设计通过小心的供电网络划分来降低电源噪声的耦合. 设计的锁相环路在输出为 1.6GHz 的时候均方根抖动为 3.1ps，而仅消耗约为 1mA 的电流.

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