Degradation of nMOS and pMOSFETs with Ultrathin Gate Oxide Under DT Stress*

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Abstract: The degradation of device parameters and the degradation of the stress induced leakage current (SILC) of thin tunnel gate oxide under constant direct-tunneling voltage stress are studied using nMOS and pMOSFETs with 1.4nm gate oxides. Experimental results show that there is a linear correlation between the degradation of the SILC and the degradation of V_{th} in MOSFETs during different direct-tunneling (DT) stresses. A model of tunneling assisted by interface traps and oxide trapped positive charges is developed to explain the origin of SILC during DT stress.

Key words: threshold voltage; interface traps; direct tunneling; SILC
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1 Introduction

Aggressive shrinking of MOSFETs causes direct-tunneling (DT) gate leakage to become significant in transistor operation, and thus spurs investigation into DT phenomena through gate insulators. In the thin gate oxide regime, direct tunneling current increases exponentially as oxide thickness decreases, which is of primary concern for CMOS scaling[1~5]. Some models have been presented to investigate the theory of direct tunneling. However, few studies have concentrated on the degradation of devices under DT stress.

The stress induced leakage current (SILC), namely the excess low field current across a thin gate oxide after a high electric field stress, is a major concern for long-term reliability and the scaling of the tunnel oxide in nonvolatile memories[6~11]. SILC plays an important role in the reliability of devices. The SILC has been also indicated as a precursor of catastrophic breakdown[12~15]. For these reasons, the investigation of SILC is of primary importance for oxide degradation. Although a consensus has been reached in understanding the conduction mechanism of SILC in relatively thick samples (>4nm), the low voltage SILC generation mechanism in ultrathin (<3nm) oxide films is still not clearly understood[16~18]. Therefore, further study is necessary to investigate the origin of SILC during DT stress.

In this work, we present experimental results of MOSFETs reliability with ultrathin oxide (1.4nm). The current through the oxide under direct tunneling stress degrades the quality of the oxide, causing drift in the threshold voltage (V_{th}), a reduction of saturation drain current (I_{dsat}), and an increase of stress-induced oxide leakage current. It is found experimentally that there is a linear correlation between the degradation of the stress induced leakage current and the degradation of V_{th} in MOSFETs during different DT stresses. We develop a model of tunneling assisted by interface traps and oxide trapped positive charges to explain the origin of SILC during DT stress.

2 Devices and experiments

The MOSFETs used here were fabricated using 90nm process technology with a lightly doped drain (LDD) structure and a shallow trench isolation (STI) scheme. The MOSFETs have a channel length of 40μm, a width of 10μm, and a gate oxide thickness of 1.4nm. The gate oxides of all devices were annealed in N_2O gas ambient after thermal growth. The operation voltage is 1.0V for the MOSFETs. An Agilent B1500A high-precision semiconductor parameter analyzer was used to conduct the tests.

Constant voltage stress and *I-V* measurements were performed with an Agilent B1500A semiconductor parameter analyzer. Both positive gate bias DT (+DT) stress and negative gate bias DT (−DT) stress were performed on MOSFETs. For both the nMOSFET and pMOSFET, the +DT stress was per-

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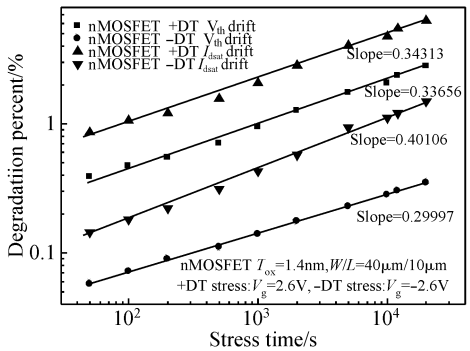

Fig. 1　Time dependence of degradation of device parameters in nMOSFET under positive and negative gate bias DT stress

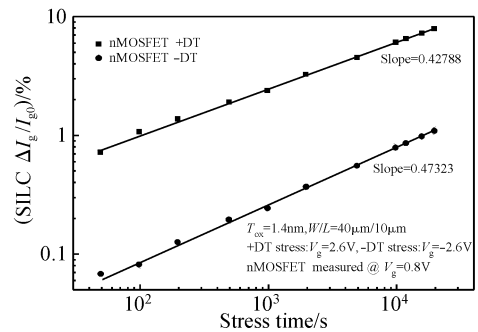

Fig. 3　Time evolution of SILC under direct tunneling stress on the nMOSFET

formed at V_{gs} = +2.6V and the −DT stress was performed at V_{gs} = −2.6V. Stress was interrupted at regular intervals and device parameters were measured. The SILCs were characterized by measuring the *I-t* (gate current-stress time) characteristics at constant, low, pre-tunneling voltages at regular intervals. The SILC was measured at V_g = 0.8V during DT stress for the nMOSFET and measured at V_g = −0.8V during DT stress for the pMOSFET. All experiments were performed at room temperature.

3　Results and discussion

First, we study the degradation of device parameters including V_{th} and I_{dsat} under constant direct-tunneling voltage stress in MOSFETs. Figures 1 and 2 show the time dependence of the degradation of device parameters in nMOSFETs and pMOSFETs, respectively. V_{th} in the nMOSFET increases towards the positive direction and I_{dsat} in the nMOSFET decreases. V_{th} in the pMOSFET increases towards the negative direction and the absolute value of I_{dsat} in the pMOSFET decreases. The degradation of device parameters during +DT stress is more serious than that of during −DT stress for the nMOSFET, and the degradation of device parameters during −DT stress is more serious than that of during +DT stress for the pMOSFET. It is also evident that the degradation of I_{dsat} is more serious than that of V_{th} during both DT stresses for the nMOSFET, but the degradation of V_{th} is more serious than that of I_{dsat} during both DT stresses for the pMOSFET.

Second, the SILC of ultrathin gate oxide is also investigated. Figures 3 and 4 show the time evolution of SILC under direct tunneling stresses on the nMOSFET and pMOSFET, respectively. SILC in the nMOSFET increases towards the positive direction and SILC in the pMOSFET increases towards the negative direction. The relationship between SILC and stress time under different stresses shows perfect linearity in the log-log scale, as shown in Figs. 3 and 4. The SILC increases with the stress time under four different tunneling stresses. The degradation of SILC measured at V_g = 0.8V during +DT stress is more serious than that of during −DT stress for the nMOSFET, and the degradation of SILC measured at V_g = −0.8V during −DT stress is more serious than that of during +DT stress for the pMOSFET. The SILC result is consistent with the result of the degradation of device parameters.

In our experiments, there is a good linear correlation between the degradation of SILC and the degradation of V_{th} in MOSFETs during different DT stresses, as shown in Fig. 5. This result is deserved to be paid

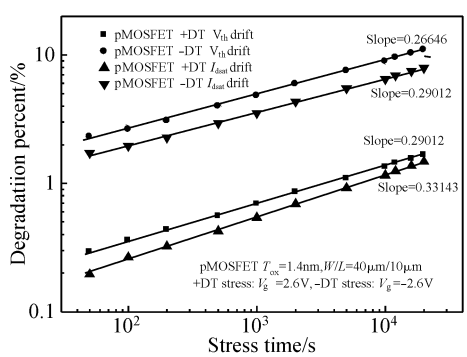

Fig. 2　Time dependence of degradation of device parameters in pMOSFET under positive and negative gate bias DT stress

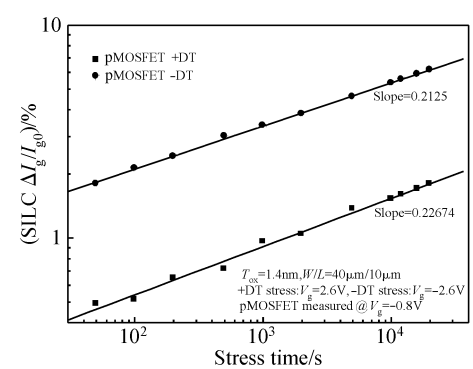

Fig. 4　Time evolution of SILC under direct tunneling stress on the pMOSFET

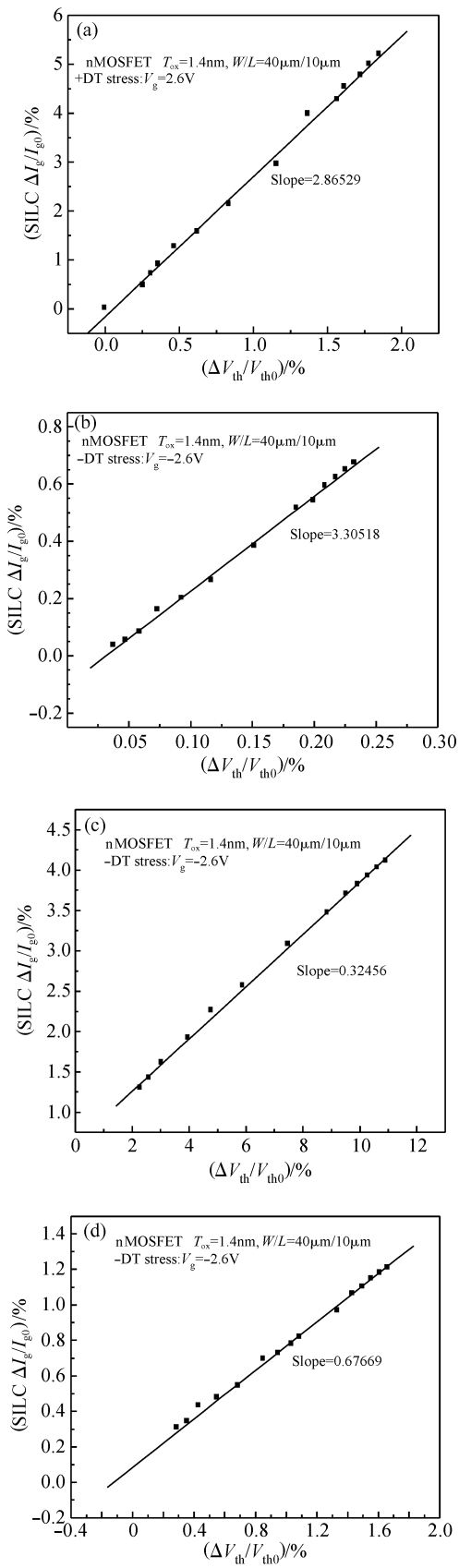

Fig. 5 SILC (measured at $V_g = 0.8$V for the nMOSFET and measured at $V_g = -0.8$V for the pMOSFET) variations versus V_{th} variations under different DT stresses for MOSFETs

attention to. Through a good analysis of the result, we can investigate the origin of SILC in MOSFETs during DT stress.

For a good understanding of the experimental results, it is necessary to clearify the process of the motion of carriers under various constant direct-tunneling voltage stresses in the MOSFETs. Figure 6 shows the energy band diagrams of the MOS structure under the four stress conditions. The energy band diagram for the nMOSFET under + DT stress is presented in Fig. 6 (a). Electrons directly tunneling from the inverted channel are dominant during + DT stress in the nMOSFET. A fraction of the injected electrons arriving at the anode (the polysilicon gate) lose their energy by creating electron-hole pairs in the valence band of the polysilicon gate via impact ionization. These holes tunnel back into the oxide layer and are transported towards the cathode. Some of the injected holes get trapped near the gate/oxide interface and become a part of the oxide trapped charges.

The energy band diagram for the nMOSFET under − DT stress is shown in Fig. 6 (b). Electrons are first injected from the gate into the conduction band of SiO_2 due to direct tunneling. Since the electric field is very high, the injected electrons will gain kinetic energy from the oxide field and will lose energy by phonon scattering. The energetic electrons will arrive at the silicon substrate and will produce electron-hole pairs via the interband impact mechanism. The holes generated with enough energy will tunnel back into the oxide layer. A small fraction of these holes are trapped near the Si-SiO_2 interface and become a part of the oxide trapped charges. When stress was interrupted at regular intervals, device parameters were measured. The measurement setup is the same. V_{th} is one of the most important parameters, and here we mainly focus on the degradation of V_{th}. V_{th} in an nMOSFET can be expressed as

$$V_{th} = 2\phi_F + \frac{\sqrt{2qK_s\varepsilon_0 N_A(2\phi_F)}}{C_{ox}} + \phi_{MS} - \frac{\lambda Q_{ox}}{C_{ox}} - \frac{Q_{it}(\phi_s = 2\phi_F)}{C_{ox}} \quad (1)$$

where ϕ_F is the Fermi potential, q the electron charge, K_s the silicon dielectric constant, ε_0 the permittivity of free space, N_A the acceptor doping concentration, C_{ox} the oxide capacitance, ϕ_{MS} the metal-semiconductor work function difference, and λ the charge distribution factor[19]. Here, Q_{ox} is defined as the trapped-oxide sheet charge density, which includes all charge components that are not sensitive to the silicon surface potential such as the trapped-oxide charge and the fixed oxide charge, λ is the charge distribution factor and Q_{it} is the interface trapped charge density at the Si/SiO_2 interface, which depends on the surface potential ϕ_s. The shift of V_{th} can be

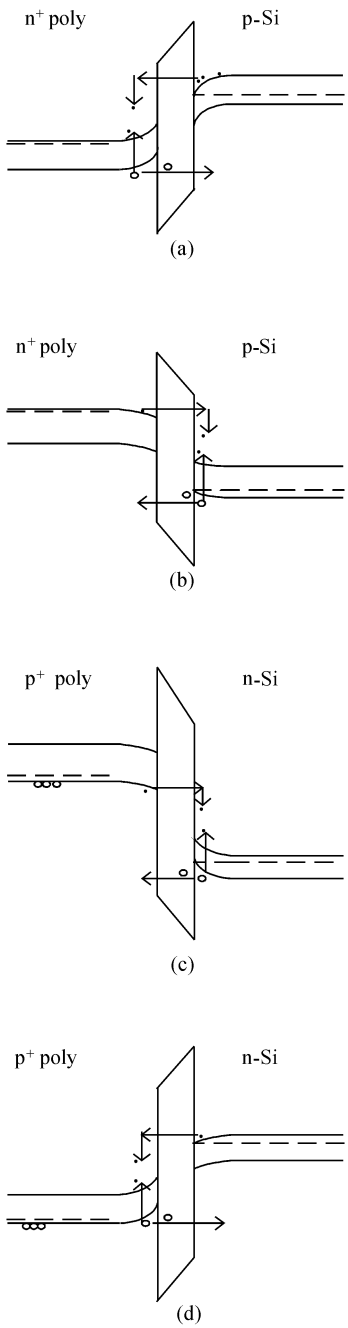

Fig. 6　Energy band diagrams of the MOS structure under different stress conditions　(a) + DT stress for the nMOSFET; (b) − DT stress for the nMOSFET; (c) − DT stress for the pMOSFET; (d) + DT stress for the pMOSFET

caused by the increase of the trapped-oxide charges and interface traps. For the nMOSFET under DT, interface traps are charged negatively during the measurement, and the trapped-oxide charges are positive. Interface traps make V_{th} drift positively, but the trapped-oxide charge makes V_{th} drift negatively. The trapped-oxide charges and interface traps in the nMOSFET during DT stress play different roles in the degradation of V_{th}. When the injected holes get trapped near the gate/oxide interface, λ is very small and is almost 0. When the injected holes get trapped near the Si/SiO_2 interface, λ is large and is almost 1. So the holes trapped near the Si/SiO_2 interface are more effective than the holes trapped near the gate/oxide interface. In addition, the difference between − DT and + DT stresses is that the impact-ionization generated electron-hole pairs will occur at the Si/SiO_2 interface in the case of − DT stress and will play an important role in the generation of interface traps, whereas the electron-hole pairs generated in the + DT stress will be generated in the heavily-doped polysilicon and quickly recombine. Figure 1 shows that the degradation of V_{th} during + DT stress is more serious than that of during − DT stress for the nMOSFET. Thus, the increase of holes trapped near the Si/SiO_2 interface can shield a part of the increase of interface traps at the Si/SiO_2 interface during − DT stress for the nMOSFET.

The energy band diagram for the pMOSFET under − DT stress is presented in Fig. 6(c). The valence electrons tunnel from the p^+ polysilicon gate into the inverted p type channel of the substrate. A fraction of the injected electrons will lose their energy when arriving at the anode by creating electron-hole pairs via impact ionization. These holes tunnel back into the oxide layer and are transported towards the cathode. Some of the injected holes get trapped near the Si/SiO_2 interface and become a part of oxide trapped charges.

The energy band diagram for the pMOSFET under + DT stress is shown in Fig. 6 (d). The electrons tunnel from the accumulated substrate Si layer into the p^+ polysilicon gate. A fraction of the injected electrons will lose their energy when arriving at the anode by creating electron-hole pairs via impact ionization. These holes tunnel back into the oxide layer and are transported towards the cathode. Some of the injected holes get trapped near the gate/oxide interface and become a part of the oxide trapped charges. The shift of V_{th} is caused by the increase of trapped-oxide charges and interface traps in the pMOSFET. For the pMOSFET, interface traps are charged positively during the measurement, and the trapped-oxide charges are positive. Interface traps make V_{th} drift negatively and the trapped-oxide charges also make V_{th} drift negatively. The holes trapped near the Si/SiO_2 interface play a more important role than the holes trapped near the gate/oxide interface. The impact-ionization generated electron-hole pairs will occur at the Si/SiO_2 interface in the case of − DT stress and play an important role in the generation of interface traps. This experimental result shows that the degradation of device parameters during − DT stress is more serious than that of during + DT stress for the

pMOSFET, as shown in Fig. 2.

The origin of SILC has been examined many times[20~26]. Some models have been presented to investigate the SILC, among which the trap assisted tunneling model, the thermal assisted tunneling model, and the resonant tunneling model are the most popular. However, no complete agreement has been reached and it is not easy to analyze the SILC in ultrathin 1.4nm thick oxide using these models. SILC is measured by interrupting stress at regular intervals. There is a good linear correlation between the degradation of SILC and the degradation of V_{th} in MOSFETs during different DT stresses, as shown in Fig. 5. Because the shift of threshold voltage results from the generation of interface traps and oxide trapped positive charges, there should be some connection between the degradation of gate leakage current and their generation. We develop a model with interface traps and oxide trapped positive charges to explain the SILC here.

The model with interface traps and oxide trapped positive charges assisting tunneling are schematically shown in Fig. 7. For nMOSFETs, the SILC is measured at $V_g = 0.8$V after DT stress. When the measurement voltage is applied, there are interface traps and oxide trapped positive charges generated. Because the gate voltage is much larger than 0V, as shown in Figs. 7 (a) and 7(b), the p-Si conduction band is higher than the n^+-polysilicon valence band. Electrons can emit from the inverted channel. The energy band diagram for the measurement of SILC in the nMOSFET under + DT stress is drawn in Fig. 7 (a). Interface traps at the Si/SiO_2 interface can serve as a stepping stone because they effectively capture the electrons from the inverted channel and then immediately emit them. Meanwhile, the oxide trapped positive charges near the gate/oxide interface help electrons to tunnel through the oxide by causing a barrier height lowering and enhancing the electric field in the oxide. The energy band diagram for the measurement of SILC in the nMOSFET under − DT stress is presented in Fig. 7 (b). The oxide trapped positive charges are near the Si/SiO_2 interface. Interface traps and oxide trapped positive charges play the same role in Figs. 7 (a) and 7(b).

For pMOSFETs, the SILC is measured at $V_g = -0.8$V after DT stress. When the measurement voltage is applied, there are also interface traps and oxide trapped positive charges that have been generated. Because the gate voltage is much smaller than 0V, as shown in Figs. 7(c) and 7(d), the p^+-polysilicon valence band is higher than the n-Si conduction band. Electrons can emit from the p^+-polysilicon valence band. The energy band diagram for the measurement of SILC in the pMOSFET under − DT stress is drawn in Fig. 7(c). The oxide trapped positive charges near the Si/SiO_2 interface help electrons to tunnel through the oxide by causing a barrier height lowering and en-

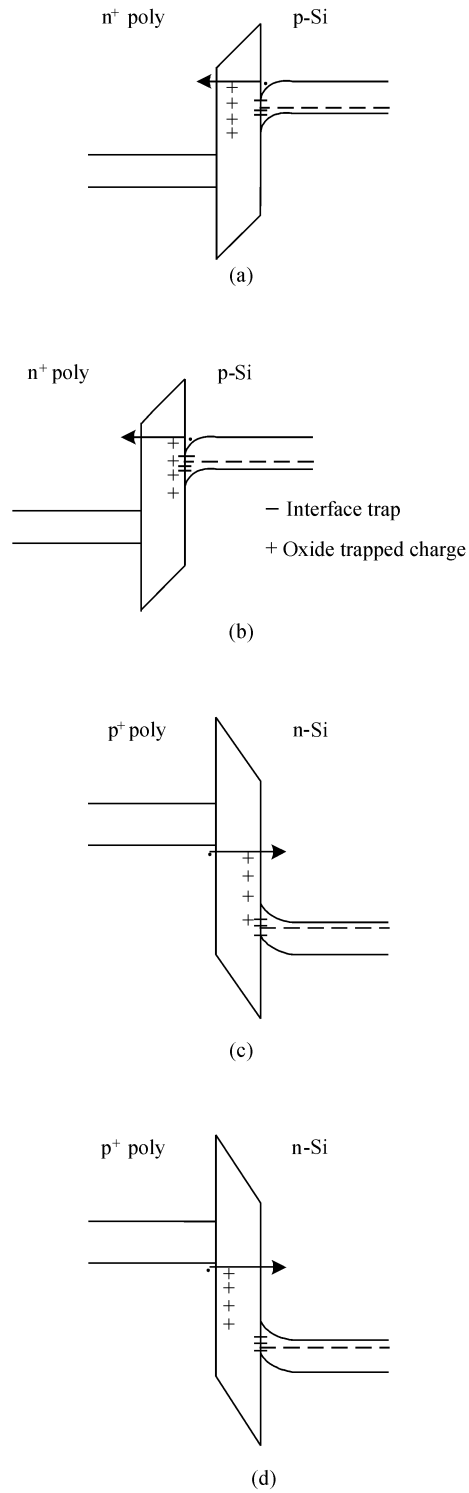

Fig. 7 Schematics of the model with interface traps and oxide trapped charges assisting tunneling during the measurement of SILC (a) Under + DT stress for the nMOSFET; (b) Under − DT stress for the nMOSFET; (c) Under − DT stress for the pMOSFET; (d) Under + DT stress for the pMOSFET

hancing the electric field in the oxide. Interface traps at Si/SiO_2 interface can serve as a stepping stone. They can effectively capture the electrons from the p^+-polysilicon valence band and then immediately emit them toward the substrate. The energy band diagram for the measurement of SILC in pMOSFET under +DT stress is shown in Fig. 7 (d). The oxide trapped positive charges are near the gate/oxide interface. Interface traps and oxide trapped positive charges play the same role in Figs. 7(c) and 7(d). In this model, the interface traps and oxide trapped positive charges during DT stress play an important role in the degradation of the SILC.

4 Conclusion

In this paper, the degradation of devices has been investigated in detail under a variety of DT stress conditions. First, the degradation of device parameters, including V_{th} and I_{dsat}, under constant direct-tunneling voltage stress in MOSFETs was presented. Second, the SILC of ultrathin gate oxide was also investigated and it was found that there is a linear correlation between the degradation of SILC and the degradation of V_{th} in MOSFETs during different DT stresses. By analyzing the process of motion of carriers under various constant direct-tunneling voltage stresses in the MOSFETs, it is confirmed that the degradation of V_{th} and the degradation of SILC are interrelated due to the generation of interface traps and trapped holes during DT stresses. We developed a model of tunneling assisted by interface traps and oxide trapped positive charges to explain the origin of SILC during DT stresses.

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直接隧穿应力下超薄栅氧 MOS 器件退化*

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摘要：研究了栅氧厚度为 1.4nm MOS 器件在恒压直接隧穿应力下器件参数退化和应力感应漏电流退化.实验结果表明,在不同直接隧穿应力过程中,应力感应漏电流(SILC)的退化和 V_{th}的退化均存在线性关系.为了解释直接隧穿应力下 SILC 的起因,建立了一个界面陷阱和氧化层陷阱正电荷共同辅助遂穿模型.

关键词：阈值电压；界面陷阱；直接隧穿；应力感应漏电流

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