Benchmark tests on symmetry and continuity characteristics between BSIM4 and ULTRA-BULK*

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Abstract: This paper presents the benchmark test results on the symmetry and continuity characteristics between BSIM4 from Berkeley and ULTRA-BULK from Peking University. It is shown that the industry standard model BSIM4 has a series of the shortcomings of the continuity and symmetry, such as the charge, high-order current derivatives, and the trans-capacitances while the latest advanced surface-potential based MOSFET compact model, ULTRA-BULK, demonstrates all necessary continuity and symmetry characteristics, which are very important for analog and RF circuit design.

Key words: compact model; BSIM4; ULTRA-BULK; circuit design; continuity; symmetry

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1. Introduction

Compact models bridge the gap between circuit design and process fabrication, playing an important role in the development of the CMOS-based IC industry. The BSIM series of compact MOSFET models are the industry standards which are successfully used throughout the semiconductor industry and the research community for digital and analog circuit design. Most of the traditional MOSFET compact models, however, have drawbacks stemming from simplifying assumptions made during their development. These drawbacks limit the accuracy of these models in specific operation regions of devices such as analog circuit and RF circuit simulation. For example, BSIM3v3, MM9, and PCIM have discontinuities in the derivatives of the drain current and terminal charges at the boundary between forward and reverse mode operation[1−6]. Another problem of these models is the incorrect capacitance versus bias behavior, such as unequal C_{gd} and C_{gs} values at $V_{ds} = 0$. Although the technical experts consider BSIM4 to be an excellent model for 90 nm node and beyond, the drawbacks on its continuity and symmetry will lead to problems in analog applications. The same case exists even at 180 and 130 nm. The threshold voltage based concept of both BSIM3 and BSIM4 is generally considered to be the primary cause.

Due to the identified drawbacks of these threshold voltage based models mentioned above, advanced compact models are developed based on the surface potential approach, charge approach and BSIM model enhancement[7−12]. Among them, the surface potential based models are generally believed to be the physics based model that retains the essential basic physics of a MOSFET and gives continuous representation of device characteristics for all regions. Meanwhile, it is easier to implement gate leakage current and quantum mechanical effects (QME) into these models, both of which are becoming more and more critical with the trend of scaling down. The surface potential based models are established on the physical characteristics of CMOS, using less number of parameters compared with other models, thus, the considerable attention in recent years has been focused on developing such a kind of the surface-potential-based models[13].

The ULTRA-BULK is developed in the Nano- & Tera-Device and Circuit group of Peking University of China to overcome drawbacks of the traditional threshold voltage based models and aiming at fulfilling the following features: the first-principle derivation of the complete MOSFET surface potential equation[14,15]; physics based analytic solution of the surface potential equation[16]; accurate description of physics based channel current equation and calculation[17]; and self-consistent modeling of short-channel effects to ensure the high accuracy parameter extraction[18]. The latest model predictions have also been verified by the numerical analysis and the wide experiment data, proving the ULTRA-BULK validity[17]. This paper presents the test results on the symmetry and continuity characteristics between the latest improved BSIM model, BSIM4, from Berkeley and ULTRA-BULK from Peking University. It is shown that the industry standard model BSIM4 has a series of the shortcomings of the continuity and symmetry, such as the charge, high-order current derivatives and the trans-capacitances while the latest advanced surface-potential based MOSFET compact model,

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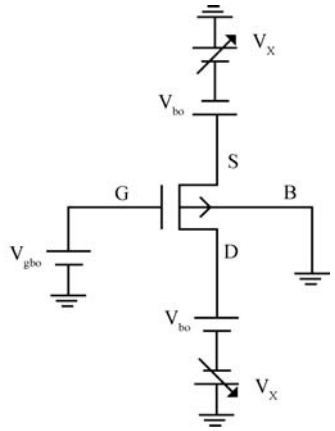

Fig. 1. Circuit used in the Gummel symmetry tests.

ULTRA-BULK, demonstrates all necessary continuity and symmetry characteristics, which are very important for analog and RF circuit design.

2. Comparison between BSIM4 and ULTRA-BULK

The BSIM4 is the successor of the BSIM3; both have been widely used in the present international semiconductor industry. Compared with BSIM3, the advantages of the BSIM4 includes: more accurate short/narrow channel effect model; multiple current saturation mechanisms; quantum mechanic effective gate oxide thickness model; gate dielectric tunneling current model; enhanced RF model including unified flicker noise model, holistic thermal noise model and parasitical component model; scalable stress effect model, etc. The BSIM4 model, however, also demonstrates a series of drawbacks due to the $V_{\rm th}$ based model characteristics, such as too many parameters, negative capacitance and conductance in some cases. The serious problems of BSM4 are the discontinuities in derivatives of the drain current and terminal charges at the boundary between forward ($V_{\rm ds} > 0$) and reverse ($V_{\rm ds} < 0$) mode operation, which cannot predict RF circuit performance correctly. Besides mere digital circuits, since CMOS is playing a more and more important role in RF and analog circuits, it is crucial for the international semiconductor industry to have an independent compact model to predict the transistor performance in all conditions (including RF and analog circuits). In order to overcome the shortcomings of the BSIM4 and other models, new generation surface potential based model, ULTRA-BULK has been developed. As a result of the physical essence of ULTRA-BULK, it can provide accurate results for the whole operation region from DC to over 50 GHz. So far, there have no evident shortcomings of the ULTRA-BULK model to be found although it needs more tests and applications to further calibrate.

For the crucial importance of symmetry and continuity characteristics to the convergence in simulation and analysis of RF and analog circuits, our attentions are focused to these characteristics and the tests are based on them. The results of Gummel symmetry tests on BSIM4 and ULTRA-BULK are

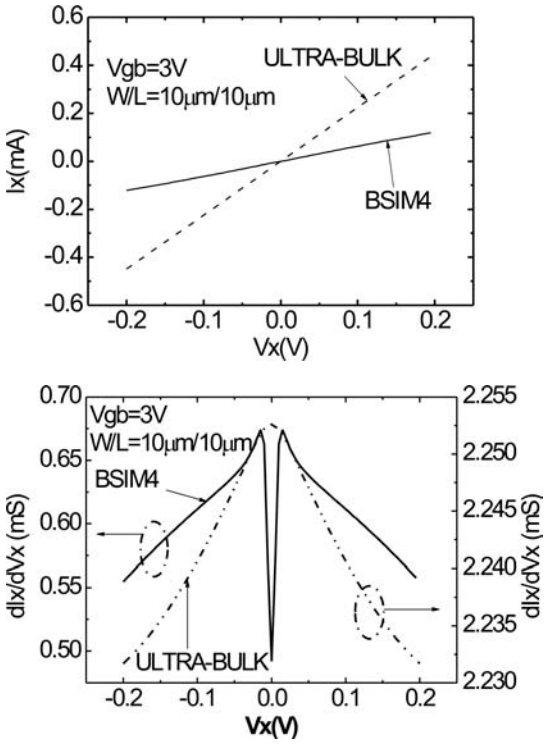

Fig. 2. Plots of $I_{\rm x}$ and $\mathrm{d}I_{\rm x}/\mathrm{d}V_{\rm x}$ versus $V_{\rm x}$.

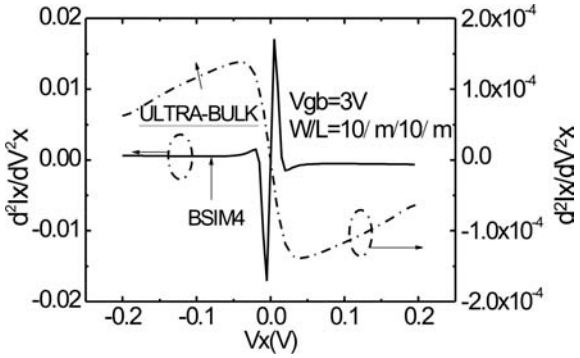

Fig. 3. Plots of $\mathrm{d}^2I_{\rm x}/\mathrm{d}V_{\rm x}^2$ versus $V_{\rm x}$.

demonstrated in this paper. The circuit used in Gummel symmetry tests is shown in Fig. 1. It is evident that for uniform doped MOSFET the drain current $I_{\rm d}$ should be an odd function of $V_{\rm x}$ which is

$$I_{\rm d}(V_{\rm x}) = -I_{\rm d}(-V_{\rm x}). \tag{1}$$

So we can get

$$I_{\rm x}(V_{\rm x}) = 0.5(I_{\rm d}(V_{\rm x}) - I_{\rm s}(V_{\rm x})). \tag{2}$$

Furthermore, if a MOSFET is continuous around $V_{\rm ds} = 0$, $I_{\rm d}$ and its derivatives with respect to $V_{\rm x}$ should be continuous and its second derivative with respect to $V_{\rm x}$ should be 0 at $V_{\rm x} = 0$.

Figures 2 and 3 demonstrate the simulated variation of $I_{\rm x}$, $\mathrm{d}I_{\rm x}/\mathrm{d}V_{\rm x}$ and $\mathrm{d}^2I_{\rm x}/\mathrm{d}V_{\rm x}^2$ versus $V_{\rm x}$. It is easy to see that $I_{\rm x}$ versus $V_{\rm x}$ of BSIM4 and ULTRA-BULK are both symmetric and continuous around $V_{\rm x} = 0$. But the first derivative and second-order derivative of $I_{\rm x}$ of BSIM4 with respect to $V_{\rm x}$ are

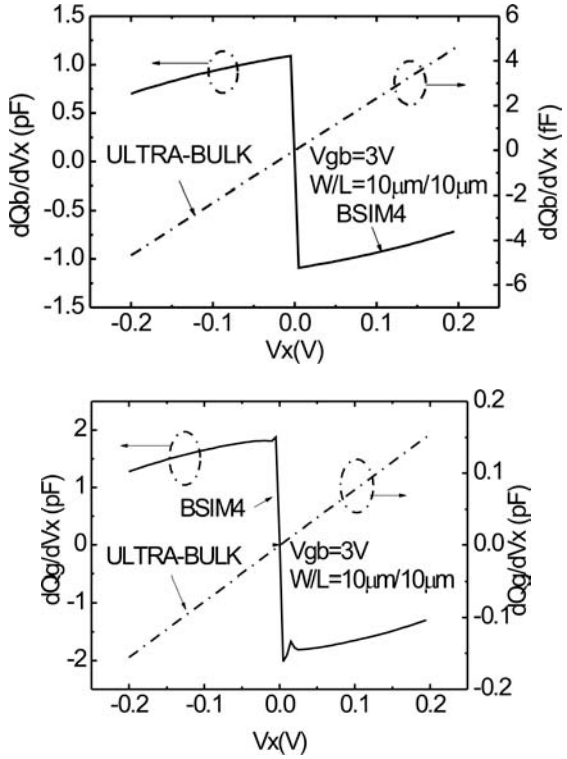

Fig. 4. Plots of the derivative of Q_g and Q_b versus V_x.

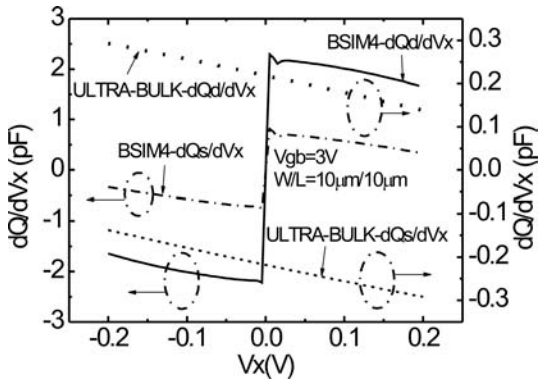

Fig. 5. Plots of derivative of Q_d and Q_s versus V_x.

discontinuous at $V_x = 0$. In contrast, ULTRA-BULK model shows a perfect symmetry of both dI_x/dV_x and d^2I_x/dV_x^2 around $V_x = 0$.

In addition to the current behavior, we can get the terminal charge behavior by using the circuit in Fig. 1. We also sweep V_x from a negative value to an equal positive value to simulate the gate, source, drain and bulk charges of the MOSFET (Q_g, Q_s, Q_d, and Q_b), respectively. We make the derivatives of charges versus V_x plotted and we can see the charge behavior in the plots. If a model is continuous around $V_x = 0$, the derivatives of charges should pass smoothly through $V_x = 0$ and have no discontinuities. Furthermore, the derivatives of Q_s and Q_d should be equal and opposite at $V_x = 0$ because the device is assumed to be symmetric. Figures 4 and 5 demonstrate the charge behavior comparison. It is obvious that the derivative of the gate, source, drain and bulk charges versus V_x are discontinuous around $V_x = 0$ in BSIM4. But all the plots of ULTRA-BULK show no discontinuity around $V_x = 0$.

Another problem of BSIM4 lies in the capacitance

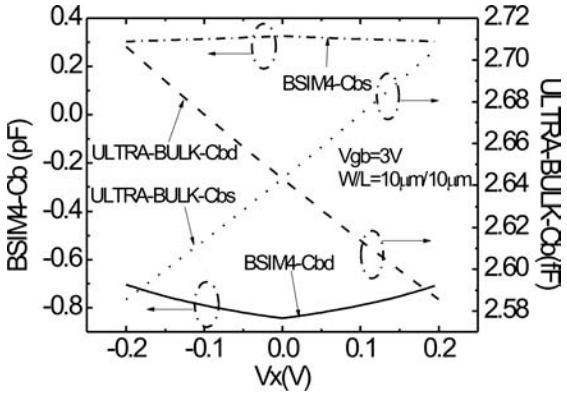

Fig. 6. Plots of capacitances (C_{bd} and C_{bs}) versus V_x.

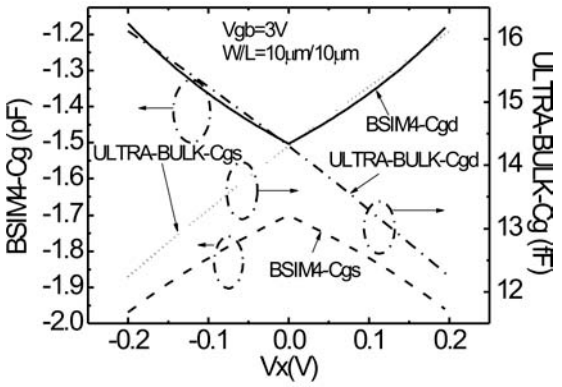

Fig. 7. Plots of capacitances (C_{gd} and C_{gs}) versus V_x.

model. An ideal symmetric device should be symmetric, the capacitance C_{gs} and C_{gd} should have be equal at $V_x = 0$ as well as C_{bs} and C_{bd}, C_{dd} and C_{ss}, respectively. The asymmetry in capacitance model may induce the nonconservation of charge and energy, resulting in the nonconvergence and the abortion of circuit simulation. Figures 6 and 7 demonstrate the comparison of the capacitance behavior between BSIM4 and ULTRA-BULK. It is evident that capacitances (C_{gd} and C_{gs}, C_{bd} and C_{bs}, C_{dd} and C_{ss}) versus V_x of BSIM4 are not equal at $V_x = 0$, respectively. But the capacitances in Figs. 6 and 7 are equal at $V_x = 0$ in ULTRA-BULK ($C_{gd} = C_{gs}$, $C_{bd} = C_{bs}$, $C_{dd} = C_{ss}$).

Furthermore, the capacitance behavior can be seen from Fig. 8 in another way. Here, capacitances (C_{gd} and C_{gs}, C_{bd} and C_{bs}, C_{dd} and C_{ss}) versus V_{gb} of BSIM4 are not equal where V_{ds} is fixed to 0, but those of ULTRA-BULK are equal. So we can see the errors of capacitances in the model of BSIM4 and the advantages of ULTRA-BULK.

3. Conclusion

The newly developed model ULTRA-BULK in Peking University avoids using the specific assumptions in the threshold voltage based models, thus, it is a more accurate CMOS model to predict CMOS characteristics in physics, especially at the condition that the source and drain operate at the zero bias or that the gate bias is around the threshold. The comparison of symmetry and continuity tests between BSIM4 and ULTRA-BULK has been presented. Through the Gummel

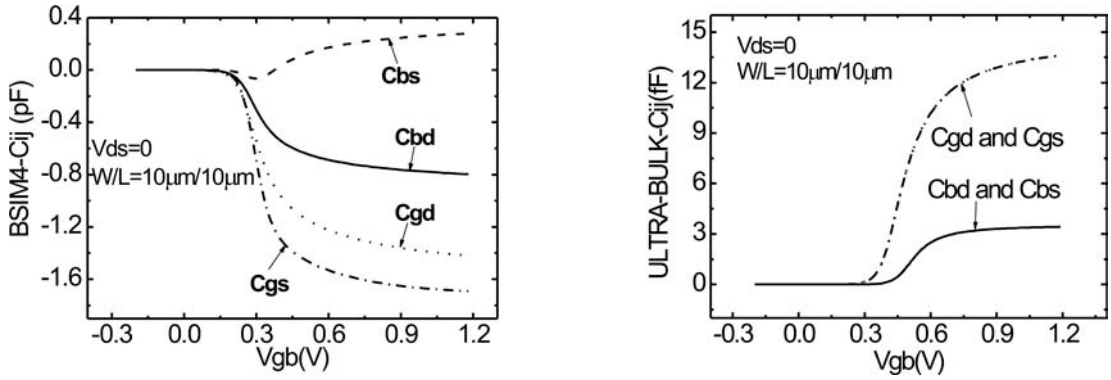

Fig. 8. Plots of capacitances behavior versus V_{gb} of BSIM4 and ULTRA-BULK.

symmetry tests, the typical terminal currents and charges of MOSFET are obtained, which enable us to discuss the distribution of the currents and charges between the two models. The results show that the current, charge and capacitance behaviors of the new model ULTRA-BULK have not any drawbacks and flaws that BSIM4 and other published models have. This surface potential based model gives consistent I–V and C–V models and shows good continuous and symmetric characteristics. Therefore, ULTRA-BULK can predict and model the typical RF and analog circuits effectively, such as R2R, MRC, VARACTOR, etc.

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