An Integrated Power Management Unit for a Battery-Operated Wireless Endoscopic System*

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Abstract: This paper presents an integrated power management unit (PMU) for a battery-operated wireless endoscopic system. This PMU is integrated with a baseband chip in standard 0.18μm CMOS technology, promising low cost, ease in PCB design, and a minimum in system size. The optimized power supply architecture is derived from comparison. Circuits of sub blocks are presented in detail. As a result, only five small off-chip capacitances are required by PMU with an overall quiet current consumption of less than 100μA. Moreover, a digital calibration method is adopted to alleviate the effect of process variation. The achieved performance is also demonstrated with corresponding measurement results.

Key words: power management unit; LDO; charge pump; oscillator; integration; wireless endoscopic system
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1 Introduction

Recently, the advance of CMOS technology has made battery-operated wireless endoscopic capsule systems[1] available to diagnose the whole small intestine. More research has been performed in this field. As a classical battery-operated wireless sensor node, it is composed of image sensors, a signal processing unit, an RF transceiver, and a power management unit (PMU). This PMU is often fabricated as a separate chip, which has adverse impact on PCB area and the miniature size of the system. In order to save cost and minimize the size, this paper presents a PMU integrated into the baseband chip. The approach of an integrated PMU allows one to achieve optimum overall chip and system cost and size. The PMU has been fabricated with the same technology as the baseband chip.

2 Architecture overview

The integrated PMU has to not only supply on-chip functional blocks but also deliver the power for additional components connected to the chip, e. g., CMOS image sensor, RF transceiver, and LEDs for illumination. The miniature size requirement of the wireless endoscopic system makes very severe demands on the area of PCB board and the number of off-chip components inside the capsule. An overall system architecture that can reduce the on-board components is explored by considering not only chip architecture but also the capsule architecture. The block diagram of the baseband chip with integrated PMU is shown in Fig. 1. The presented chip is based on the architecture as described in Ref. [2]. Several design issues have to be considered for integrating the PMU functionality: (1) The realization of PMU in a digital CMOS technology; (2) The requirement of off-chip components should be as few as possible; (3) Noisy blocks have to be separated from sensitive blocks in the layout and sensitive lines have to be shielded[3]; (4) The quiet current of PMU should be as low as possible to save energy.

3 Integrated PMU

The presented chip, which is mainly composed of a digital baseband processing unit and a power management unit, is implemented in 0.18μm CMOS technology with 1.8 and 3.3V transistor devices. The chip is designed to provide several power supply domains, including RF transceiver chip, CMOS image sensor, digital core, I/O pads, and LEDs. These power domains are needed to meet different demands and for cross-talk reduction by decoupling different circuits. Due to the fact that the PMU is integrated, a deep alignment between the performance requirements of the functional blocks and design parameters can be done such as maximum current, voltage range, and

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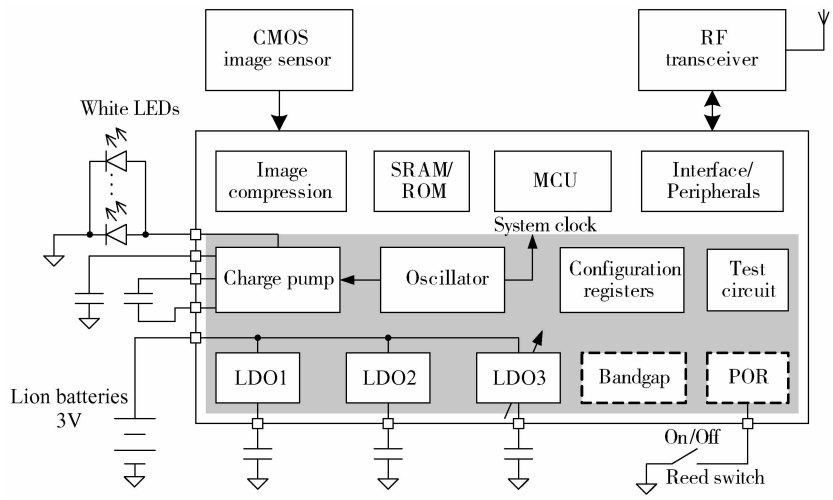

Fig. 1 Block diagram of the baseband chip with integrated PMU for wireless endoscopic system

power supply rejection (PSR).

Unlike a separate PMU chip, the integration facilitates the digital control from the digital baseband processing unit and reduces the PCB routing and its associated noise coupling. This dedicated design of the PMU results in a cost-optimized and size-miniaturized system.

3.1 Power supply architectures

To make a better compromise among power conversion efficiency, on-chip area, off-chip components, and PCB routing requirement, two possible power supply architectures that meet the integrated requirements have been considered and compared, as shown in Fig. 2. The difference between the two architectures is the selection of power supply conversion, using either linear or switched regulator types. The first architecture is built-up without a DC-DC converter and is a purely based LDO, as shown in Fig. 2. The second one uses a DC-DC convertor to generate the supply voltage for the digital core. The selection of the types of regulator is, in general, a tradeoff between power conversion efficiency and system cost. A linear regulator results in lower voltage ripple, less off-chip components, and less chip area. However, it is less efficient if the voltage difference between the input and output is large. On the other hand, switched regulators exhibit higher efficiency, but require more on-chip area for the more complex switching stage, one additional off-chip power inductor, higher voltage ripple, and have an electromagnetic interference (EMI) problem. Moreover, additional noise-reduction filtering has to be utilized to suppress the switching spurious in the receive- and transmit-band for the RF part[4].

In order to assess the two architectures, the achievable current consumption and implementation cost are evaluated. The average current consumption of all blocks is summarized in Fig. 3. The voltage of the analog and RF part is too high to justify a switching regulator. Therefore, they are supplied directly by LDOs. Only the current consumed by the digital core is relevant with the use of switching DC-DC converters. It is notable that, for the purpose of ultra low power, the supply voltage of the digital core can be scaled down from 1.8 to 1.1V without degrading the performance. This results in more than a 60% power reduction of the digital core. With the consideration

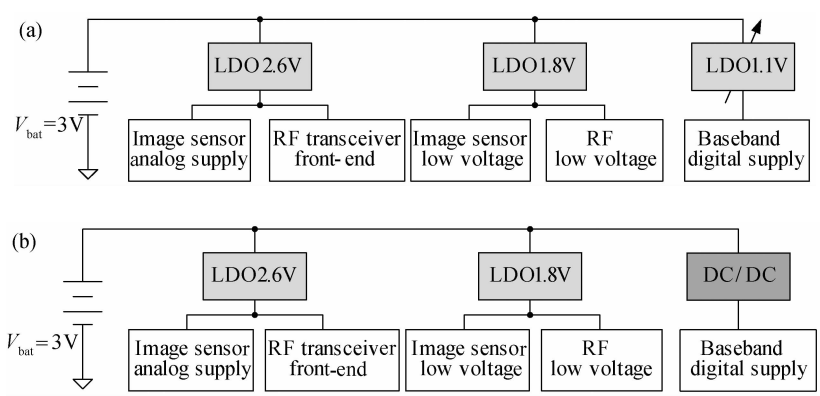

Fig. 2 Two different power supply architectures

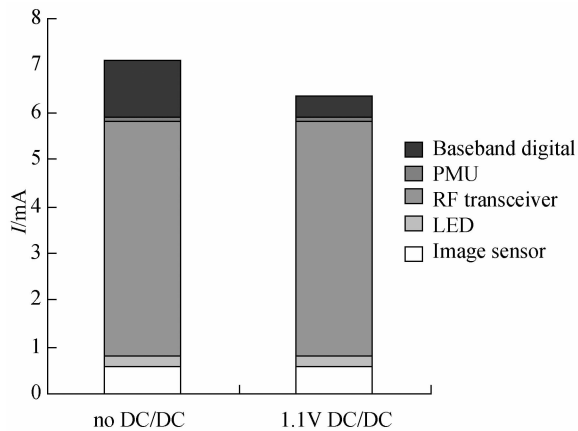

Fig. 3　Current consumption for different blocks

of voltage scaling, the application of the DC-DC convertor only saves about 10.5% of the battery current compared with the pure LDOs architecture. Therefore, considering off-chip components, chip-area, and other aspects, the pure LDOs architecture is employed in this design.

3.2　Low-dropout regulator (LDO)

The 3.3V maximum operating voltage of the 0.18μm CMOS technology facilitates the design of LDO, which regulates the battery voltage 3V down to a desired output voltage. The LDO can be directly powered by battery without an over-voltage problem. Although it is possible to design an LDO with small on-chip load capacitance to reduce the off-chip components, this requires a large die area, large quiet current[5], or a gate over driven[6,7], which is not tolerable for the low-cost and low-power target. Thus, the load capacitance is designed as the only off-chip component.

Figure 4 illustrates the LDO circuitry design. It is composed of an error amplifier, a unit-gain buffer, a pMOS pass device, a feedback network, and a loading capacitance. The pMOS pass device (MP) exhibits minimum channel length and very large width since it is designed to source 30 mA current. This in turn makes the parasitic capacitances associated with this device very large, which affects the circuit's frequency performance by reducing the value of the parasitic pole present at the gate of the pass device[8]. Therefore, phase-margin degrades and stability may be compromised unless the output impedance of the error amplifier is reduced accordingly. As a result, a unit-gain buffer stage derived from Ref. [9] is designed. The unity gain buffer isolates the large capacitance from the sensitive error amplifier and pushes the pole at the gate of the pass transistor to the high frequency.

An Ahuja compensation method[10] rather than Miller compensation is used. The cascade transistor M4 in the error amplifier is used as the transistor in the feedback path. The transconductance of the cascade transistor M4 is designed large enough to make the source of M4 virtual ground. Therefore, any current flowing through C_c goes through the source of M4 and comes out of the drain. Due to the low impedance present at node A, the pole at node A is pushed to higher frequency, which improves the phase margin of the feedback loop. Compared to Miller compensation, which connects C_c to high impedance node B, the Ahuja compensation exhibits excellent phase margin across all loads. The Ahuja compensation also provides higher PSR than classical Miller compensation. The Miller topology has worse PSR because the Miller capacitance feeds any ripple from the supply to node B thus directly to the output of LDO. The Ahuja topology has excellent PSR because of the absence of such a path.

3.3　Charge pump

The wireless endoscopic system is equipped with white LEDs as illumination devices, which need a

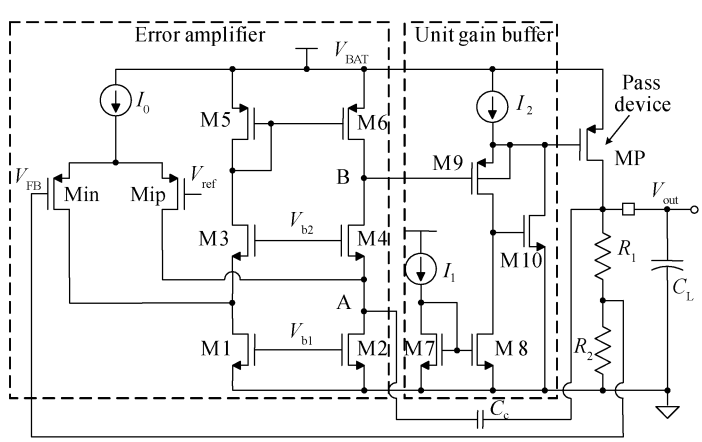

Fig. 4　Schematic of LDO

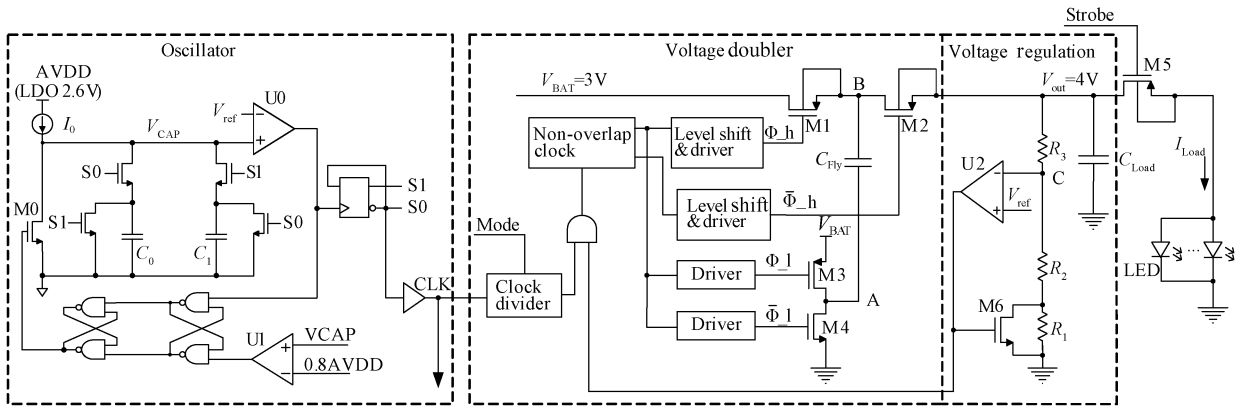

Fig. 5 Schematic of oscillator and charge pump

constant voltage higher than the battery voltage to provide constant light density. This is achieved by the integrated charge pump. One major design challenge of the integrated charge pump is the high output voltage compared with the 3.3V maximum operating voltage of 0.18μm CMOS technology. The transistor that withstands a voltage difference across their terminals of up to 4V or even more would face lifetime reduction. However, long lifetime is not required in our application since the endoscopic capsule only needs to work for tens of hours. In addition, LEDs are not conducted continuously. Therefore, short-time over voltage is allowed in this specific application.

The charge pump is mainly composed of a voltage doubler and voltage regulation, as shown in Fig. 5. The circuit works as follows. During clock phase φ, M1, M4 are on and M2, M3 are off, then the C_{Fly} is charged to V_{BAT}. During clock phase $\overline{\varphi}$, M1, M3 are off and M2, M3 are on, the voltage at node A is driven to V_{BAT}, the voltage over C_{Fly} cannot be changed, which makes the voltage at node B twice the supply voltage. The charge on C_{Fly} will be transferred to C_{Load} to accommodate a load current. A comparator U2 is used for regulating the output voltage to a desired value. The output of the comparator changes to GND if the output voltage on C_{Load} is higher than the specific level. Then the clock is gated and voltage doubler is turned off. When the output voltage is lower than the specific level as C_{Load} is discharged by I_{Load}, the clock will be opened and C_{Load} will be charged again. As a result, a constant voltage is generated. Resistors R_2, R_3 are used as voltage dividers to generate feedback voltage. A small resistor R_1 and M6 are used to prevent unnecessary switches of the output of the comparator if the voltage at node C is very close to V_{ref}. M5, controlled by strobe signal, acts as a switch to charge the LED.

For our application, the charge pump is only discharged at the moment of capturing images. To save energy, two different operating modes are implemented. If the strobe signal is active, the charge pump works in high speed mode with 1MHz clock frequency and high bias current of the comparator, resulting in large output current sourcing ability and low voltage ripple. Otherwise, 20kHz clock frequency and low bias current are employed to sustain the output voltage in order to ensure a prompt reaction of the strobe signal. With this approach, the power consumed by the charge pump is greatly saved when the LED is off.

3.4 Oscillator

The on-chip oscillator is designed not only to provide a clock for the charge pump, but also to provide a system clock for the digital core and CMOS image sensor. Thus, an off-chip crystal oscillator can be saved to reduce the PCB area.

The circuit of the oscillator is shown in Fig. 5. Capacitors C_0 and C_1 are charged and discharged by turns. Once one of the capacitors is charged above V_{ref}, the output of comparator U0 changes, which causes the output of D flip-flop to invert. Then the capacitor discharges and the other capacitor starts to repeat the same process. The frequency can be adjusted by controlling I_0. A saw tooth wave, which is composed of the voltage of C_0 and C_1, will be generated at node VCAP. The output of comparator U0 is a square wave with a certain duty cycle. The D flip-flop acts as a frequency divider that generates square waves with a 50% duty cycle. In addition to comparator U0, a second comparator U1 is used to prevent the oscillator from stopping oscillating if the frequency is too high, which is a decision by comparator U0. The reference voltage of comparator U1 is higher than that of U0. Once the voltage of node VCAP is higher than reference, the M0 will discharge the capacitors and reset the oscillator. In order to make the frequency independent of the variation of battery voltage, the oscillator is powered by the output of LDO.

3.5 Bandgap reference

A fully-integrated bandgap reference voltage generator provides a reference voltage and bias currents for the other circuit. It adopts a classical self-biased cascade structure to eliminate the dependence of supply voltage and temperature. The current consumed by the bandgap reference is 12μA.

3.6 Soft start-up

Due to the limited ability of sourcing current for the battery, a large start-up peak current may cause an apparent voltage drop of batteries, which will result in a failure of start-up. In order to minimize the peak current, soft-start ability should be included in the PMU. This is achieved by generating different start signals at different time slots for each block. The time intervals between the two start signals are specified by the RC delay. Therefore, blocks in PMU will be enabled in a predefined sequence and a large start-up current can be avoided, which results in a more stable start-up process. Furthermore, the reset signal of the digital core is also generated at the end of the start-up process when the supply voltage is stable.

3.7 Integration aspects

For the purpose of saving PCB area, only large capacitances are used as off-chip components while all the other capacitance and resistors are fully integrated. The process variation makes it very difficult to promise precise values for on-chip capacitances and resistors, which will cause a variation of the circuit performance, like the voltage level of bandgap reference or the frequency of the oscillator. Therefore, resistor and capacitance with trim ability are widely used. The trim options are controlled by the configuration register files, which can be controlled by the digital core. The configuration process can be started by wireless communication. This facilitates the configuration even if the endoscopic system were hermetically encapsulated within the package.

Furthermore, the regulators for analog and digital power supply lines are separated locally with adequate space between each other. It helps to reduce the inductive coupling of the digital power supply, where mainly the high frequency switching current generates spuriousness in the analog domains while the average DC current causes no trouble[11]. The PMU is placed at the corner of the die for a maximum isolation distance. Each block is surrounded by p-plus and n-well guard rings for further isolation. Neither triple-well nor deep n-well was utilized to reduce technology cost.

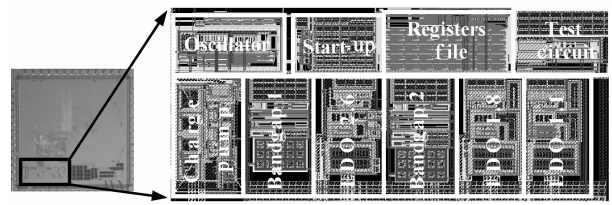

Fig. 6　Layout of the baseband chip and PMU

4 Implementation and experimental results

The layout of the PMU is shown in Fig. 6. It was fabricated in 0.18μm 1 poly 6 metals CMOS technology. The PMU is located in the left bottom corner of the layout with an area of 1301μm × 515μm. Only 5 off-chip capacitances less than 1μF with micro-SMD packages are required, which effectively saves PCB board area. The overall quiet current of PMU is less than 100μA. The experimental results of each block are as follows.

The LDO is tested under V_{BAT} = 3V and ceramic output capacitor C_L = 1μF. The ESR of C_L is less than 100mΩ. The LDO is stable as the load current condition changed from 0 to 30mA. The DC gain of the LDO is over 80dB. The phase margin of the loop is no less than 40° under different load currents and PVT corners. The PSR is higher than 70dB at a frequency of 50kHz, which is expected due to the application of the Ahuja compensation method. The detailed performance parameters achieved with the LDO are summarized in Table 1.

The charge pump is designed with two off-chip capacitances, namely a fly capacitance of 0.1μF and a load capacitance of 1μF. The output voltage of the charge pump ranges from 3.6 to 5.5V. The performance of charge pump in different mode is summarized in Table 2. 5mA load current sourcing ability and

Table 1　Performance summary of LDOs

	1.8V & 1.1V LDO	2.6V LDO	Condition
V_{in}	3.0V	3.0V	
Load capacitance	1μF	1μF	
Output current	0～30mA	0～30mA	
Quiescent current	18μA	20μA	No load current
Line regulation	0.25mV	0.14mV	V_{in} = 2.8～3.2V
Load regulation	1.9mV	2.0mV	I_{Load} = 0.1～30mA
Line transient response	2.9mV	1.7mV	V_{in} = 2.8～3.2V
Load transient response	6.4mV	6.0mV	I_{Load} = 0.1～30mA
Power supply rejection	73dB	72dB	Frequency @50kHz
Chip area	0.046mm^2	0.046mm^2	

Table 2 Performance of charge pump in different modes

Mode	Clock	$I_{control}$	V_{out}	Voltage ripple
High speed	1MHz	14μA	4V	50mV@5mA
Low speed	20kHz	4μA	4V	210mV@0mA
Standby	No clk	$<$ 1nA	0V	—

50mV voltage ripple can be achieved in high speed mode with 14μA quiet current and 1MHz clock frequency. This promises a constant light density of illumination LEDs. In low speed mode, the quiet current is reduced to 4μA to save power while maintaining the output voltage.

The fully integrated on-chip oscillator generates clock signals with 5% frequency variation due to device variation. With the calibration, the frequency of the oscillator will be fixed at 20MHz. The 20MHz clock signal is fed to the digital core, CMOS image sensor, and the charge pump.

Figure 7 shows the soft start-up process of PMU, in which 2.6V LDO, 1.8V LDO, and the charge pump are started at different time slots. The peak current at start-up process is no more than 60mA, which can be sustained by the battery. The overall start-up time is less than 400μs. The calibration of the PMU can be performed by the digital core afterward. The bandgap reference, output voltages of LDOs and charge pump, the frequency of oscillator all can be adjusted to the desired values. In order to keep the calibration results when PMU is disabled in standby mode, the calibrated values are stored in an always-on register file that is directly powered by the battery instead of the output of the LDO. Thus, the calibration of the PMU has to be performed only once before the wireless endoscope capsule is hermetically encapsulated within the package. This facilitates the production and assembly process.

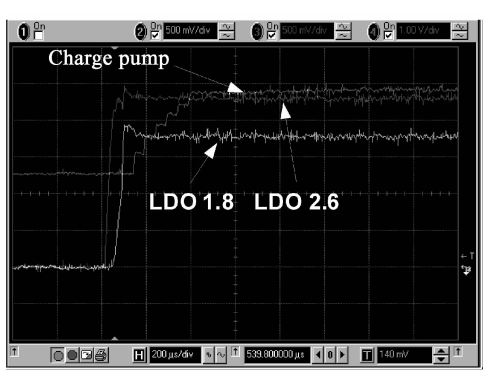

Fig. 7 Start-up measurement result (the other blocks are not shown)

5 Conclusion

This paper presented an integrated power management unit in 0.18μm CMOS technology for a battery-operated wireless endoscopic capsule system. The integration of this power management unit enables the build-up of a miniature wireless endoscopic capsule with only five off-chip capacitances. Optimized power supply architectures are derived from comparison. Details of the circuit including LDO, charge pump, bandgap, oscillator, and start-up are given. Measurement results show that PMU is suitable for a battery powered system.

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一种用于电池供电的无线内视镜系统的片上集成的电源管理单元*

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摘要：介绍了一种应用于电池供电的无线内视镜系统的片上集成的电源管理单元.该电源管理单元使用标准的 0.18μm CMOS 工艺与基带处理芯片集成在一起.电源管理单元的集成减小了系统成本，方便了 PCB 的设计并缩小了系统的尺寸.通过比较得到了优化的电源结构方案，并描述了该方案中子模块电路的具体实现.整个电源管理单元只需 5 个片外小电容元件，其整体消耗的静态电流小于 100μA.此外，该方案还采用数字校准的方法以克服工艺偏差对电路性能的影响.本文还描述了电路所达到的性能指标及相应的测试结果.

关键词：电源管理单元；低压差稳压器；电荷泵；振荡器；片上集成；无线内视镜系统
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