InP-base resonant tunneling diodes

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Abstract: We have fabricated $In_{0.53}Ga_{0.47}As$/AlAs/InP resonant tunneling diodes (RTDs) based on the air-bridge technology by using electron beam lithography processing. The epitaxial layers of the RTD were grown on semi-insulating (100) InP substrates by molecular beam epitaxy. RTDs with a peak current density of 24.6 kA/cm^2 and a peak-to-valley current ratio of 8.6 at room temperature have been demonstrated.

Key words: RTD; electron beam lithography; air-bridge

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1. Introduction

The resonant tunneling diode (RTD) is one of the most promising devices in the field of nanometer devices. The RTD is the most promising for ultra-high frequency, ultra-high speed, and low power consumption devices[1−3]. The RTD has attracted much attention in recent years, because it can reduce the circuit complexity while providing the same functions as conventional CMOS implementations. Because of improvements in growth and fabrication technologies, peak–valley current ratios up to 30 and oscillation frequencies over 700 GHz at room temperature have been demonstrated[4]. In addition, a variety of compact size and low-power circuits have been analyzed by using different structures based on RTDs with negative differential resistance characteristics[5].

The $In_{0.53}Ga_{0.47}As$/AlAs/InP material system shows the highest peak-to-valley current ratio (PVCR) and the highest speed at room temperature due to the large increase in the conduction band discontinuities of the potential barrier, the electron mobility of the emitter and the collector, and allows a non-alloyed ohmic contact with a contact resistivity as low as 1.7×10^{-8} Ω·cm^2[6, 7] relative to the GaAs material system. Because the realization of InP-based RTD devices is very difficult, InP-based RTD development in China has been reported rarely. In this paper, we develop RTD samples based on the InGaAs/AlAs/InP system incorporating an air-bridge, which is made by electron beam lithography processing. For this type of diode characteristics for PVCR of 8.6 and a peak current density of 24.6 kA/cm^2 at room temperature are demonstrated.

2. Material growth

The RTDs were grown in a Vecoo GENII MBE system. Polished (100) Fe-doped semi-insulating 3-inch InP substrates were used in this work. The material structure is shown in Fig. 1. The symmetric RTD structure used in this work consists of a 300-nm n$^+$-InGaAs emitter-contact layer (1.5×10^{18} cm^{-3}, Si), a 100-nm n-InGaAs emitter layer (2×10^{17} cm^{-3}, Si), a 1.8-nm intrinsic InGaAs isolation layer, an undoped double-barrier structure sandwiched with a 2.8-nm AlAs/5.1-nm $In_{0.53}Ga_{0.47}As$/3.0-nm AlAs strained well, an 1.8-nm intrinsic InGaAs isolation layer, a 100-nm n-InGaAs collector layer (2×10^{17}cm^{-3}, Si), and, finally, a 100-nm n$^+$-InGaAs collector-contact layer (1.5×10^{18} cm^{-3}, Si).

In the RTD structures, there are two different thicknesses of the barrier layers; the emitter barrier is thinner than the collector barrier. The emitter barrier became lower when the device was biased, and at the same time, the electron flow was mainly limited by the collector barrier. So, we can effectively improve the PVCR of the RTD and increase its negative differential resistance effect by increasing the thickness of the collector barrier. We decreased the thickness of the emitter barrier at the same time to improve the peak current density. The peak current density can index increase when the barrier thickness is decreased. The spacer of the RTD is a thin layer of intrinsic InGaAs between the emitter and the barrier regions. It has two functions: first, it stops the impurity diffusion from the emitter regions to the barrier and well regions; second, the fact that an

InGaAs:Si	100 nm	1.5×10^{18} cm^{-3}
InGaAs:Si	100 nm	2×10^{17} cm^{-3}
InGaAs		1.8 nm
AlAs		3.0 nm
$In_{0.53}Ga_{0.47}As$		5.1 nm
AlAs		2.8 nm
InGaAs		1.8 nm
InGaAs:Si	100 nm	2×10^{17} cm^{-3}
InGaAs:Si	300 nm	1.5×10^{18} cm^{-3}

Fig. 1. Schematic cross section of an $In_{0.53}Ga_{0.47}As$/AlAs/InP resonant tunneling diode.

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Table 1. RTD process developed in this work.

Step	Name	Description
1	Contact 1	Patterning of photoresist; Deposition and metal lift off for the first contacts of the diodes
2	RTD mesa	Etch semiconductor layer to form contact 2 layer using contact 1 metal as mask
3	Contact 2	Patterning of photoresist; Deposition and metal lift off for the second contacts of the diodes
4	Isolation	Patterning of photoresist; Etch down to the semi-insulating substrate
5	Passivation	Deposition of Si_3N_4 by PECVD
6	Via hole	Patterning of photoresist; Via hole etching by RIE to form interconnects
7	Interconnection	Patterning of photoresist; Deposition and metal lift off for the interconnects

intrinsic InGaAs layer forms a sub-well in the emitter regions will transform the three-dimensional/two-dimensional resonant tunneling into a two-dimensional/two-dimensional resonant tunneling, which can improve the *I–V* characteristics and the PVCR of RTDs.

We researched the effect of increasing spacer layer thickness on the PVCR of RTDs[8]. A thick spacer layer requires a two-step electron transport process. The first step is a thermionic emission and/or tunneling across the emitter spacer layer, followed by tunneling through the rest of the double-barrier structure as the second step. When increasing the spacer layer width, thermionic emission over the emitter spacer layer barrier becomes the rate-limiting transport process, leading to a suppression of the resonant tunneling current and a leakage current (thermionic emission of electrons over the double-barrier and photon assisted electron tunneling across the double-barrier). Below the critical spacer width, the current density and PVCR continue to improve with increasing the spacer layer thickness. Above this critical width, PVCR of RTDs has not been improved. The exact design of the optimum spacer layer thickness to achieve a maximum PVCR is made difficult due to the necessary compromise between an improved performance following a reduction of impurity scattering and a decreased performance by a suppression of the tunneling current due to the spacer barrier.

3. Device fabrication

Our technology uses electron beam lithography and contact photolithography and does not require dry-etching techniques, allowing a fast fabrication time. A simple mask set has been designed and made for the fabrication of RTDs. Since both contact layers are heavily-doped (n^+) InGaAs layers, non-alloyed ohmic contacts (Au/Pt/Ti) were used. A non-selective wet etching by an $H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 40$ solution was used for the mesa formation with the first ohmic contact as the etching mask. Several additional process steps are necessary; these include device isolation, passivation, via hole opening, and air-bridge interconnection formation. The process procedures are described in Table 1.

Air-bridge interconnection technology has been widely applied in high-speed devices because of its advantages of low parasitic capacitance, high current work, eliminating the impact of the edge, and so on. The air-bridge interconnection process was developed for the RTD fabrication by using e-beam lithography and electron beam evaporation technologies in this study. The MMA, PMGI(SF11) and AZ1518 photoresists are used to form the air-bridge. PMGI resist can be flowed during the postbake process in order to produce a sloped sidewall profile in the patterned openings. PMGI resist is simply removed using its solvent: n-methylpyrollidone (NMP). In order to avoid tearing off the metallization, the deposition of Ti/Au/Pt/Ti was done four times through beam evaporation, though it is preferable to use one depositing step. Figures 2 and 3 are the SEM images of the fabricated RTD using the air-bridge interconnection technology.

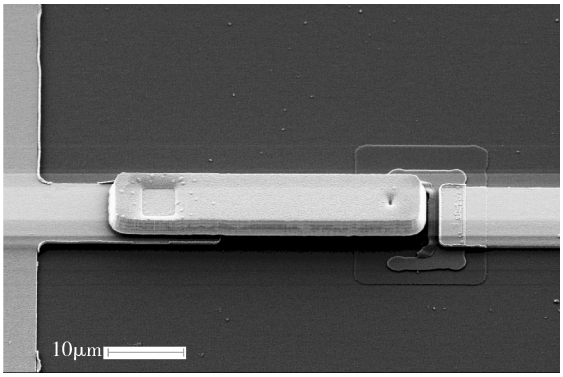

Fig. 2. SEM image of the fabricated RTD with air-bridge.

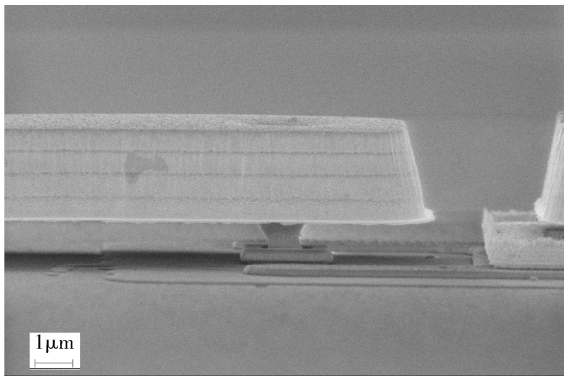

Fig. 3. SEM image of the air-bridge.

4. Results and discussion

We have measured the RTD devices by using a transistor characteristic curve tracer at room temperature. Figure 4 is the *I–V* curve of a $8 \times 8\ \mu m^2$ RTD at room temperature. The peak current density is 24.6 kA/cm^2, the valley current density is

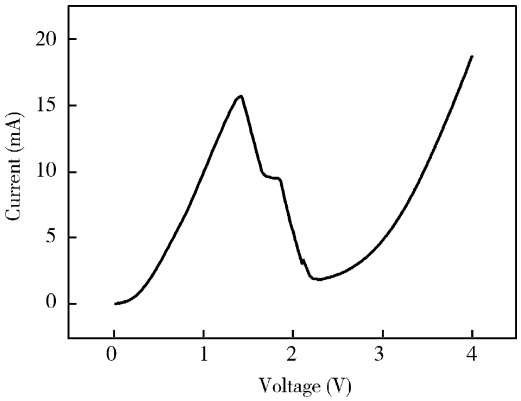

Fig. 4. I–V curve of a 8×8 μm^2 RTD at room temperature.

2.86 kA/cm^2, and the peak–valley current ratio is 8.6.

The measured data shows that the peak current density of the RTD is not high enough because AlAs barrier layer is too thick. Another cause for the low peak current density is that increasing the spacer thickness results in a smaller capacitance. The I–V curve of the RTD for low voltage values is not straight, because the non-ideal ohmic contacts of the device result in a higher series resistance in the diode. Following improving device processing, material growth conditions and adjusting barrier and spacer layer structure parameters, we believe that a better PVCR and peak current density will be attained. In addition, the application of an InAs subwell can effectively reduce the peak voltage of RTDs. These attempts are now in progress.

In the RTD curve (Fig. 4), there is a plateau region between the peak and valley. It is believed that this plateau region is due to an oscillation between the RTD and the measurement system[9]. It is not a real feature in the DC characteristic[10].

5. Conclusion

The RTD design used an InGaAs layer as the well and an AlAs layer as the barrier in the double-barrier structures .The RTD material was grown on a 3-inch InP substrate by MBE. The fabrication processes of the devices have been systematically investigated and analyzed. RTD devices based on these processes have been fabricated successfully, and the electronics characteristics of the fabricated RTD devices at room temperature were tested. We obtained a peak current density of 24.6 kA/cm^2 and a peak–valley current ratio of 8.6.

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