Design and analysis of a UWB low-noise amplifier in the 0.18 μm CMOS process*

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Abstract: An ultra-wideband (3.1–10.6 GHz) low-noise amplifier using the 0.18 μm CMOS process is presented. It employs a wideband filter for impedance matching. The current-reused technique is adopted to lower the power consumption. The noise contributions of the second-order and third-order Chebyshev filers for input matching are analyzed and compared in detail. The measured power gain is 12.4–14.5 dB within the bandwidth. NF ranged from 4.2 to 5.4 dB in 3.1–10.6 GHz. Good input matching is achieved over the entire bandwidth. The test chip consumes 9 mW (without output buffer for measurement) with a 1.8 V power supply and occupies 0.88 mm^2.

Key words: ultra-wideband; low-noise amplifier; CMOS

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1. Introduction

Ultra-wideband (UWB) is a new wireless technology that is expected to improve the performance and reduce the power consumption and cost of short-range wireless communications in applications such as remote controllers, RF-IDs, sensor networks, and wireless personal area networks (WPANs)[1]. As approved by FCC, the UWB system using the unlicensed frequency band of 3.1–10.6 GHz is of much interest for broadband wireless communications. A critical component of the ultra-wideband system is the wideband low-noise amplifier (LNA). It should provide a low noise figure, stable gain, and good input matching over the entire bandwidth simultaneously with low power consumption. In addition, it is highly desirable to implement this amplifier in CMOS technology in order to perform a high level of integration with the digital baseband processor.

There are several solutions for the wideband amplifiers in CMOS. The distributed amplifiers provide impedance matching, flat gain over wide bandwidth, but they are usually power hungry and occupy a large area for the use of on-chip transmission lines. The resistive-shunt feedback amplifiers provide wideband input matching, low NF using large loop gain. But they require large power to achieve a high loop gain in a single stage. The common-gate low-noise amplifiers achieve wideband input matching straightforwardly, but the gain is usually low and the input matching is sensitive to the variations of components.

In this paper, a UWB low-noise amplifier using the 0.18 μm CMOS process is presented. We design a multi-section passive network to form a second-order Chebyshev bandpass filter for input matching. A current-reused technique is adopted to lower the power consumption. The ladder-filer is a topology well known for its low sensitivity to component variations[2], so we can perform robust input matching with this structure.

2. UWB LNA architecture

The proposed ultra-wideband LNA is shown in Fig.1, and all components in the figure are integrated on-chip. A second-order Chebyshev filter is chosen for the input matching in this design. Inductor L_{G2} and capacitor C_G are used to couple the output of the first stage to the second stage. The L_{LD1} is large enough in the interesting band to block the path from M1 to M2. The load presents a peaking at high frequency so as to compensate for the gain roll-off of the amplifier. A source follower is added as the buffer for the measurement.

3. Design and analysis

The design and analysis of the amplifier in all aspects, such as input matching, gain and noise, are described in detail as follows.

3.1. Input impedance matching

The inductively degenerated common-source technique is widely used in narrow-band designs. But it can achieve impedance matching only in a narrow-band[3,4]. In this paper, we adopt the wideband bandpass filter for input matching[2,11]. The equivalent schematic of the input matching network is shown in Fig.2. The C_1 is used as an AC-coupling capacitor

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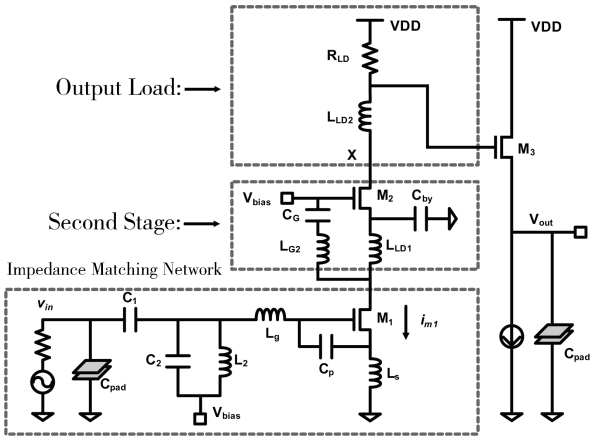

Fig.1. Proposed ultra-wideband low-noise amplifier.

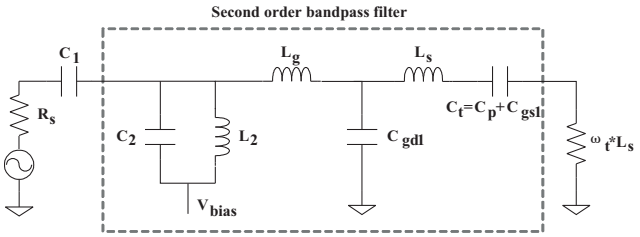

Fig.2. Schematic of the LNA input matching network.

Table 1. Input matching networks components.

Type	Order	L_2 (nH)	C_2 (fF)	$L_g + L_s$ (nH)	C_{gs1} + C_p (fF)
Chebyshev	2	1.9	300	1.2	700

here. The inductors L_2, L_g, L_s, and capacitors C_2, C_{gs1}, C_p compose a second-order Chebyshev filter, whose passband is 3.1–10.6 GHz. The input impedance of the matching network is

$$Z_{in}(s) = \frac{\omega_t L_s}{W(s)}, \tag{1}$$

where $W(s)$ is the transfer function of the filter. $|W(s)|$ is the approximate unity in the passband, and tends to zero out-of-band. The input impedance of the amplifier is equal to $\omega_t L_s$ in the passband, and it is very high out-of-band. Assume that the ripple in the passband is ρ_p, and then the input reflection coefficient can be expressed as [2]

$$\Gamma^2 = 1 - 1/\rho_p. \tag{2}$$

To achieve the reflection coefficient less than –10 dB, Equation (2) yields $\rho_p < 0.5$ dB. We can derive the component values for this second-order Chebyshev filter using a filter synthesis tool. Table 1 shows the calculated component values.

3.2. Gain analysis

The total gain of the proposed LNA is equal to the product of the gain of the first and second stages.

Compared with the transconductance, g_m, of the transistor, the effective transconductance (G_m)[5] is a more suitable parameter to estimate the gain performance of the radio frequency amplifier. The G_m is defined as the amplitude of the output current i_{out} flowing into the load, divided by the input

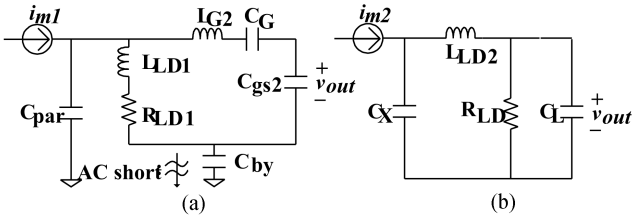

Fig.3. Equivalent circuit of the loads of the amplifier: (a) Load of first stage; (b) Load of second stage.

voltage of the amplifier v_{in}. Obviously, the G_m is proportional to the g_m of the input transistor, and the proportional coefficient depends on the input network. We can see that the G_m of the second stage is g_{m2} straightforwardly. From Fig.2, the gate-source voltage of M1, V_{gs1} is $v_{in}W(s)/sC_t\omega_t L_s$, where C_t equals to $C_{gs1} + C_p$, therefore the G_m of the first stage, G_{m1} can be expressed as

$$G_{m1} = \frac{i_{m1}}{v_{in}} = \frac{g_{m1}W(s)}{sC_t\omega_t L_s} = \frac{g_{m1}W(s)}{sC_t R_s}. \tag{3}$$

The equivalent circuits of the loads are shown in Fig.3. From Fig.3 (a), the load impedance of the first stage can be written as

$$\begin{aligned} Z_{L1} = \frac{v_{out}}{i_{m1}} &= [(sL_{G2} + \frac{1}{sC_G} + \frac{1}{sC_{gs2}}) \\ &\quad \|(sL_{LD1} + R_{LD1})] + \frac{1}{sC_{by}}]\|\frac{1}{sC_{par}} \\ &\approx \frac{R_{LD1} + sL_{LD1}}{(R_{LD1} + sL_{LD1}) + (sL_{G2} + 1/sC_G + 1/sC_{gs2})} \\ &\quad \times\frac{1}{sC_{gs2}}, \end{aligned} \tag{4}$$

where R_{LD1} is the parasitic resistor of inductor L_{LD1}, and C_{par} is the total parasitic capacitor at the drain of transistor M1. In the practical design, the capacitor C_{by} in Fig.3 (a) is chosen to be large enough so that the source of transistor M2 can be seen as AC ground. If $L_{LD1}+R_{LD1}$ exhibits higher impedance than L_{G2}, C_G and C_{gs2} in series, the resonant frequency is mainly determined by the L_{G2} and C_G. Note that the resonance presents a narrow-band characteristic. Therefore, the gain is maximized near the resonant frequency, which is designed to enhance the gain at the middle of the desired band.

The stagger-compensated series peaking technique[6] is adopted in the second stage to compensate for the high frequency gain roll-off. The equivalent circuit of the load using this peaking technique is shown in Fig.3 (b). The load impedance of the second stage can be written as

$$\begin{aligned} Z_{L2} &= \frac{v_{out}}{i_{m2}} \\ &= \frac{R_{LD}}{1 + sR_{LD}(C_x + C_L) + s^2L_{LD2}C_1 + s^3L_{LD2}C_xC_LR_{LD}}, \end{aligned} \tag{5}$$

where C_x is the total parasitic capacitor at the drain of transistor M2, and C_L is the total capacitor at the input of the buffer. At $\omega_r = 1/\sqrt{L_{LD2}C_x}$, L_{LD2} resonates with C_x, thus the response shows a peak at ω_r which compensates for the gain roll-off of the amplifier at high frequency.

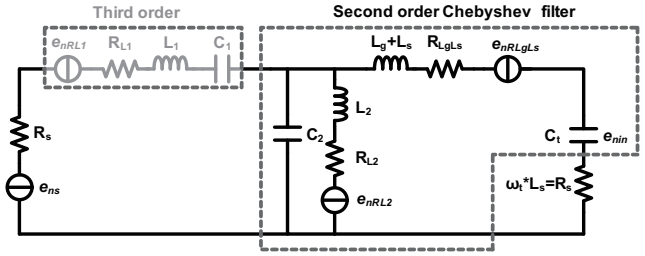

Fig.4. Noise model of the input matching network.

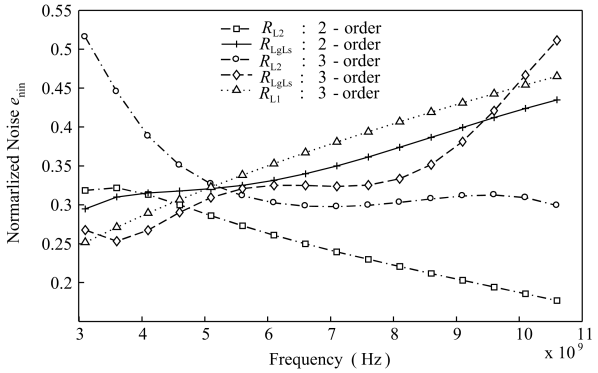

Fig.5. Simulated normalized $e_{\rm nin}$ assuming Q =7 in 3.1–10.6 GHz for all inductors.

Combining the gain versus frequency characteristic of the two stages, the gain flatness can be achieved over the entire bandwidth.

3.3. Noise analysis

In the proposed LNA, the noise of the second stage is reduced by the gain of the former stage, so the noise performance is dominated by the first stage. The two main noise contributors of the first stage are: the losses of the input matching network and the input transistor M1. The noise factor NF of amplifier considering M1 only can be written as Eq.(6), and detail derivation can be seen in Ref.[2].

$$F(\omega) = 1 + \frac{P(\omega)}{g_{\rm m}R_{\rm s}}\,\frac{\gamma}{\alpha}, \tag{5}$$

where

$$\begin{aligned} P(\omega) &= \frac{p^2\alpha^2\chi^2(1-|c|^2)}{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2} \\ &\quad + \omega^2C_{\rm t}^2R_{\rm s}^2(1+2|c|p\alpha\chi+p^2\alpha^2\chi^2), \qquad (6) \\ \chi &= \sqrt{\frac{\delta}{5\gamma}}. \end{aligned}$$

In Eq.(7), $p = C_{\rm gs}/C_{\rm t}$, c is the correlation coefficient between the gain noise and the drain noise, δ and γ are the excess noise parameters, and $\alpha = g_{\rm m}/g_{\rm d0}$ accounts for short-channel effects. For CMOS devices, $\delta \approx 1.33-4, \gamma \approx 0.67-1.33$, and $c \approx 0.4{\rm j}$[7]. Equations (6) and (7) show that increasing the transconductance improves the noise performance while all the other parameters keeping constant. To achieve better noise performance, we can increase the bias current, as long as the noise performance is limited by the contribution of M1. The NF is also affected by the over-drive voltage of M1. Simulation reveals that, for a given current budget, there is a value of M1 width that yields the best average NF over the whole bandwidth. This is the same as its narrow band counterpart. In this design, the dominant noise contributor is input transistor M1.

For silicon based passive devices, the quality factor (Q) at high frequency is limited by the losses in the silicon substrate. The parasitic resistance of the inductor increases as frequency rises, but the effective transconductance ($G_{\rm m}$) of the first stage decreases as frequency rises. This will deteriorate the noise performance at high frequency. The noise model of the input matching network is shown in Fig.4. The L_1 and C_1 in light gray are components of the third-order Chebyshev filter used in Ref.[2], where $R_{\rm L1}$ is the parasitic resistor of L_1. The $R_{\rm L2}$ and $R_{\rm LgLs}$ are the parasitic resistors of L_2 and $L_{\rm g}+L_{\rm s}$. The voltage sources $e_{\rm nRL1}$, $e_{\rm nRL2}$, and $e_{\rm nRLgLs}$ represent the thermal noise generated by resistors $R_{\rm L1}$,$R_{\rm L2}$ and $R_{\rm LgLs}$. The transfer functions for these three noise sources are listed as below.

$$TF_{\rm RL1} = \frac{e_{\rm nin}}{e_{\rm nRL1}} = \frac{W(s)}{[W(s)+1]sC_{\rm t}R_{\rm s}}, \tag{7}$$

where $W(s)$ is the third-order Chebyshev filter transfer function.

$$TF_{\rm RL2} = \frac{e_{\rm nin}}{e_{\rm n}R_{\rm L2}} = \frac{(1/sC_2)\|Z_{\rm g,s}\|Z_1}{Z_2+(1/sC_2)\|Z_{\rm g,s}\|Z_1}\;\frac{1}{Z_{\rm g,s}(sC_{\rm t})}, \tag{8}$$

$$TF_{\rm RLgLs} = \frac{e_{\rm nin}}{e_{\rm n}R_{\rm LgLs}} = \frac{1}{Z_{\rm g,s}+Z_1\|(1/sC_2)\|Z_2}\;\frac{1}{sC_{\rm t}}, \tag{9}$$

where $Z_2 = sL_2 + R_{\rm L2}$,$Z_{\rm g,s} = s(L_{\rm g}+L_{\rm s}) + R_{\rm LgLs} + 1/(sC_{\rm t}) + R_{\rm s}$, $Z_1 = sL_1 + R_{\rm L1} + R_{\rm s} + 1/sC_1$ for the third-order filter, and $Z_1 = R_{\rm s}$ for the second-order filter. The simulated $e_{\rm nin}$ caused by these noise sources normalized to $e_{\rm nin}$ caused by $e_{\rm ns}$ is shown in Fig.5. To simplify the simulation, Q = 7 over 3.1–10.6 GHz for all inductors are assumed. We can see that the noise contribution from the passive devices of the third-order filter is much larger than that of their second-order counterpart, so a second-order Chebyshev filer is more suitable to shoot for low noise.

3.4. Circuit design

The input matching network is designed first. Equation (3) shows that the gain of the amplifier is inversely proportional to the capacitance $C_{\rm t}$. In this paper, we make $C_{\rm t}$ smaller than the value achieving the best input reflection performance. This helps us obtain larger gain and lower noise with moderate S_{11}. For a given current budget, 5 mA, the width of M1 (200 μm) is optimized for noise and sized to make the contributions of thermal and induced gate noise balanced. Simulation helps in choosing the final values of the components: $L_{\rm s}$ = 0.45 nH, $L_{\rm g}$ = 0.75 nH, L_2 = 1.9 nH, C_2 = 0.3 pF, and $C_{\rm t}$ = 0.7 pF.

The parasitic inductance of bonding wire connecting $L_{\rm s}$ to the PCB ground impacts the input matching network severely. Several PADs are in parallel between $L_{\rm s}$ and PCB ground to mitigate this effect.

Table 2. Summary of measurement results and comparisons with previous work.

	Ref.[2]	Ref.[6]	Ref.[9]	This work
Process	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Bandwidth (GHz)	3.1–10.6	3.1–10.6	3.1–10.6	3.1–10.6
S_{11} (dB)	< −9.4	< −10	< −11	< −9.8
S_{22} (dB)	N/A	< −10	N/A	< −12
S_{21} (dB)	10.4(Max)	8.5(Max)	9.7(Max)	12.4–14.5
S_{12} (dB)	< −35	N/A	N/A	< −11
NF (dB)	5.3(Avg)	4.4–5.3	4.5–5.1	4.2–5.4
IIP3 (dBm)	–6.7@6 GHz	7.4–8.3	–6.2@6 GHz	–7.2@6 GHz
Power (mW)	9	4.5	20	5 mA×1.8 V
Area (mm^2)	1.1	1.0	0.59	0.88

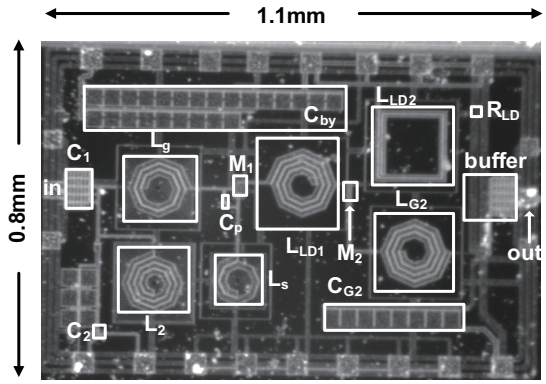

Fig.6. Microphotograph of the proposed LNA.

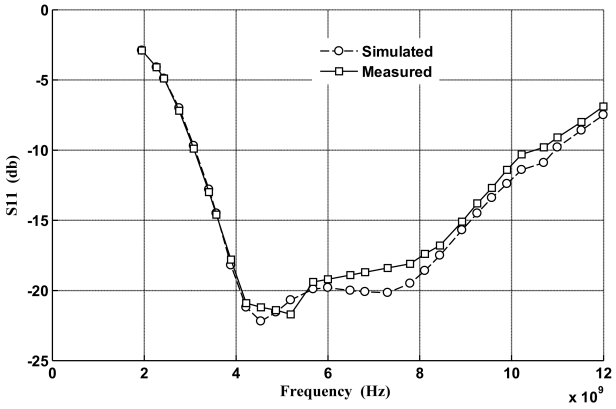

Fig.7. Simulated and measured input reflection coefficient (S_{11}).

The L_{G2} performs series-resonant with C_{G2} and C_{gs2} for a low impedance path to couple the output of the first stage to the input of the second stage, while the inductor L_{LD1} is chosen to be large enough to provide a high impedance path to block the signal in the interesting band. In this design, the inductance value of L_{LD1} is set to be 2 nH. The series-resonant frequency of the coupling path is chosen at 5.8 GHz which will improve the gain-flatness over the entire bandwidth. The component values of the coupling path are L_{G2} = 2 nH and C_{G2} = 3.8 pF.

The load of the second stage is designed to present a peaking at high frequency (9 GHz), which compensates for the gain roll-off of the amplifier. The inductance value of L_{LD2} is set to be 2.4 nH. The value of R_{LD} is set as large as possible to enhance the gain of the amplifier. The upper limit of R_{LD} is set by the voltage head room and the bandwidth, and R_{LD} is set as 90 Ω here. A small resistor ($R \approx 10$ Ω) that is not shown in Fig.1 is added in the series with L_{LD2} to broaden the peaking response [6]. The transistor M2 is chosen to be as small as possible to reduce the parasitic capacitances. The lower limit to the size of M2 is set by its noise contribution. The width of M2 also affects the linearity of the amplifier. In this design, the width of M2 is chosen as 100 μm.

The buffer is designed to drive the 50 Ω external load for measurement purposes, so the transconductance of M3 must be equal to 1/50. The bias current of M3 is selected to be 5 mA, and the width of M3 is 70 μm.

The bias voltages for M1 and M2 are set externally to investigate the impacts of the transistor bias conditions on the performance of the amplifier flexibly. The buffer is biased by means of a current mirror which is not shown in Fig.1. All the inductors used are simulated and characterized by the Agilent Advanced Design System (ADS)[10].

4. Measurement results

The test chip has been fabricated in a 0.18 μm mixed-signal CMOS process. The microphotograph of the LNA is shown in Fig.6. The die area including I/O PADs is 0.88 mm^2. All I/O PADs are not electrostatic-discharge (ESD) protected to decrease the parasitic capacitance. The raw die is mounted on the PCB by the COB (Chip-on-Board) package. The DC signals are supplied through the PCB. The measurements are carried out by mounting the PCB on a Cascade M150 Manual probe station. RF probes are used for RF signals measurement. The losses due to the RF probes and cables are calibrated using WinCal software[8]. The S-parameters are measured using an Agilent N5230A Network Analyzer.

Figure 7 shows the simulated and measured input reflection coefficients (S_{11}). As can be seen, the measurement results meet the simulation very well, and S_{11} is less than −9.8 dB between 3–11 GHz. The measured output coefficients (S_{22}) are less than –15 dB over the whole bandwidth.

The simulated and measured power gain (S_{21}) and reverse isolation (S_{12}) are presented in Fig.8. The power gain is 12.4–14.5 dB between 3.1–10.6 GHz. The measured reverse isolation is less than –11.2 dB over the entire bandwidth.

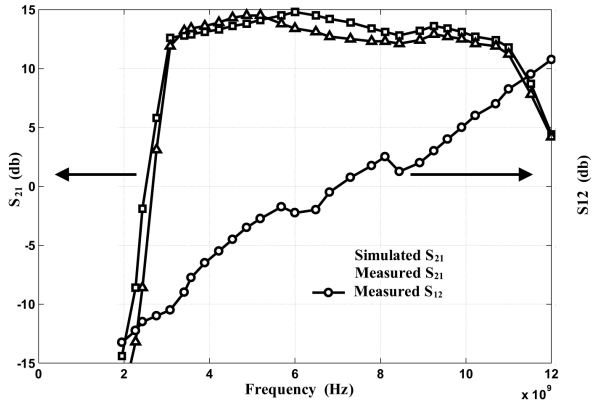

Fig.8. Simulated and measured power gain (S_{21}) and reverse isolation (S_{12}).

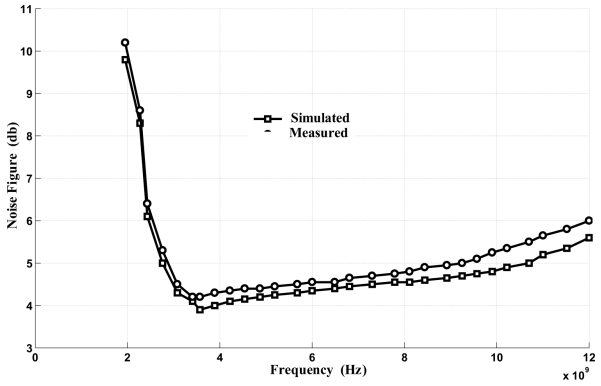

Fig.9. Simulated and measured Noise Figure (NF).

Without the cascade transistor, the reverse isolation is worse than the classical cascade amplifier[2] as expected.

The measured and simulated noise factors (NF) are depicted in Fig.9. The minimum NF is as low as 4.2 dB. The NF is between 4.2–5.4 dB over the entire bandwidth. The difference between the simulated and measured NF at high frequency probably results from: (1) the quality factors of inductors are lower than simulated; (2) the imprecise of the transistor's noise model at high frequency.

The measured third-order intermodulation distortion (IIP3) is –7.2 dBm at 6 GHz. Table 2 gives the measurement results compared with the recently published works for UWB low-noise amplifier in the 0.18 μm CMOS process.

5. Conclusion

In this paper, a low-noise amplifier for an ultra-wide band (3.1–10.6 GHz) is designed. A Current-Reused technique is used for lower power consumption. The input matching, gain, and noise performance of the amplifier are analyzed in detail. The test chip is fabricated in the 0.18 μm CMOS process. The proposed LNA provides a power gain of 12.4–14.5 dB within the bandwidth and good input matching with a power dissipation of 9 mW. NF ranges from 4.2 to 5.4 dB in 3.1–10.6 GHz. The effectiveness of our design is supported by the experiment results. To the authors' knowledge, this is the first low-noise amplifier for a full-band (3.1–10.6 GHz) UWB using the CMOS process reported in domestic literature.

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