Capacitance–voltage characterization of fully silicided gated MOS capacitor*

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Abstract: This paper investigates the capacitance–voltage (C–V) measurement on fully silicided (FUSI) gated metal-oxide-semiconductor (MOS) capacitors and the applicability of MOS capacitor models. When the oxide leakage current of an MOS capacitor is large, two-element parallel or series model cannot be used to obtain its real C–V characteristic. A three-element model simultaneously consisting of parallel conductance and series resistance or a four-element model with further consideration of a series inductance should be used. We employed the three-element and the four-element models with the help of two-frequency technique to measure the Ni FUSI gated MOS capacitors. The results indicate that the capacitance of the MOS capacitors extracted by the three-element model still shows some frequency dispersion, while that extracted by the four-element model is close to the real capacitance, showing little frequency dispersion. The obtained capacitance can be used to calculate the dielectric thickness with quantum effect correction by NCSU C–V program. We also investigated the influence of MOS capacitor's area on the measurement accuracy. The results indicate that the decrease of capacitor area can reduce the dissipation factor and improve the measurement accuracy. As a result, the frequency dispersion of the measured capacitance is significantly reduced, and real C–V characteristic can be obtained directly by the series model. In addition, this paper investigates the quasi-static C–V measurement and the photonic high-frequency C–V measurement on Ni FUSI metal gated MOS capacitor with a thin leaky oxide. The results indicate that the large tunneling current through the gate oxide significantly perturbs the accurate measurement of the displacement current, which is essential for the quasi-static C–V measurement. On the other hand, the photonic high-frequency C–V measurement can bypass the leakage problem, and get reliable low-frequency C–V characteristic, which can be used to evaluate whether the full silicidation has completed or not, and to extract the interface trap density of the SiO_2/Si interface.

Key words: FUSI; C–V; photonic high-frequency C–V; MOS capacitor model
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1. Introduction

As the dimensions of complementary metal-oxide-semiconductor (CMOS) devices are continuously scaled down in order to improve speed and performance, tunneling leakage current through SiO_2/SiON, increasing exponentially, becomes a major contribution to the static power consumption. Thus, SiO_2/SiON gate dielectric has to be replaced by high-k dielectrics in 45 nm technology node and beyond. On the other hand, poly-Si gates also should be replaced by metal gates in such devices in order to avoid poly-Si depletion effects and the compatibility problems between poly-Si gates and high-k dielectrics, such as Fermi level pinning and mobility degradation[1–6]. Fully silicided (FUSI) gate has been proposed and investigated extensively due to its large work function (WF) modulation and excellent compatibility with the conventional CMOS field effect transistor fabrication process[1–6].

Capacitance–voltage (C–V) measurement is a fundamental characterization technique for MOS devices. Accurate determination of device capacitance is crucial to the measurement of equivalent oxide thickness, inversion layer charge, interface trap density, channel carrier mobility, and channel length and other electrical characteristics of MOS field effect transistors[7, 8].

The leakage current increases exponentially when the gate dielectric thickness is reduced to a quantum mechanical regime. The usual parallel/series models result in some systematic measurement errors. Even the three-element model simultaneously consisting of parallel conductance and series resistance cannot be used to extract the capacitance accurately[7, 9]. So, the four-element model with further consideration of series inductance due to extension cables and the probing system was proposed to extract the true value of the capacitance[8, 10]. The true capacitance can then be used to calculate the dielectric thickness with quantum effect correction by NCSU C–V program[11]. On the other hand, the low-frequency C–V measurement is another important characterization method for an MOS capacitor, especially for the study of poly-Si depletion effects and the SiO_2/Si interface trap

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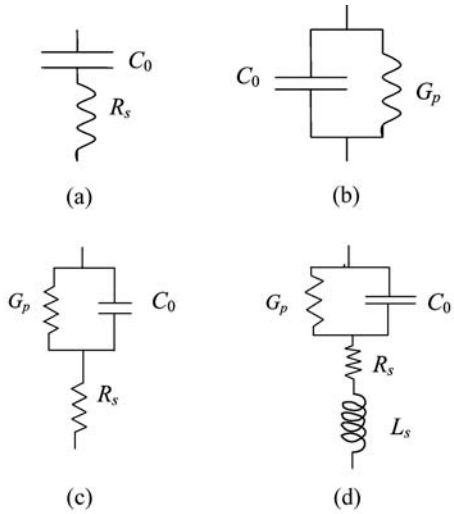

Fig. 1. Equivalent circuit models for an MOS capacitor: (a) Two-element series model; (b) Two-element parallel model; (c) Three-element model; (d) Four-element model.

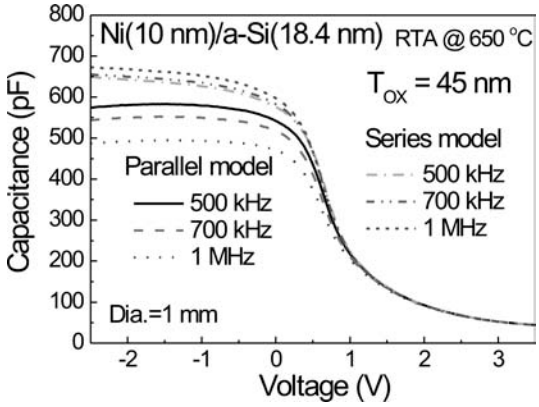

Fig. 2. High-frequency *C–V* curves acquired at 500, 700, and 1000 kHz by the two-element series and parallel model.

density. However, for extremely thin oxides, the leakage current will be added to the displacement current which is essential for the capacitance measurement. Although high-frequency *C–V* measurement of MOS transistor can be alternatively used for the low-frequency *C–V* curve acquisition for a thin leaky gate dielectric, it needs much more process steps. Therefore, a new efficient measurement technique is required.

This paper investigates the applicability of the MOS capacitor models, influence of MOS capacitor area on the *C–V* measurement, and the photonic high-frequency *C–V* measurement on Ni FUSI gated MOS capacitors.

2. MOS capacitor measurement

2.1. MOS capacitor models

Figures 1(a) to 1(d) show the four equivalent circuit models for an MOS capacitor: two-element series model, two-element parallel model, three-element model, and four-element model, respectively. Generally an impedance analyzer can measure a complex impedance with real and imaginary parts, which can be interpreted ideally by either series (completely electrically isolated) or parallel (completely free of series resistance) two-element model. However, a real MOS capacitor always has leakage current and series resistance simultaneously. In the case where both parallel conductance and series resistance are significant, a simple two-element model, either series or parallel, will result in measurement errors. The three-element model with capacitance, parallel conductance and series resistance as shown in Fig. 1(c) can be then used to extract the true value of the MOS capacitance by two-frequency or multi-frequency technique[7, 9]. However, the three-element model was also shown to be dependent on the leakage current, the two frequencies adopted, and the device area[8]. As a result, the electrical parameter of the oxide layer may not be extracted accurately[8, 9]. So, the four-element model with further consideration of series inductance as shown in Fig. 1(d) should be used[8, 10]. In this four-element model, C_0 is the real dielectric capacitance, G_p is the parallel conductance due to the gate leakage current, R_s is the series resistance due to well/substrate and contact resistance, and L_s is the series inductance due to extension cables and the probing system[8, 12].

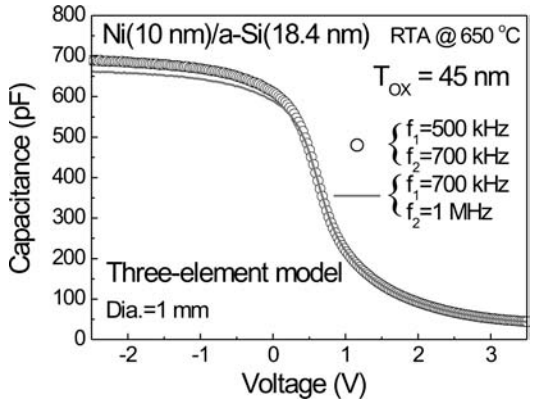

Fig. 3. High-frequency *C–V* curves extracted by the three-element model with the two-frequency technique.

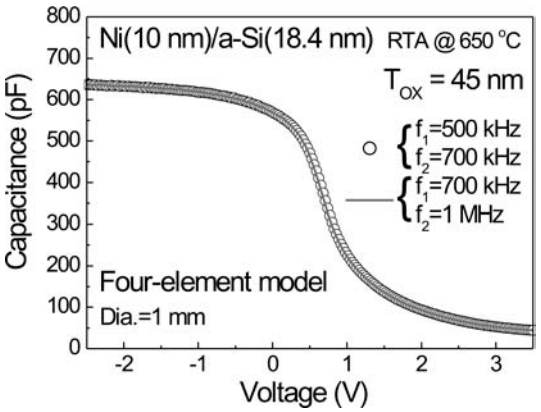

Fig. 4. High-frequency *C–V* curves extracted by the four-element model with the two-frequency technique.

The impedance of the two-element parallel model in Fig. 1(b) is given by

$$Z = \frac{1}{G_\mathrm{p}^\mathrm{m} + \mathrm{j}\omega C_\mathrm{p}^\mathrm{m}}. \tag{1}$$

The impedance of the four-element model in Fig. 1(d) is given by

$$Z = \frac{1}{G_\mathrm{p} + \mathrm{j}\omega C_0} + \mathrm{j}\omega L_\mathrm{s} + R_\mathrm{s}. \tag{2}$$

Equating the real and imaginary parts of the measured impedance (1) and the modeled impedance (2), one can obtain

$$\frac{G_{\rm p}^{\rm m}}{(G_{\rm p}^{\rm m})^2+\omega^2(C_{\rm p}^{\rm m})^2}=R_{\rm s}+\frac{R_{\rm p}}{1+\omega^2\left(C_0R_{\rm p}\right)^2} \tag{3}$$

$$\frac{C_{\rm p}^{\rm m}}{(G_{\rm p}^{\rm m})^2+\omega^2(C_{\rm p}^{\rm m})^2}=-L_{\rm s}+\frac{C_0R_{\rm p}^2}{1+\omega^2\left(C_0R_{\rm p}\right)^2}. \tag{4}$$

The two-frequency technique to analyze the three-element model[7] can also be used to analyze the four-element model[8]. The two-frequency technique measures capacitance and conductance at two different frequencies ω_1 and ω_2, which can be substituted into Eqs. (3) and (4) to get four equations. Solving the four equations, one can obtain the product of the dielectric capacitance C_0 and the parallel resistor $R_{\rm p}$:

$$C_0R_{\rm p}=\frac{C_1\left(G_2^2+\omega_2^2C_2^2\right)-C_2\left(G_1^2+\omega_1^2C_1^2\right)}{G_1\left(G_2^2+\omega_2^2C_2^2\right)-G_2\left(G_1^2+\omega_1^2C_1^2\right)}, \tag{5}$$

where C_1 and G_1 refer to the values measured at the frequency ω_1, while C_2 and G_2 refer to the values measured at the frequency ω_2.

The parallel resistor can be calculated by the following equation with the obtained $C_0R_{\rm p}$:

$$R_{\rm p}=\frac{\left[1+\omega_1^2\left(C_0R_{\rm p}\right)^2\right]\left[1+\omega_2^2\left(C_0R_{\rm p}\right)^2\right]}{\left(\omega_1^2-\omega_2^2\right)\left(C_0R_{\rm p}\right)^2}\left[\frac{G_2}{G_2^2+\omega_2^2C_2^2}-\frac{G_1}{G_1^2+\omega_1^2C_1^2}\right]. \tag{6}$$

Once $C_0R_{\rm p}$ and $R_{\rm p}$ are calculated, C_0 can be calculated. In addition, the parallel conductance $G_{\rm p}$, series resistance $R_{\rm s}$, and series inductance $L_{\rm s}$ can be obtained by

$$G_{\rm p}=\frac{1}{R_{\rm p}} \tag{7}$$

$$R_{\rm s}=\frac{G_1}{G_1^2+\omega_1^2C_1^2}-\frac{R_{\rm p}}{1+\omega_1^2\left(C_0R_{\rm p}\right)^2} \tag{8}$$

$$L_{\rm s}=\frac{C_0R_{\rm p}^2}{1+\omega_1^2\left(C_0R_{\rm p}\right)^2}-\frac{C_1}{G_1^2+\omega_1^2C_1^2}. \tag{9}$$

2.2. Experimental application of capacitor models

MOS capacitors were fabricated on an n-type Si (100) substrate with a doping concentration of 5×10^{14} cm^{-3}. After the standard RCA cleaning and the treatment with diluted HF, ~45 nm thick thermal oxide was grown by dry oxidation. 18.4 nm thick a-Si and 10 nm thick Ni film was deposited by ion beam sputtering onto the grown oxide film with a circular shadow mask. The diameter of the formed capacitor is 1 mm. Silicidation process was performed by rapid thermal anneal (RTA) at 650 °C in N_2 for 90 s. High-frequency C–V measurements were done by Agilent 4294A precision impedance analyzer at different frequencies between 400 kHz and 1 MHz.

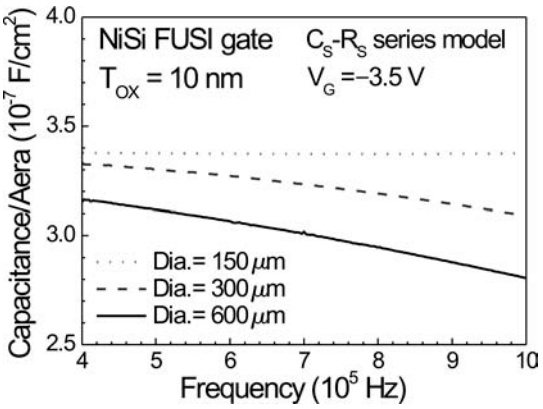

Fig. 5. Frequency dispersion of the capacitance per unit area of three MOS capacitors with a diameter of 600, 300, and 150 μm measured at a fixed gate voltage $V_{\rm G}=-3.5$ V and acquired by the two-element series model.

Figure 2 shows the high-frequency C–V curves acquired at 500, 700, and 1000 kHz by the two-element series and parallel models. The accumulation capacitances of the two-element series and parallel models are frequency-dependent and different from each other obviously. And the capacitance of the two-element parallel model decreases in the strong accumulation region, which might be related to the imperfect quality of the oxide, high temperature anneal, incompleted silicidation, therefore large leakage current and series resistance. In short, neither the series nor the parallel two-element model can be used to extract the MOS capacitor accurately.

Figure 3 shows the high-frequency C–V curves extracted by the three-element model with the two-frequency technique. From Fig. 3, it can be seen that the corrected C–V curves of 500–700 kHz and 700 kHz–1 MHz still disperse in the accumulation region, indicating that further inclusion of the series inductance may be needed for the accurate extraction of the true value of the capacitance.

Figure 4 shows the high-frequency C–V curves extracted by the four-element model with the two-frequency technique. From Fig. 4, it can be seen that the corrected C–V curves of 500–700 kHz and 700 kHz–1 MHz are in excellent agreement in the whole bias range. The results prove that the four-element model with consideration of the parallel resistance, series resistance, and series inductance can eliminate the frequency dispersion of the measured capacitance, and extract the capacitance accurately.

2.3. Influence of capacitor area on C–V measurements

In order to minimize the frequency dispersion of measured capacitance and extract the true value of the capacitance more conveniently, we further investigated the influence of MOS capacitor area on the C–V measurement.

The starting material was a p-type Si (100) substrate with a resistivity of 6–10 Ω·cm. A 10 nm thick thermal oxide was grown by dry oxidation, and 110 nm undoped poly-Si film was deposited by low-pressure chemical vapor deposition onto the grown oxide film. Then, the wafer received a spike activation anneal at 1050 °C in N_2. After native oxide was removed

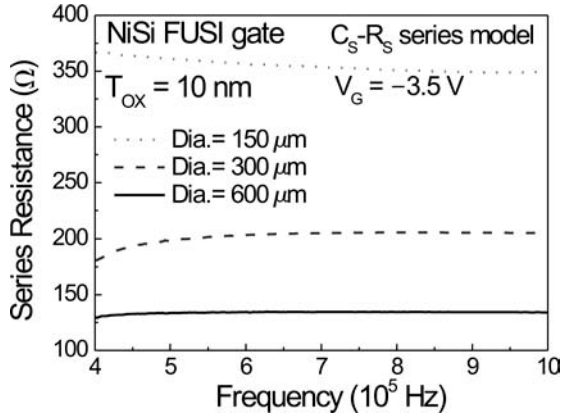

Fig. 6. Frequency dependence of the series resistance of the MOS capacitors with a diameter of 600, 300, and 150 μm measured at a fixed gate voltage V_G = −3.5 V and acquired by the two-element series model.

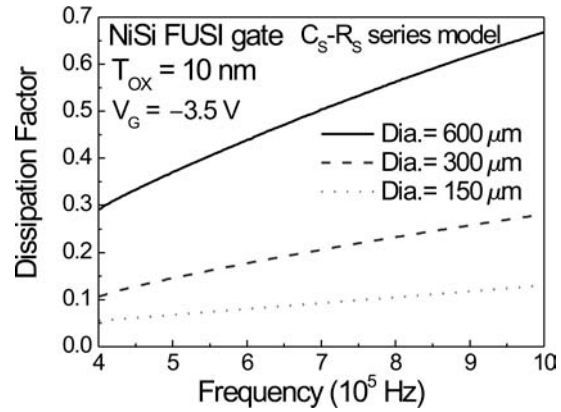

Fig. 7. Frequency dependence of the dissipation factor of three MOS capacitors with a diameter of 600, 300, and 150 μm measured at a fixed gate voltage V_G = −3.5 V and acquired by the two-element series model.

by diluted HF, 76 nm Ni was deposited on poly-Si by ion beam sputtering. The silicidation process was performed by RTA at 510 °C in N_2 for 90 s. Un-reacted metals were selectively etched by sulfuric peroxide mixture (H_2SO_4 : H_2O_2 = 4 : 1). Metal gate stacks were then patterned by wet etch to form capacitors with a diameter of 600, 300, and 150 μm. High-frequency *C*–*V* measurements were done by Agilent 4294A using the two-element series model at different frequencies.

Figure 5 shows the frequency dispersion of the capacitance per unit area of three MOS capacitors with a diameter of 600, 300, and 150 μm measured at a fixed gate voltage V_G = –3.5 V and acquired by the two-element series model. It can be seen from Fig. 5 that the capacitor with a diameter of 600 μm varies with frequency significantly, while that with a diameter of 150 μm varies indistinctively. Clearly, it shows that the smaller the capacitor area, the smaller the frequency-dispersion of the measured capacitance.

Figure 6 shows the frequency dependence of series resistance of the three MOS capacitors measured at a fixed gate voltage V_G = –3.5 V and acquired by the two-element series model. It can be seen from Fig. 6 that the series resistance of the MOS capacitor acquired by the two-element series model

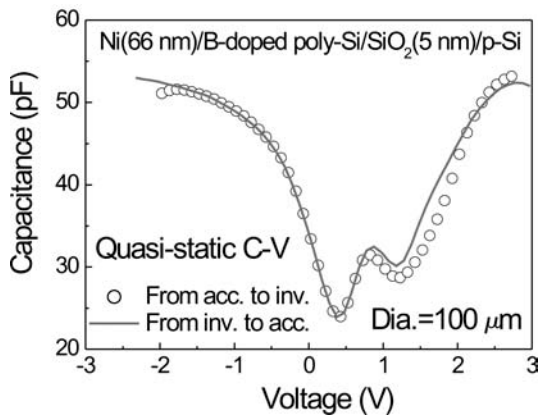

Fig. 8. Low-frequency *C*–*V* curves measured by quasi-static *C*–*V* technique, from accumulation to inversion, and sweeping reversely.

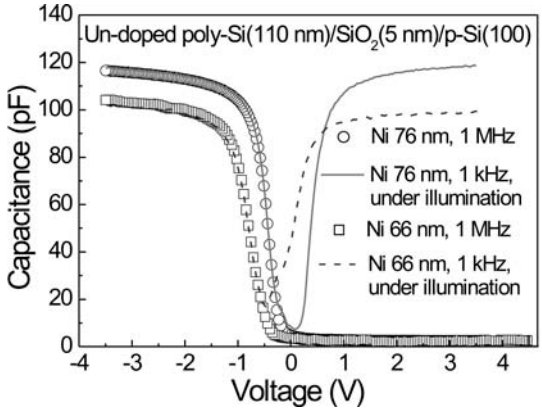

Fig. 9. High-frequency *C*–*V* curves and photonic high-frequency *C*–*V* curves for undoped Ni (76 nm) FUSI gated and undoped Ni (66 nm) incompletely silicided gated MOS capacitors.

is 130–134, 180–205, and 367–349 Ω for diameter 600, 300, and 150 μm, respectively. Due to the tunneling conductance and series inductance, the series resistance varies with the frequency. When the diameter decreases from 600 to 150 μm, the capacitance decreases by 16 times, and the parallel resistance increases by 16 times. However, the two-element series resistance only increases by 2.8–2.6 times. The series resistance is primarily a spreading resistance, which is nearly inversed to the square root of capacitor area. So the series resistance increases more slowly compared to the parallel resistance[13]. In other words, when the capacitor area decreases, the parallel resistance increases faster than series resistance. To some extent of the area reduction, the device capacitance can be well described by the two-element series model and acquired by normal single-frequency measurement.

A reliable capacitance measurement demands a small dissipation factor *D* can be written as[9]

$$D = \frac{R_s + R_p}{\omega C R_p^2} + \omega C R_s. \tag{10}$$

It can be seen from Eq. (10) that, when the frequency ω is high enough, the first item can be ignored, so *D* is linear with frequency[9].

Figure 7 shows frequency dependence of the dissipation factor *D* of the three MOS capacitors with different diameter measured at a fixed gate voltage V_G = –3.5 V and acquired by

the two-element series model. When the frequency ω is high enough, D is linear with frequency as expected above. When the diameter decreases from 600 to 150 μm, the capacitance decreases by 16 times, however, the two-element series resistance only increases by 2.8 – 2.6 times. So, the dissipation factor D of the capacitor with a diameter of 150 μm is obviously small (< 0.13), and the measured capacitance is relatively accurate. In contrast, the dissipation factor D for the diameter of 600 μm is appreciably large, 0.29 at 400 kHz, and 0.67 at 1 MHz. As a result, the measured capacitance is inaccurate in this case.

3. Photonic high-frequency *C–V* method

In order to get low-frequency C–V curve, the quasi-static measurement of an MOS capacitor and the high-frequency C–V measurement of an MOSFET are commonly used. The source and drain of an MOSFET can provide minority carriers for inversion layer. So the minority carriers can respond to an applied AC signal, and low-frequency C–V characteristic can be obtained[14]. However, the process flow of an MOSFET are much more complicated than that of an MOS capacitor, so it would be preferred to use an MOS capacitor if it works. It was also reported that the quasi-static method is susceptible to the tunneling leakage current and voltage sweep velocity[15]. Figure 8 shows the low-frequency C–V curves measured by quasi-static C–V technique, sweeping from accumulation to inversion, and sweeping reversely. When sweeping from the accumulation to the inversion, the capacitance increases along with voltage sweep direction at the beginning (strong accumulation) and at the end (strong inversion) of the sweep. However, when sweeping from inversion to accumulation, the capacitance increases along with voltage sweep direction in the strong inversion and accumulation regions. This is due to the measurement error induced by tunneling current. The real MOS capacitance C_0 and the measured capacitance $C_{\rm m}$ have the following relation[15]:

$$C_{\rm m} = C_0 + I_{\rm tunnel}\,({\rm d}V/{\rm d}t)^{-1}\,, \tag{11}$$

where $I_{\rm tunnel}$ is the tunneling current, and ${\rm d}V/{\rm d}t$ is the voltage sweep velocity. $I_{\rm tunnel}$ is defined positive from gate to substrate.

The tunneling current is large in the accumulation and inversion regions. It can be deduced form Eq. (11) that $C_{\rm m}$ is smaller than C_0 at the beginning of the sweep and larger than C_0 at the end of the sweep. The measured capacitance $C_{\rm m}$ increases along with voltage sweep direction. As a result, the measured accumulation and inversion capacitances are not accurate. So, full silicidation of the MOS capacitor with thin leakage gate dielectric cannot be verified from the quasi-static C–V curves.

As an alternative, photonic high-frequency method was proposed to measure low-frequency C–V curves[16–19]. In this work, we measured capacitance with photonic high-frequency method at 1 kHz under illumination. Figure 9 shows high-frequency C–V curves and photonic high-frequency C–V curves for undoped Ni (76 nm) FUSI gated and undoped Ni (66 nm) incompletely silicided gated MOS capacitors. As shown in Fig. 9, photonic illumination increases the capacitance values measured in the inversion region. Photonic illumination accelerates the generation of minority carriers so that the charges of the inversion layer may response to the high-frequency voltage change. In addition, the illumination also induces a decrease of the surface potential under a constant applied voltage. The decrease of the surface potential results in a decrease of the depletion width, and therefore the increase of the capacitance. Both effects increase the capacitance in the inversion region[16,20]. From Fig. 9, it can be seen that photonic high-frequency C–V characteristics show smaller inversion capacitances compared to the accumulation capacitances, indicating that the poly-Si depletion occurred for the Ni (66 nm) silicided gated MOS capacitor. Due to the Ni/Si thickness ratio variation in the process, and the nonuniformity of local silicidation rate which can be varied by more than a factor of two[1], MOS capacitor with Ni (66 nm) may not be fully silicided. In Fig. 9, photonic high-frequency C–V characteristics of the Ni (76 nm) FUSI gated MOS capacitor show that the accumulation and inversion capacitances are identical and bigger than those of Ni (66 nm) incompletely silicided gated MOS capacitor, suggesting that absence of gate depletion and full silicidation indeed occurred for the Ni (76 nm) FUSI gated MOS capacitor. High-frequency C–V characteristic of Ni (76 nm) FUSI gated MOS capacitor shows that the flat-band voltage $V_{\rm FB}$ is higher than that of the Ni (66 nm) incompletely silicided gated MOS capacitor which are actually a juxtaposition of local WFs of metal and poly-Si[1], also suggesting that the absence of gate depletion for the Ni (76 nm) FUSI gated MOS capacitor.

Furthermore, the photonic high-frequency C–V curves can also be used to measure the SiO_2/Si interface trap density[2, 6, 18].

4. Conclusion

This paper investigates the measurement of the C–V characteristic and the applicability of MOS capacitor models. The results indicate that the four-element model with consideration of the parallel resistance, series resistance and series inductance can minimize the frequency dispersion of the measured capacitance for capacitors with large leakage current. The true value of the capacitance can be used to calculate the dielectric thickness with quantum effect correction by NCSU C–V program. The reduction of capacitor area lowers the dissipation factor D, improves the measurement accuracy, and reduces the frequency dispersion of the measured capacitance. Therefore the two-element series model can be used to obtain reliable C–V characteristic curves for capacitors with small enough area. Photonic high-frequency method can eliminate the influence of the leakage current that significantly affects the quasi-static C–V measurement, and get reliable low-frequency C–V curves. Photonic high-frequency method can be used to evaluate whether the full silicidation has completed or not, and to extract the interface trap density of the SiO_2/Si interface.

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