A novel low-voltage operational amplifier for low-power pipelined ADCs

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Abstract: A novel low-voltage two-stage operational amplifier employing class-AB architecture is presented. The structure utilizes level-shifters and current mirrors to create the class-AB behavior in the first and second stages. With this structure, the transconductances of the two stages are double compared with the normal configuration without class-AB behaviors with the same current consumption. Thus power can be saved and the operation frequency can be increased. The nested cascode miller compensation and symmetric common-mode feedback circuits are used for large unit-gain bandwidth, good phase margin and stability. Simulation results show that the sample-and-hold of the 12-bit 40-Ms/s pipelined ADC using the proposed amplifier consumes only 5.8 mW from 1.2 V power supply with signal-to-noise-and-distortion ratio 89.5 dB, spurious-free dynamic range 95.7 dB and total harmonic distortion –94.3 dB with Nyquist input signal frequency.

Key words: low-voltage operational amplifier; class-AB; two-stage amplifier; low-power pipelined ADC
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1. Introduction

For the switched-capacitance circuits such as the pipelined analog-to-digital converters (ADC), the power consumption will probably increase as the supply voltage goes down, because the voltage available to represent the analog signal is reduced. Therefore, the dynamic range becomes an important issue. Both telescopic and folded-cascode op-amps are not suitable for low-voltage applications because of their small output swings. The normal two-stage op-amp needs a lot of current in the first and second stages to get a large unit-gain bandwidth, so it cannot be used for low-power design. As a result, using class-AB op-amps is essential in designing low-voltage low-power high-resolution ADCs[1,2]. In Refs. [1,2], the op-amps both utilized folded-cascode and gain-boosting in the first stage for high-gain, and class-AB in the second stage for large output swing. However, in low-voltage supply, the cascode architecture with gain-boosting is complex and difficult to design for stability. In this paper, a novel class-AB two-stage op-amp is proposed which uses class-AB, not gain-boosting, in the first stage for high-gain, lower power and simpler design compared with Refs.[1,2], and also class-AB in the second stage for large output swing. The transconductances (g_m) of the two stages are double compared with the normal configuration without class-AB behaviors with the same current consumption. With this structure, the quiescent current can be chosen to be small, and the current will be dynamically increased when needed[3,4]. Compared with the traditional cascode miller compensation[5], the proposed nested cascode miller compensation architecture saves a lot of current through eliminating a pair of cascode circuits. Thus power can be saved obviously and the operation frequency can be increased with the proposed op-amp in high-speed and high-resolution applications. The principle of the class-AB is presented. Then the novel operational amplifier is given with detailed design considerations and analysis.

2. New application of class-AB

In order to efficiently use the supply power, an output stage should combine a high maximum output current with a low quiescent current. To meet this requirement, class-B biasing can be used, whose power-efficiency is about 75% for a rail-to-rail output sine wave. However, the class-B biasing introduces a large cross-over distortion. To minimize the distortion, the class-A biasing can be employed. But the power-efficiency of the class-A biasing is only 25% for a rail-to-rail output sine wave. To achieve a good compromise between distortion and power-efficiency, an output stage has to be biased between the class-A and class-B, called class-AB biasing. The transistors are biased at a small quiescent current by a V_{gs} little above V_{th}, which decreases the cross-over distortion compared to that of class-B biased transistors[6]. The maximum output current of the output stage is much larger than its quiescent current, which increases its power-efficiency compared to that of class-A biasing. The principle of class-AB biasing is shown in Fig.1. The DC voltage V_{in1} and V_{in2} are set differently to get small V_{dsats} of M1 and M2 for a low quiescent current. If the V_{in1} has a direct relationship with V_{in2}, for example, $V_{in1} = V_{in2} + V_L$, where V_L is a voltage level-shifter, class-AB can be applied in the input stage. When the op-amp with class-AB biased input is used for switched-capacitor circuits, there are two work phases: the amplifying phase and the sampling phase. In the sampling phase, the C_{LS} is charged with

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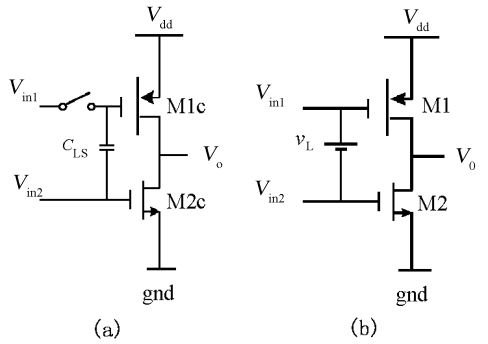

Fig.1. (a) Principle of the class-AB; (b) An implementation of switch-capacitor class-AB.

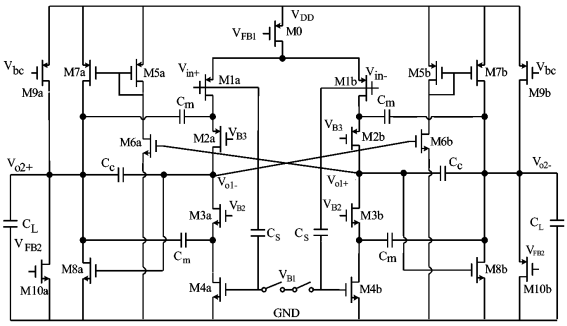

Fig.2. Novel proposed two-stage amplifier.

the voltage of the difference between V_{in1} and V_{in2} and the op-amp is idle. In the amplifying phase, the switch turns off and the PMOS current source is biased with a suitable voltage that is signal-dependent, considering the capacitor has little charge leakage. A large capacitor should be chosen to decrease the effect of the parasitic capacitor at the nod of the PMOS transistor in Fig.1 (b). In this structure, the equivalent transconductance of the stage is got as follows:

$$g_{in} = g_{m1c} + g_{m2c}. \tag{1}$$

If the V_{gs}–V_{th} of M1c is equal to that of M2c, the input transconductance is enhanced almost two times compared with the same configuration of a single stage class-A amplifier consuming the same current.

3. Proposed op-amp architecture

A novel low-voltage low-power two-stage amplifier is presented in Fig.2, which makes use of class-AB principle in both of the two stages to obtain good frequency response, fast-settling performance, large output swing and low power consumption under 1.2 V power supply. The C_S here is as large as 3 pF to minimize the parasitic capacitance effect in the gate of M4. Through making the overdrive voltages of M1 and M4 equal, the input transistor transconductance is

$$g_{m,input} = g_{m1} + g_{m4} = 2g_{m1}. \tag{2}$$

The output transistor transconductance becomes

$$g_{m,output} = g_{m8} + g_{m7}g_{m6}/g_{m5}. \tag{3}$$

By choosing $(W/L)_6/(W/L)_8$ equal to $(W/L)_5/(W/L)_7$, the $g_{m,output}$ is easily designed to be $2g_{m8}$[5]. So the transconductance

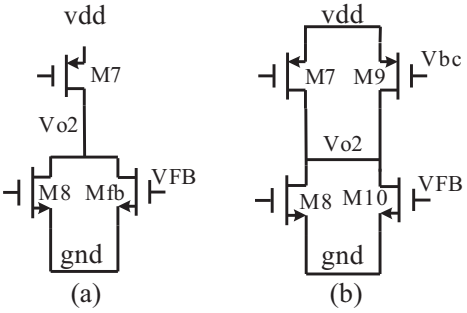

Fig.3. Two ways to realize the CMFB of the output class-AB stage.

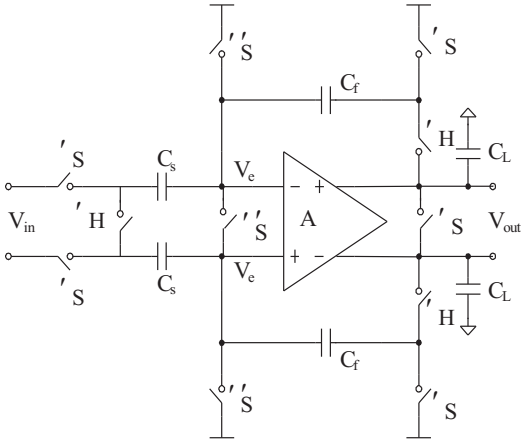

Fig.4. S/H configuration with the proposed two-stage amplifier.

is enhanced two times without increasing current. As there is a large ratio between the dynamic current and the quiescent current when the class-AB stage works, the transconductance of the class-AB stage changes over a large range. Therefore, using the normal miller compensation or the cascode miller compensation is not enough to keep the op-amp stable. A nested cascode miller compensation is employed here to cope with the headache problem and a very good frequency response is reached by this method[6]. Compared with the traditional low-voltage two-stage op-amp with cascode miller compensation, the proposed architecture saves current through eliminating a pair of cascode circuits[5]. So a lot of power is saved by the proposed op-amp. The location of the poles and zeros of the proposed amplifier is given as follows:

The dominant pole P_1 is located at

$$p_1 = -\frac{1}{r_{o1}r_{o2}g_{m2}g_{m8}r_{o8}(c_m + c_c)}. \tag{4}$$

The place of the first non-dominant pole P_2 is at:

$$p_2 = -\frac{g_{m8}}{(c_m + c_L)\left(1 + \dfrac{c_{g8}}{c_c}\right)}\frac{c_m + c_c}{c_c}, \tag{5}$$

where c_{g8} is the total parasitic capacitance at the gate of transistor M8a, which is equal to the transistor M8b.

The second non-dominant pole P_3 is at

$$p_3 = -g_{m3}\frac{c_m + c_L}{c_L}. \tag{6}$$

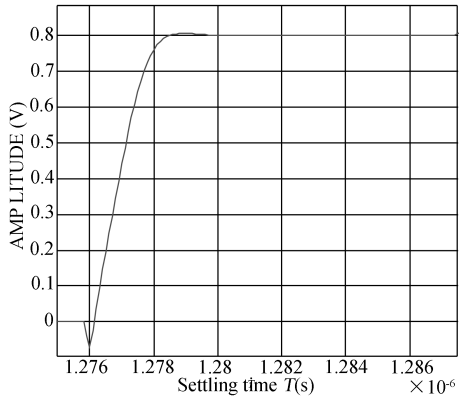

Fig.5. Simulated op-amp step response.

The unity-gain frequency, which is equal to Gain Bandwidth (GBW), should be set at $\frac{1}{3}P_2$ for a good phase margin consideration[3], thus,

$$\mathrm{GBW} = \frac{2g_{\mathrm{m1}}}{c_{\mathrm{m}} + c_{\mathrm{c}}} = \frac{1}{3}P_2. \tag{7}$$

An additional zero is at a frequency of

$$Z = -\left(\frac{g_{\mathrm{m3}}}{c_{\mathrm{m}}} + \frac{g_{\mathrm{m3}}}{c_{\mathrm{c}}}\right). \tag{8}$$

The minimum damping of the system ζ_{min} is given here:

$$\zeta_{\mathrm{min}} \approx \sqrt{\frac{c_{\mathrm{m}}}{c_{\mathrm{m}} + c_{\mathrm{c}}}}. \tag{9}$$

From the above Eq.(9), the damping of the circuit is always larger than 0.7 when the value of c_{m} is larger than that of c_{c}, which means that peaking will never occur[6]. Here c_{m} is chosen two times as large as c_{c} for a larger GBW consideration.

Another important issue to be considered is the common-mode feedback of the proposed op-amp. As the output common-mode levels of two stages in the proposed op-amp are set independently, two independent common-mode feedback (CMFB) circuits are needed to define the common-mode voltages at the outputs of the first and second stages. The CMFB circuit is adopted with a symmetric switched capacitor network[7], which has more merits, such as faster DC settling, lower steady-state errors, charge injection errors and leakage errors, compared with the traditional simple switched capacitor network[5]. In the second stage, the output common-mode voltage is used to control two added common source amplifiers, M9a, M10a and M9b, M10b, that drive the output nodes to keep the output common-mode voltage stable. There are usually two ways to control the output common-mode voltage[2,8], which are shown in Fig.3. In the way shown in Fig.3 (a), the transconductance of M7 is larger than M8 with the equal V_{dsat} because the current in Mfb must go through M7. However, in the circuit provided by Fig.3.(b), the current through the feedback transistor M10 is mainly generated by M9 which is biased with dedicated voltage V_{bc}. So the

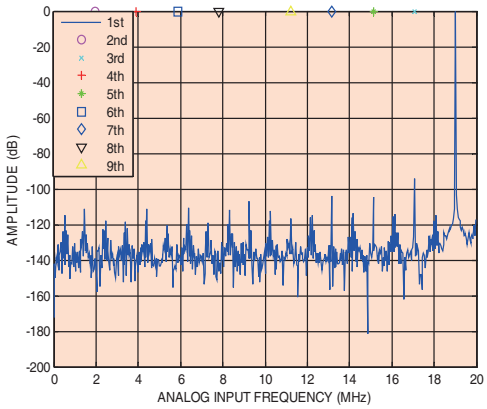

Fig.6. FFT performance of the S/H with a nyquist-frequency full-swing input.

Table 1. Performance comparison between different configurations of the op-amp output stage CMFB.

Configuration of the output stage CMFB	SFDR	THD(dB)
With Fig.3 (a)	87.2	−85.9
With Fig.3 (b)	95.7	−94.3

Table 2. Performance comparison of different class-AB op-amps.

Parameter	This work	Ref.[1]	Ref.[5]
Process (μm)	0.18	0.09	0.25
Power supply voltage (V)	1.2	1.0	1.5
DC gain (dB)	85	74	80
Phase margin	68	/	73.5
Settling time (ns)	6 (0.005%)	/	7.1 (0.01%)
Output swing V_{pp} (V)	1.6	1.5	1.13
Unity gain bandwidth (MHz)	481	1000	167
Load (pF)	3	/	4
Power consumption (mW)	5.8	34	8.9

transconductance of M7 is almost equal to that of M8, which is very useful for enhancing the THD and SFDR of the op-amp. From Table 1, the THD and SFDR of the op-amp with Fig.3 (b) configuration in the output stage are more than 8 dB better than that of the one with Fig.3 (a) configuration. In order to have a good stability and a quick feedback operation, the added common source amplifier for the second stage CMFB should consume at least one fifth of the current through the second stage. It is really a large amount, but for large bandwidth and high speed consideration it is worthwhile.

4. Simulation results

In a TSMC 0.18 μm CMOS process, the proposed op-amp is simulated with HSpice in all process corners with good performances. Under TT 75 ° C, the proposed op-amp of Fig.1 showns 85 dB DC gain, 1.6-$V_{\mathrm{p\text{-}p,diff}}$ output swing, 481 MHz

unity-gain bandwidth with 68° phase margin with feedback factor of 0.5 when driving 3 pF load, totally consuming 5.8 mW from 1.2 V power supply voltage. Table 2 gives the performance comparison of different class-AB op-amps, among which the proposed op-amp is the most efficient one in power dissipation. The step response of the op-amp is given in Fig.5 with the S/H configuration in Fig.4. A 0.005% precision can be reached in 6 ns, which is enough for 12 b 40 MHz pipelined ADC. With a nyquist-frequency full-swing input, the FFT performance of the S/H in Fig.6. shows SNDR 89.5 dB, SFDR 95.7 dB and THD −94.3 dB.

5. Conclusions

In this paper, a new approach leading to a low-voltage, low-power, and fast-settling op-amp is presented. By employing class-AB biasing in both of the input and output stages and the proposed nested cascode compensation, the proposed op-amp has large unit-gain bandwidth, good phase margin, fast-settling behavior and large output swing. The proposed op-amp is applied to the S/H of a 12 b 40 MHz pipelined ADC as an example to demonstrate very good performance and power-efficiency in high-speed switched-capacitor applications.

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