A low-power monolithic CMOS transceiver for 802.11b wireless LANs*

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Abstract: A single-chip low-power transceiver IC operating in the 2.4 GHz ISM band is presented. Designed in 0.18 μm CMOS, the transceiver system employs direct-conversion architecture for both the receiver and transmitter to realize a fully integrated wireless LAN product. A sigma-delta ($\Sigma\Delta$) fractional-N frequency synthesizer provides on-chip quadrature local oscillator frequency. Measurement results show that the receiver achieves a maximum gain of 81 dB and a noise figure of 8.2 dB, the transmitter has maximum output power of -3.4 dBm and RMS EVM of 6.8%. Power dissipation of the transceiver is 74 mW in the receiving mode and 81 mW in the transmitting mode under a supply voltage of 1.8 V, including 30 mW consumed by the frequency synthesizer. The total chip area with pads is 2.7×4.2 mm^2.

Key words: WLAN; direct-conversion; low power; RF CMOS; transceiver
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1. Introduction

Wireless LANs (WLANs) are currently seeing significant growth in the worldwide consumer electronics market. The high data rate (11 Mbps) WLAN standard IEEE 802.11b[1] in unlicensed 2.4 GHz ISM band is the most popular one. With more handheld devices such as PDA and IP phones integrated with the WLAN function, the low power design of the wireless transceiver chip is becoming critically important in order to increase battery life. On the other hand, realizing a high level of integration in low-cost CMOS technology is desirable to reduce the manufacturing cost.

A monolithic CMOS 802.11b transceiver with low power consumption is presented in this paper. The transceiver architectures and system level design issues are discussed. A detailed circuit design is given, but only the receiver and the frequency synthesizer will be covered, readers may refer to Ref.[2] for more information on the transmitter.

2. Transceiver architecture

The wideband nature of the WLAN signal and the time division duplex (TDD) mode enables the use of direct conversion architecture, so the cost and size of the overall transceiver are reduced, as well as the total power consumption. The block diagram of the proposed transceiver system is shown in Fig.1. All signal paths are realized differentially to suppress even order distortion and common mode noises.

The receiver consists of an LNA with two-step gain control, followed by a quadrature demodulator directly down converting the RF signal into I and Q channel baseband signals. LPFs are used to provide sufficient attenuation to the adjacent channel that transforms into an interferer due to aliasing from ADC sampling. Variable gain amplifiers (VGA) guarantee that ADC sees a proper signal level at the receiver output. DC-offset and $1/f$ noise are suppressed in the analog baseband by DC feedback loops. In order to satisfy the sensitivity and adjacent channel blocker requirement in 802.11b PHY standard [1], the receiver should provide a large amount of gain and dynamic range, which requires design trade-off between noise and distortion. A system level calculation is performed to find an optimal partition of noise and distortion among the receiver stages.

The transmitter consists of a reconstruction filter and VGA in each I and Q channel. VGA control the signal level at input of the up-conversion mixer, so that the mixer can have the best dynamic range performance. Meanwhile it also provides the power control ability of the RF output power. A highly linear single side-band (SSB) mixer directly converts baseband signals into carrier frequency, and PA driver (PAD) amplifies the RF signal to a level suitable for an off-chip PA. System level analysis is also performed to determine the block

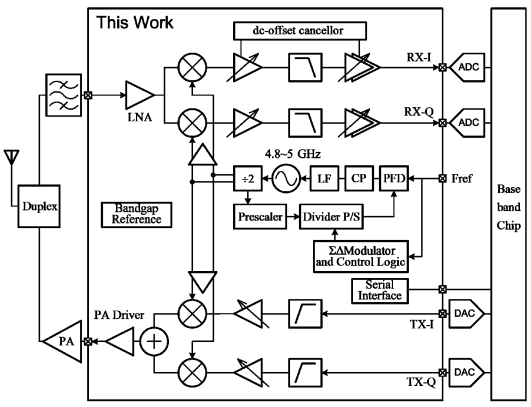

Fig.1. Transceiver architecture.

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Table 1. Main specification summary.

RX gain	> 80 dB	TX output power	0 dBm
RX noise figure	< 11 dB	TX output must meet spectrum mask requirement	
RX IIP3	>−15 dBm	TX Peak EVM	< 35%
RX VGA range	60 dB	RX/TX LPF	4th Chebyshev, f_{-3dB}= 9 MHz
Synthesizer phase noise	in-band integrated PN<−33 dBc, out-band PN<−127 dBc/Hz		

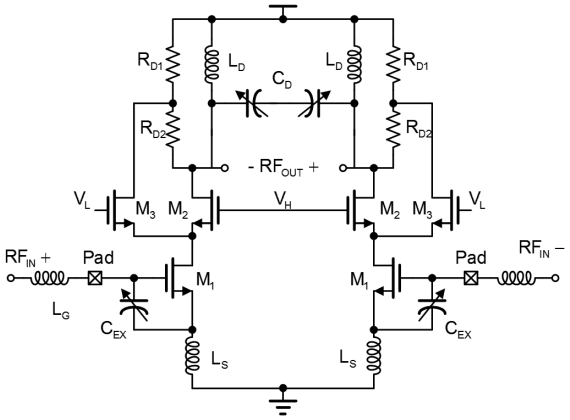

Fig.2. Proposed differential LNA.

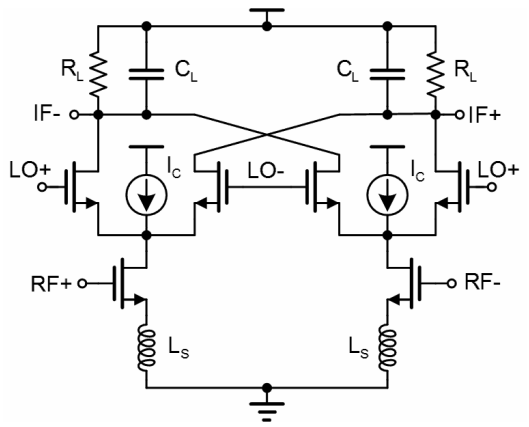

Fig.3. Down-conversion mixer.

specification in the transmitter, so that the EVM and spectrum mask requirements are met.

A ΣΔ fractional-N frequency synthesizer is integrated for on-chip LO generation. It utilizes a phase-locked loop (PLL) and a digital ΣΔ modulator to obtain the desired frequency range and channel spacing. Due to the adopted direct-conversion transmitter architecture, VCO is oscillating at twice the carrier frequency to avoid LO pulling. Quadrature LO signals are generated by a divide-by-two circuit, buffered and sent to mixers in the receiver and transmitter, respectively. The design challenge of the frequency synthesizer comes from rigorous requirements on phase noise and spurs. The in-band phase noise and spurs of PLL will be converted to noise and distortion in the signal band during the progress of frequency mixing, degrading SNR of the receiver and EVM of the transmitter, while the out-band phase noise and spurs, on the other hand, will cause spurious emission compromising the spectrum mask requirement of the transmitter. The main transceiver design specifications derived from system level analysis are summarized in Table1. Supporting circuitry such as bandgap reference and serial-parallel interface (SPI) are also integrated on-chip to minimize the number of off-chip components. Receiver gain and channel bandwidth, transmitter output power level and channel bandwidth as well as synthesizer channel selection can all be programmed by registers through SPI. This alleviates the need for extra IO pads for numerous control signals.

3. Circuit design

3.1. Receiver

As the most critical building block in the RF receiver, the proposed differential LNA is shown in Fig.2. A power constrained simultaneous noise and input matching (PCSNIM)[3] technique is adopted to minimize the power dissipation. A classic source degenerated LNA design, as concluded in Ref.[4], also targets simultaneous noise and impedance matching with power constraints. However, due to the inverse proportional relationship between C_{gs} of the input transistor and the degeneration inductor L_S, such an approach leads to a large L_S value in a low power design, where the transistor size is kept small, i.e. C_{gs} is small. Large L_S results in high F_{min} and low voltage gain. As proposed in Ref.[3], the dependency of L_S on C_{gs} can be decoupled by inserting an extra capacitor C_{EX} between the gate and source terminal of the input transistor, achieving PCSNIM. Input impedance of LNA thus is given by

$$Z_{in} = sL_G + \left(sL_S + \frac{1}{s\left(C_{EX} + C_{gs}\right)} + \frac{g_m L_S}{C_{EX} + C_{gs}} \right) // \frac{1}{sC_P}, \quad (1)$$

where L_G includes the off-chip matching inductor and bond-wire inductance, and C_P is the parasitic capacitance contributed from the ESD diode, pad and PCB trace. To account for the uncertainty in values of C_P, C_{EX} is adjustable by using a switchable capacitor bank, so that the real part of Z_{in} can be tuned to match the 50 Ω source reliably.

LNA gain setting is necessary to avoid saturation because 802.11 specifies the maximum input level of –10 dBm. Gain setting is realized by a separate high/low gain path in the cascode stage, whose loading impedance is different. The loading capacitor is also digitally programmable to tune the resonating frequency of the LC tank into the desired band. Simulation results show that the differential LNA achieves a noise figure of 1.2 dB, a voltage gain of 22 dB in the high gain mode and 0 dB in the low gain mode, and only consumes a current of 4 mA.

The down-conversion mixer is shown in Fig.3. The current bleeding Gilbert mixer with inductive source degeneration is adopted. Noise free inductor degeneration improves

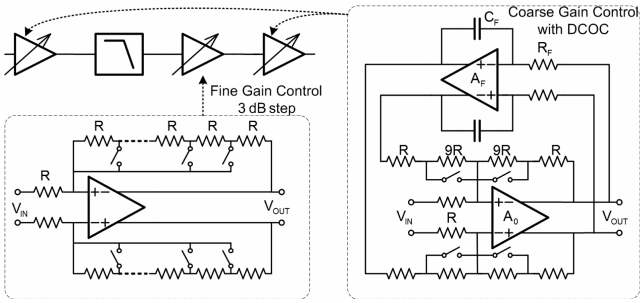

Fig.4. Analog baseband and VGA with DCOC.

the mixer's linearity. DC current injection allows the freedom to bias the transconductance stage and switching quad separately. With less DC current flowing through the switching transistors, the noise contribution especially $1/f$ noise from these transistors can be effectively reduced[5]. Current injection also helps to compensate for the mixer conversion gain, which is degraded due to the source degeneration. A first order passive RC low-pass filter is composed at the mixer output, to help attenuate out-band interferers before baseband amplification without extra power consumption. The mixer has a conversion gain of 5 dB, a noise figure of 15 dB and a IIP_3 of 10 dBm, and consumes about 3.5 mA current for two I/Q channels.

Due to the wide signal bandwidth (11 MHz) and dynamic range requirement, analog baseband circuits with two IQ channels are even more power hungry than the RF front-end in the receiver design. Our low power design strategy is to identify the key performance requirement of each block and apply optimization individually. Figure 4 shows the proposed baseband channel, the total variable gain range is distributed in 3 VGA stages. Fine gain control is realized in the second VGA with 3 dB linear-decibel steps, which is designed to guarantee feedback stability, because resistors and switches in the feedback path form a distributed RC network and introduce excess phase shift. The first and last VGA stages realize coarse gain control with a 20 dB step. Since less phase shift appears in the feedback path, the phase margin requirement of opamp can be relaxed to save power. Furthermore, because the RF front-end only provides moderate gain, the first VGA should be optimized for low noise. An opamp-RC 4th order Chebyshev low-pass filter for channel selection is placed after the first VGA, with addition gain before LPF, a higher noise level of the active filter can be tolerated. The last VGA is designed to drive large off-chip loading so extra buffer amplifiers can be saved. To sum up, careful arrangement and optimization of each block result in an overall optimal design with low power consumptions.

DC-offset is a major disadvantage in direct-conversion receivers, although balanced circuits are used, DC-offset may still appear from device mismatch and LO leakage[6]. DC-offset cancellers (DCOC) around the first and the last VGA are used to suppress DC-offset and low frequency $1/f$ noises, as shown in Fig.4. Assuming ideal opamp, the transfer function of VGA with DC feedback can be simplified as

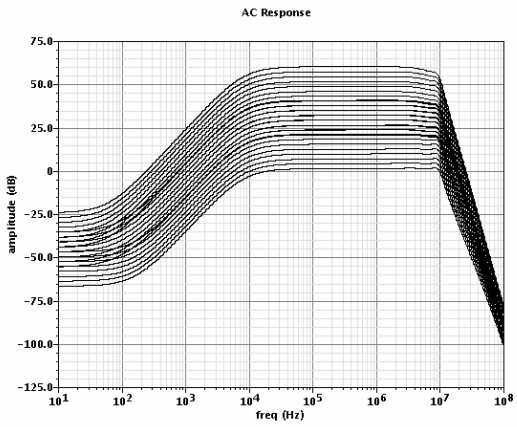

Fig.5. AC response of the analog baseband.

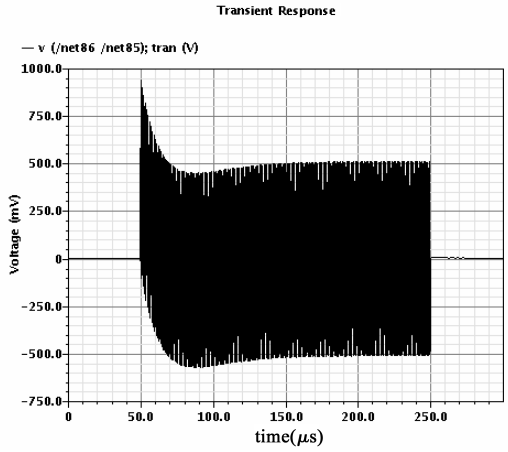

Fig.6. DCOC settling transient.

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\frac{R_2}{R_1}\frac{sR_{\mathrm{F}}C_{\mathrm{F}}R_3/R_2}{1+sR_{\mathrm{F}}C_{\mathrm{F}}R_3/R_2},$$

where R_1 is the value of the VGA input resistor, R_2 is the VGA feedback resistor and R_3 is the value of another VGA input resistor connected to the DC feedback loop. As long as R_3 and R_2 are matched, the DC feedback realizes a high-pass transfer function with constant cutoff frequency determined by R_{F} and C_{F}. Since R_2 needs to be switched for different gain settings, R_3 should be changed accordingly. Another issue related to DCOC is the settling time. Since HPF cutoff frequency should be low enough not to deteriorate the received signal, a large time constant in the DC feedback may cause a long transient when VGA gain is changed. We propose to apply an adaptive biasing technique in the DC feedback amplifier to boost its slew rate. The class AB style output can rapidly charge/discharge the integrating capacitor C_{F} when VGA gain is switched. While the DCOC loop is stabilized, quiescent biasing current is kept at a low level for power saving.

Figure 5 shows the AC simulation results of the analog baseband, 60 dB gain range with a 3 dB step can be achieved. The nominal cutoff frequency of LPF is 9 MHz, and can be adjusted in the ±30% range to account for process variation.The HPF cutoff frequency of DCOC is around 10 kHz and is independent of the VGA gain setting. Figure 6 shows the baseband

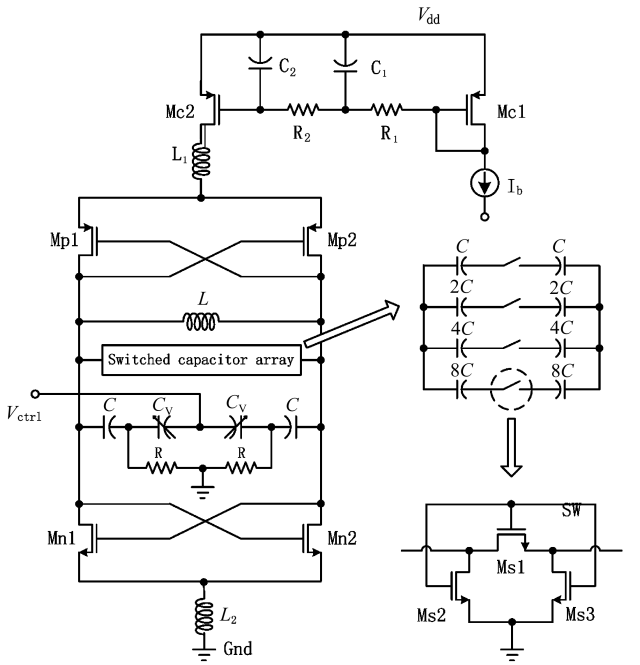

Fig.7. Schematic of the VCO.

transient response, the worst transient with a gain step of 60 dB is 0.25 μs and DCOC settled within 100 μs. This result is favourably compared to the state-of-the-art[7] whose DCOC settles in 266 μs. The two baseband channels consume a current of 18 mA.

3.2. Frequency synthesizer

The LCVCO used in PLL is shown in Fig.7, in which the VCO is based on a complementary cross-coupled topology with a top pMOS current source. To sufficiently reject the noise generated by the current mirror, two series low pass RC filters (R_1, C_1 and R_2, C_2) are introduced as shown in the figure, C_1 and C_2 are realized using MOS capacitors. Two inductors (L_1 and L_2) resonating at twice the VCO frequency are inserted at the common sources of the differential pair to further prevent noises from coming into the VCO core. The LC tank consists of an on-chip differential symmetric spiral inductor and accumulation-mode MOS varactors. As shown in Fig.7, the two varactors are put in series with two fixed-value capacitors, with their common node connecting to the ground via resistors. This prevents the VCO frequency tuning range from getting too large while maintains the desired frequency. An advantage comes from a small VCO gain which is reduced sensitivity to the noise generated by other PLL building blocks. To further reduce the VCO gain and expand the frequency tuning range, a 4-bit switched-capacitor array in parallel with the LC tank is added. The switches shown in Fig.7 can help to minimize the quality factor degradation of the LC tank. The VCO is designed to have a frequency tuning range of 4.6–5.2 GHz to cover the desired band with an adequate margin.

The prescaler shown in Fig.8 is an inherently glitch-free 7/8 dual-modulus prescaler. It is based on an improved phase-switching technique and similar to that proposed in Ref.[8]. The phase switching is made between the 90° spaced out-

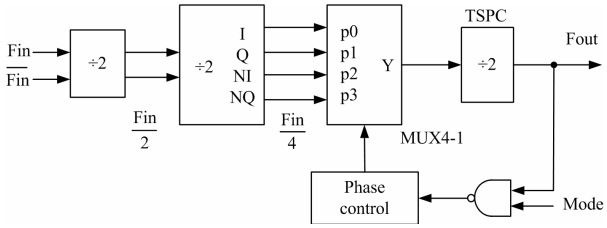

Fig.8. Block diagram of the prescaler.

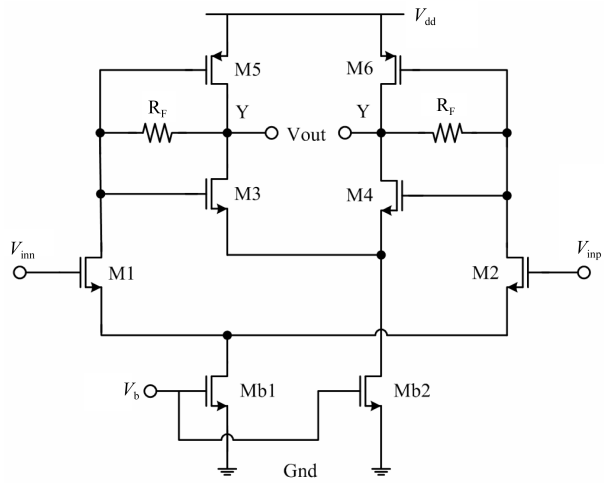

Fig.9. LO buffer.

put phases by an asynchronous divide-by-4 front stage. To reduce the power consumption and improve the robustness of this circuit, another asynchronous true single phase clock (TSPC) divide-by-two circuit is added after the multiplexer. This dynamic TSPC circuit can work at pretty high frequencies without static power consumption. The output of the VCO is followed by 3 stage divide-by-two circuits to prevent the digital logic divide circuits from working at high frequency. The function of the divide-by-2 circuit is accomplished by 2 latches based on source-coupled logic (SCL)[8]. The desired quadrature signal is also obtained at the same time. Usually, to minimize I/Q mismatch, a dummy divide-by-two circuit needs to be connected to the unused outputs of the previous divide-by-two circuit. We add the dummy divide-by-two circuit but connect its power supply to the ground to save power. Power dissipation is further reduced by proportionally scaling down the dimensions of the transistors in the cascading divide-by-two stages. The first divide-by-two stage works at a high VCO frequency of about 5 Hz and is most vulnerable, so it is AC coupled from the VCO output by an on-chip bias-T composed of the RC network. In this way we can independently bias the divide-by-two circuit to ensure its functionality.

A complementary charge pump is used, utilizing current steering and positive feedback techniques for their fast switching-speed and low charge injection errors. The passive loop filter is of 3rd order. All the capacitors used in the filter are integrated on chip. A program counter P and a swallow counter S together with the prescaler complete the function of downscaling the VCO frequency to PFD. The output is synchronized by the high frequency prescaler clock to minimize their noise to the final output.

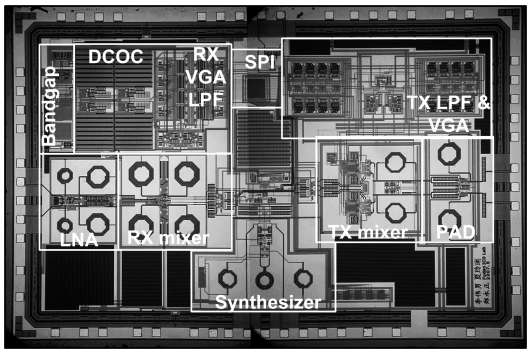

Fig.10. Transceiver chip microphotograph.

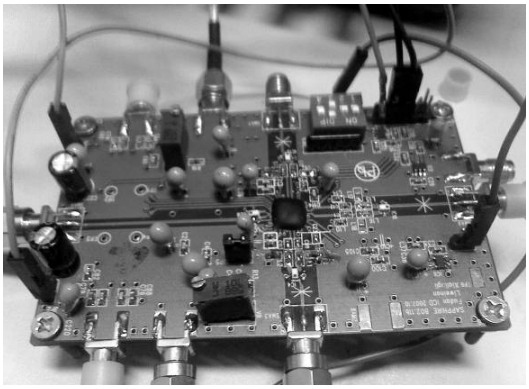

Fig.11. Test PCB.

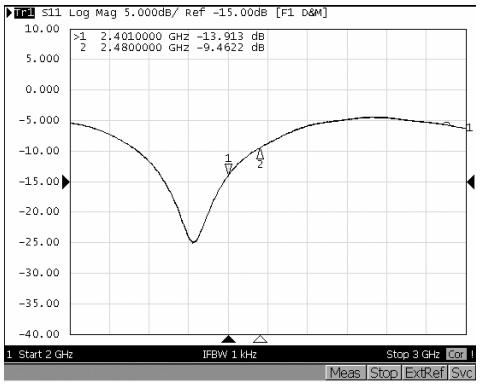

Fig.12. Measured receiver S_{11}.

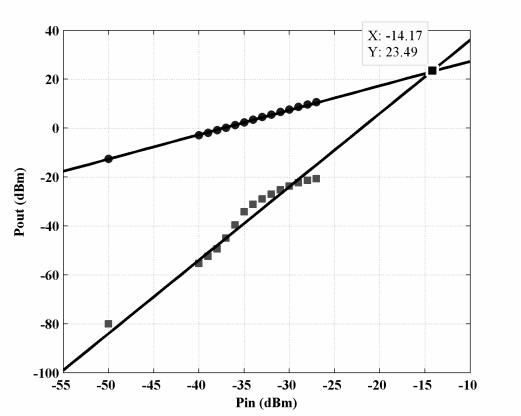

Fig.13. Measured receiver IIP_3.

For a fractional-N frequency synthesizer, two types of SDM have been reported. One is a single-loop modulator and the other is a cascaded modulator called MASH. Compared with the latter, single-stage architecture has a better noise shaping characteristic for DC inputs. So a third-order single-loop feed-forward $\Sigma\Delta$ modulator is implemented in the frequency synthesizer. To achieve sufficient output frequency resolution, the input length of the digital $\Sigma\Delta$ modulator is set to be 16 bit. With an input reference clock of 16 MHz, the achievable frequency resolution at the first divide-by-two output is around 120 Hz ($16\ \text{MHz}/2^{16+1}$).

LO buffers consume a substantial amount of power in a transceiver system. The mixers in the receiver and transmitter require a LO voltage swing of more than 600 mVpp, and they present a capacitive load of more than 300 fF, which makes the design of the LO buffer amplifier very challenging at RF frequencies. The LO buffer shown in Fig.9 is a modified Cherry-Hooper amplifier[9]. The traditional Cherry-Hooper stage has been modified by replacing resistive loads with a pMOS transconductor reusing nMOS biasing current. The slew rate of the amplifier is improved without additional power. The simulation result shows that I/Q LO buffers achieve a –3 dB bandwidth larger than 2.5 GHz with a current of 3 mA, which sufficiently satisfies our application.

4. Measurement results

A fully integrated 802.11b transceiver system is implemented in 0.18 μm 1P6M RF CMOS technology. The total die area including pads is 2.7×4.2 mm^2. Figure 10 shows the die microphotograph. The chip is directly bonded to a 4-layar FR-4 substrate for measurement, as shown in Fig.11.

An impedance matching network is designed on PCB to match the LNA input to a differential impedance of 100 Ω. An off-chip balun (TDK HMM1520) is used to convert a single-ended signal from SMA to differential LNA input. The measured S_{11} of LNA is −13.9 to −9.4 dB in the targeted 2.4–2.48 GHz frequency range, as shown in Fig.12. The shift of the minimum S_{11} in frequency is mainly caused by the parasitic of the PCB trace and bondwire inductance, whose values are hard to estimate in the design phase. The receiver noise figure is measured using the Y-factor method. The minimum noise figure of the entire receiver channel is 8.2 dB, about 4 dB higher than the worst case simulation result. However, all the PCB parasitic and losses are not de-embedded as they would be seen from an antenna mounted on the PCB in a final product. ESD protection circuits in the LNA pad may also cause degradation in noise performance. The maximum voltage gain is 81 dB. The linearity test is performed by applying two-tone signals at 1 MHz apart into the receiver input. Figure 13 shows that the measured IIP3 is −14 dBm when the LNA and the first VGA are in the high gain mode.

Figure 14 shows the result of the receiver demodulation test. A 2 Mbps DQPSK modulated 802.11b RF signal of −60 dBm is sent to the LNA input, a dual channel oscilloscope (Infiniium 54830D) samples the I/Q baseband signal at the receiver output, the sampled data are connected to the 89600 Vector Signal Analyzer for digital demodulation. The received signal has an RMS EVM of 18%, corresponding to about 15 dB SNR after ADC sampling. The measured I/Q gain/phase

Table 2. Performance summary.

RX S_{11}	< −9.4 dB	TX S_{22}	< −13 dB
RX maximum gain	81 dB	TX maximum output power	–3.4 dBm
RX noise figure	8.2 dB	TX LO feedthrough	–34 dBc
RX IIP_3	–14 dBm	TX OIP3	+12.7 dBm
DCOC cutoff frequency	10 kHz	RMS EVM	6.8%
RX IQ imbalance	0.1 dB/0.2 °	TX IQ imbalance	0.2 dB/6 °
Synthesizer phase noise	–71.5 dBc/Hz@100 kHz offset, –122.7 dBc/Hz@3 MHz offset		

Table 3. Comparison to the state-of-the-art implementations*.

	Technology	Supply (V)	RX NF (dB)	RX gain (dB)	RX IIP_3 (dBm)	TX OIP_3 (dBm)	TX output power (dBm)	Power RX/TX (mW)
JSSC,2005[10]	0.18 μm CMOS	1.8	4.8	88	-15	N/A	13	165/360
JSSC,2006 [11]	0.25 μm SiGe	2.8	4.0	66	-11	15	-5	140/129
ISSCC, 2007 [12]	0.13 μm CMOS	1.2/2.5	3.5	N/A	-13	N/A	-2.5	128/151
JSSC,2008[13] **	0.13 μm CMOS	1.2	4	95	N/A	N/A	9.5	85/125
This work	0.18 μm CMOS	1.8	8.2	81	-14	12.7	-3.4	74/81

* For multi-mode SOC, only the radio transceiver's performance in 802.11b mode is compared. The power consumption includes PLL and LO buffers.

** Single Weight Combiner system utilizing a two-antenna array receiver.

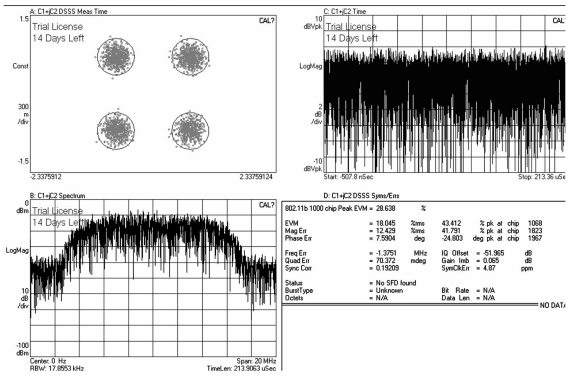

Fig.14. Receiver demodulation performance.

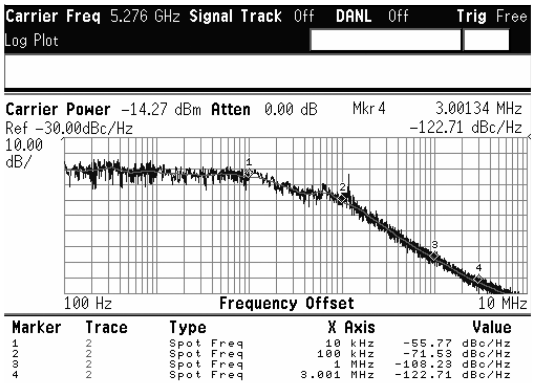

Fig.15. Measured synthesizer phase noise.

mismatchs are less than 0.1 dB and 0.2 ° , respectively.

The integrated frequency synthesizer is tested from a pair of open-drain buffers at the VCO output. The measured phase noise is −71.5 dBc/Hz at the 100 kHz offset and −122.7 dBc/Hz at the 3 MHz offset, as shown in Fig.15. The transmitter measurement results have been published in Ref.[2].

Table 2 summaries the performance of the measured IC. The measurement results reported in this paper include all the PCB related parasitic, and all pads are ESD protected. The presented transceiver system adequately meets the specification of the 802.11b PHY standard, while being compared favourably to the state-of-the-art on power dissipation. Table 3 gives the comparison results and it clearly indicates the low-power trend in recent transceiver developments.

5. Conclusion

A monolithic CMOS transceiver operating in 2.4 GHz band has been reported. The complete transceiver system integrates the RF front-end and analog baseband circuits of the receiver and transmitter, as well as a ΣΔ fractional-N frequency synthesizer. System level considerations and low power circuit design techniques are presented. Measurement results indicate that the transceiver is a low-power, low cost solution for 802.11b wireless LAN applications.

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