A linear stepping PGA used in CMOS image sensors*

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Abstract: A low power linear stepping digital programming gain amplifier (PGA) is designed for CMOS image sensors. The PGA consists of three stages with gain range from one to nine. The gain is divided into four regions and each range has 128 linear steps. Power consumption of the PGA is saved by good tradeoff between variation of amplifier feedback coefficient, pipeline stages and gain regions. With thermometer-binary mixed coding and linear pipeline gain stepping, the load capacitance keeps constant when the gain of one stage is changed. The PGA is designed in the SMIC 0.18 μm process. Simulation results show that the power consumption is 3.2 mW with 10 bit resolution and 10 MSPS sampling rate. The PGA has been embedded in a 0.3 megapixel CMOS image sensors and fabricated successfully.

Key words: CMOS image sensor; programmable gain amplifier; linear stepping; low power consumption
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1. Introduction

In recent years, vision systems based on CMOS image sensors (CIS) have acquired significant ground over those based on charge-coupled devices. The advantages of CIS are their high level of integration, random accessibility, low-voltage, low-power operation, and low cost. Silicon photodiode has different photo response properties from red, green, and blue incident photo, so a digital programmable gain amplifier (PGA) is usually used to condition image signal[1]. Traditional decibel stepping PGA has defects of great variation feedback coefficient and high power consumption. In this paper, a low power linear-stepping switch capacitor PGA is presented. With multi-stage structure and pipeline stepping, variations of feedback coefficient and load capacitance are suppressed and power consumption of the amplifier is decreased. The PGA has high common mode rejection ratio with full differential structure. Thermometer-binary mixed coding brings good capacitance matching and lesser control lines. The PGA is suitable for low power CIS.

2. The basic principle of PGA

There are two gain stepping methods in digital PGA, decibel stepping and linear stepping. Decibel stepping has merits of high speed, high gain linearity and weakness of non-uniform gain, bad capacitor matching and great variation of feedback coefficient[2]. Both feedback coefficient and load capacitance will change when gain of the traditional decibel stepping PGA changes, which will affect bandwidth and stability. Figure 1 shows a decibel stepping two-stage PGA structure. Gain is determined by feedback nets. Coarse gain selection is done by the first stage and accurate gain selection is done by the second stage. In Fig.1, C_{S1} and C_{S2} are the sampling capacitors; C_{F1} and C_{F2} are the feedback capacitors. A_1 and A_2 are the gain of the amplifier; D_1 and D_2 are the control codes.

A new gain allocation in the pipeline is presented. The full gain is divided into n pipeline stages. The former stage sampling capacitance $C_s(n-1)$ and the current stage sampling capacitance $C_s(n)$ construct arithmetic progression. When the gain of one stage changes, gain and load capacitance of the other stage keep fixed, which is beneficial for amplifier stability and reducing dynamic power consumption.

3. Improved linear stepping PGA design

Figure 2 shows an M stage linear stepping PGA with improved gain allocation. "D" is the control code and "Start" is the initial value of control code. $S_1, S_2, \cdots, S_m$ are the control codes when the first, second, and m-th stages finish stepping. A_S is the gain of the current stage and A_{Loop} is the gain of the whole PGA.

When $D <$ Start, the sampling capacitance is equal to feedback capacitance in every stage and gain of every stage is one. The full gain of PGA is one. Every stage works in fixed feedback coefficient mode with constant feedback coefficient and load capacitance.

When Start $< D < S_1$, the gain of the first stage increases. The gain of the other stages keep constant. The sampling capacitance of the first stage linearly increases as the gain control signal D increases. Gain step of the first stage is equal to the system gain step S and full gain G_{Total} is equal to the first stage gain G_{S1}:

$$G_{Total} = G_{S1} \times G_{S2} \times \cdots \times G_{SM} = \frac{C_1 + n_1 C_d}{C_1} = 1 + n_1 S, \quad (1)$$

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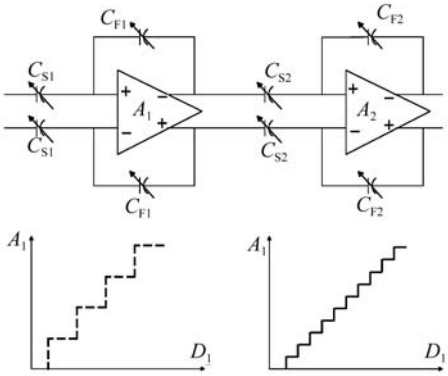

Fig.1. Two stages pipeline PGA system.

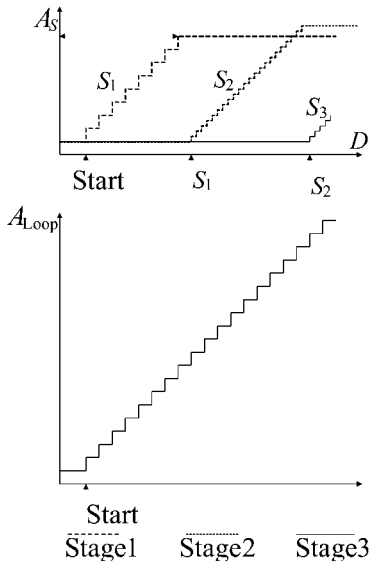

Fig.2. M stages PGA.

where n_1 is the number of gain steps, C_d is the unit increase of sampling capacitance, and C_1 is the feedback capacitance of the first stage. System gain increases uniformly.

When $S_1 < D < S_2$, the gain increase of the first stage stops and its gain is $G_1 = 1 + n_1 S$. Then the gain increase of the second stage starts, while the gains of the other stages keep constant. Set C_{S2} and C_{F2} equal to $C_1 + n_1 C_d$ when the second stage gain is 1, then the gain steps are determined by n_1 and C_d, as follows:

$$S_2 = \frac{C_d}{C_1 + n_1 C_d}. \tag{2}$$

The PGA system gain is

$$G_{total} = G_{S1} \times G_{S2} = \frac{C_1 + n_1 C_d}{C_1} \times \left[\frac{C_{S2}}{C_{F2}} + (n_2 - n_1)\frac{C_d}{C_1 + n_1 C_d}\right] = \frac{C_1 + n_2 C_d}{C_1} = 1 + n_2 S. \tag{3}$$

System gain increases by step S. Only the load capacitance of the first stage increases evenly in the process, while the load capacitance of other stages keep constant. The rest stages can be deduced by analogy: when $S_{m-1} < D < S_m$, the gain of the $(m-1)$-th stage is $G_{m-1} = 1 + n_{m-1} S$. Now the gain increase is done by the m-th stage, and the gain step of the m-th stage is determined by n_{m-1} and C_d.

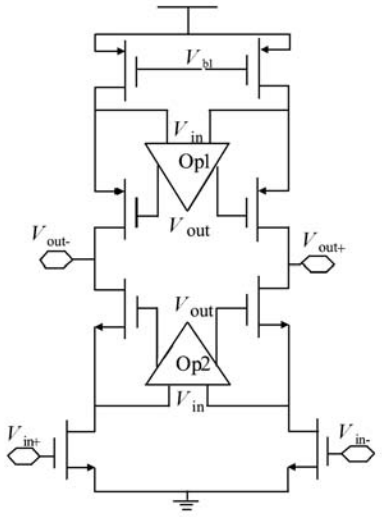

Fig.3. Schematic of operational amplifier.

$$S_m = \frac{C_d}{C_1 + n_{m-1} C_d}. \tag{4}$$

The PGA system gain is

$$G_{Total} = G_{S1} \times \cdots \times G_{Sm} = 1 + n_m S. \tag{5}$$

System gain increases evenly by step S until maximum gain is achieved. This method reduces variation of feedback nets and load capacitance, and dynamic power can be lowered.

4. Linear stepping PGA circuit design

4.1. Operational amplifier design

Errors of amplifier consist of static error and dynamic error. The static error is caused by finite gain while the dynamic error is caused by limited bandwidth. Operational amplifier (Op Amp) of every stage needs 12 bits accuracy for three stages PGA with 10 bits accuracy:

$$\frac{\frac{1}{\beta} - \frac{A}{1 + A\beta}}{\frac{1}{\beta}} \leqslant \frac{1}{2^{12}}. \tag{6}$$

A and β are respectively the direct current gain and feedback coefficient of the amplifier, and $A \geqslant 78.26$ dB is required theoretically. Telescopic cascode Op Amp with gain boost is adopted and the schematic is shown in Fig.3. The auxiliary gain boost Op Amp is a basic differential amplifier. Main Op Amp can supply 70 dB gain and auxiliary Op Amp can supply 20 dB gain. The main Op Amp is a single pole system and phase margin is easily met. Gain-bandwidth product (GBW) of the Op Amp with 12 bits accuracy and 10 MSPS is given by[3]

$$\text{GBW} > \frac{12 \ln 2 \left[1 + \frac{C_{i,tot}(C_L + C_f)}{C_f C_L}\right]}{2\pi T}. \tag{7}$$

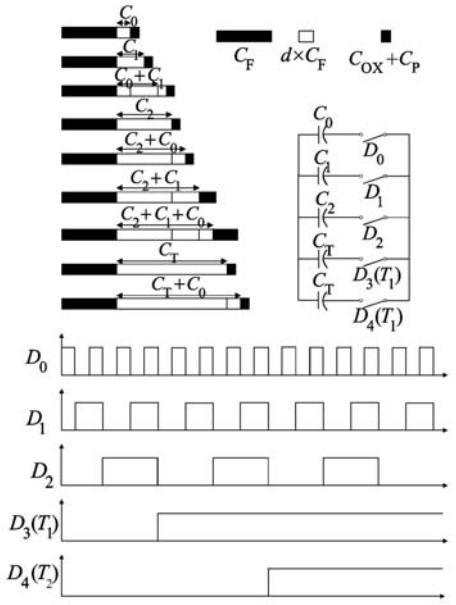

Fig.4. Mixed coding of thermometer and binary.

$C_{i,tot}$ is equal to $C_s + C_{in}$; C_s, C_f, C_L, C_{in} are respectively the sampling capacitance, feedback capacitance, load capacitance and parasitic capacitance. GBW > 98.2 MHz is required. Pole-zero doublet exists in the transfer function of main Op Amp, which could affect the closed loop time domain setting response[4]. Unit gain bandwidth of the auxiliary Op Amp must be larger than the closed loop unit gain bandwidth of main Op Amp to avoid slowing setting time. In order to keep phase margin of main Op Amp large enough, unit gain bandwidth of the auxiliary Op Amp must be less than second pole of the main Op Amp[5]. Simulation results show that the gain is 83.37 dB, bandwidth is 118.3 MHz, and phase margin is 81.52 ° .

4.2. Stages of pipeline PGA design

The PGA for CIS has a gain range from one to nine. Analog image signals are sampled and amplified by every stage. Total errors of PGA accumulate by each stage. For a 10 bits accuracy, m stages pipeline, the error caused by finite direct current gain can be depicted as

$$A_{error} \approx \sum_{n=1}^{m}\left(\frac{1}{A_{DC(n)}}\right) \approx m\frac{1}{A_{DC}}. \tag{8}$$

Direct current gain requirement will increase as the m increases. Three stages pipeline is adopted to meet 10 bits accuracy. Four gain regions and 128 stepping stages in every gain region are selected, which can meet the accuracy requirement of CIS.

4.3. Pipeline PGA capacitor array coding design

There are two kinds of sampling capacitor array coding: binary coding and thermometer coding[6]. Layout of thermometer coding is large and difficult to route, while the binary coding has large variation of sampling capacitance, and there is glitch when the gain changes. Thermometer-binary mixed coding shown in Fig.4 balances capacitance matching and routing complexity. An example of 23 gain steps is shown in Table 1. Sampling array contains of 5 capacitors, and the control signal is 5 bit. C_F is the feedback capacitance, $C_0 = dC_F$ is the unit capacitance, C_1 and C_2 is the capacitance with binary weight, C_T is the unit thermometer capacitance, C_{ox} is the oxide capacitance, and C_P is the parasitic capacitance. C_T is equal to 2^3C_0. Control signal consists of two bits thermometer coding and three bits binary coding, and uniform linear stepping with the mixed coding is realized.

Table 1. Truth table of mixed coding.

D_4	D_3	D_2	D_1	D_0	$C_{S,en}$
0	0	0	0	1	C_0
0	0	0	1	0	$C_1 = 2C_0$
0	0	0	1	1	$C_1 + C_0 = 3C_0$
0	0	1	0	0	$C_2 = 4C_0$
0	0	1	0	1	$C_2 + C_0 = 5C_0$
0	0	1	1	0	$C_2 + C_1 = 6C_0$
0	0	1	1	1	$C_2 + C_1 + C_0 = 7C_0$
0	1	0	0	0	$C_T = 8C_0$
..	..	..	..	..	..
1	1	1	1	1	$C_2 + C_1 + C_0 + 2C_T = 23C_0$

Table 2. Specification of PGA.

Process	0.18 μm
Sampling rate	10 MSPS
Gain range	1–3; 1.5–4.5; 2–6; 3–9
Supply voltage	1.8 V
Gain control methods	Linear
Resolution	10 bit
Output range	Differential 1.2 V
Gain stepping accuracy	128 stages/region
Power consumption	3.2 mW

The PGA is divided into three stages. The first stage is controlled by two bits binary code, which realizes selection of four gain regions. The second and third stages are controlled by seven bits code which realizes 128 linear gain steps. The second stage control codes are binary coding (2 : 0) and thermometer coding (2 : 0), which realize 32 bits linear gain steps. The third stage is controlled by binary coding (2 : 0) and thermometer coding (10 : 0), which realizes 96 bits linear gain steps. The 32 gain steps provided by the second stage increase firstly and then the 96 gain steps provided by the third stage starts to increase. In each of the four gain regions, 128 linear gain steps are implemented. The gain steps method keeps sampling capacitance at minimum value, which can reduce dynamic power consumption of the PGA. Only gain of one stage is changing in mixed coding PGA. Variation of load capacitance and charge-discharge probability are reduced and dynamic power consumption of PGA is lowered.

The PGA in this paper is designed in SMIC 0.18 μm process. The simulation results are shown in Fig.5 (a). When the gain of the PGA increases linearly, the output voltage increases linearly at fixed input voltage value. Figure 5 (b) shows the relation curve of gain and control code. In Fig.5 (b), "a" represents gain of the first stage and its value can be 1, 1.5, 2 and

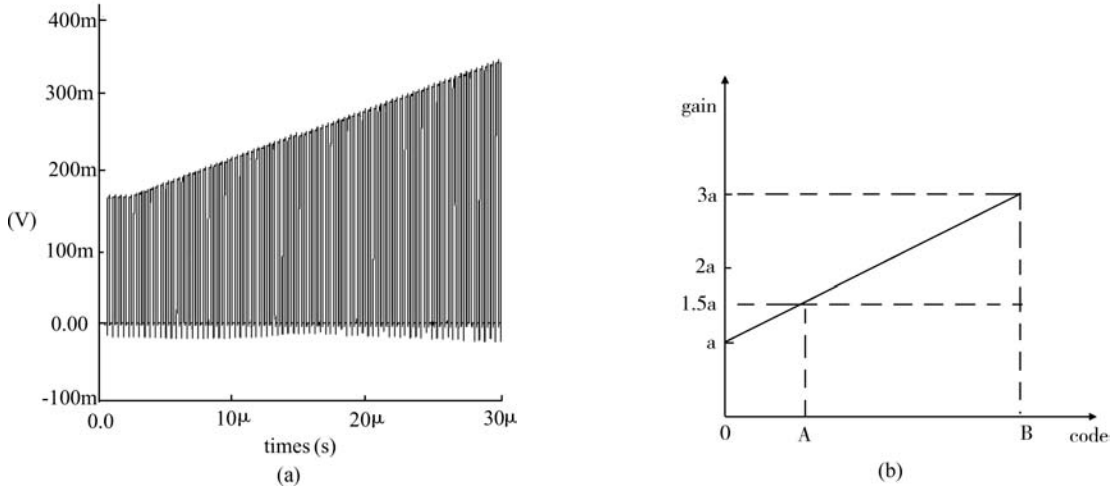

Fig.5. (a) Output voltage versus time; (b) Gain versus control code.

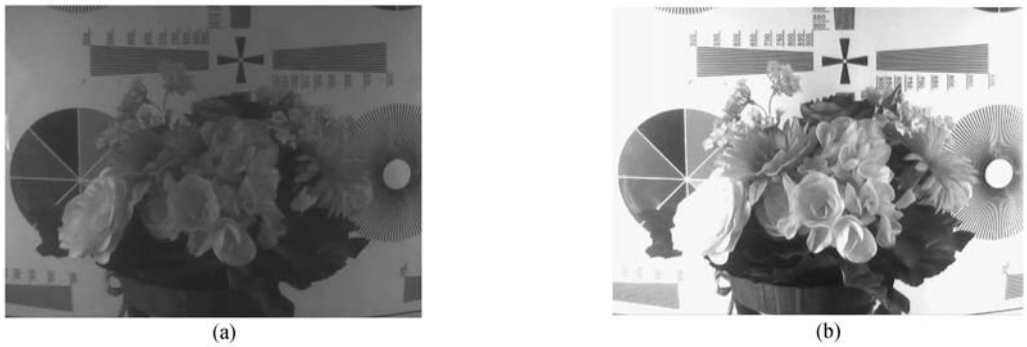

Fig.6. Photograph tested: (a) Gain is 1; (b) Gain is 9.

3. Region 0–A depicts that the second stage gain increases linearly (1–1.5) as control code increases (000000–111111), while the gain of the third stage keeps at 1. Region A–B depicts the third stage gain increases linearly (1–2) as control code increase (00000000000000–11111111111111), while the second stage gain keeps at 1.5.

The detailed specifications of the PGA are shown in Tabel 2. Furuta and Kawahito reported a PGA chip designed in 0.6 μm process. The specifications are 20 MSPS sampling rate, 9 bits accuracy, –6 to 30 dB gain range and 120 mW power consumption[1]. Power consumption of the PGA presented in this paper is 3.2 mW, which is much lower than the value reported in Furuta's paper[1]. The PGA is embedded in a 0.3 megapixels CIS. In September 2007, the CIS chip was successfully fabricated in SMIC 0.18 μm process multi-project wafer. Figure 6 shows the photograph shot by the CIS in the condition of 30 lux light intensity and 30 ms exposure time. Figure 6 (a) shows the image shot when PGA gain is 1, while Figure 6 (b) shows the image shot when PGA gain is 9. Change of gray level in the picture depicts gain change of PGA.

5. Conclusion

A three stage pipelines structure digital PGA designed for CIS was designed in this paper. The gain of the PGA is divided into four regions and each region has 128 linear steps. The PGA meets the accuracy requirement of the image signal gain adjustment. Thermometer-binary mixed coding improves the capacitance matching, reduces routing complexity. Simulation and fabrication results show that the digital PGA has advantages of linear stepping and low power. The PGA can be embedded in CIS chip.

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